CURRICULUM VITÆ

CONTACT INFORMATION

4-155 Keller Hall
200 Union St. S.E., Minneapolis, MN, 55455

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RESEARCH INTERESTS

Computer architecture, impact of technology on computing, energy-efficient computing, application-domain specialized architectures, approximate computing, computing at ultra-low voltages.

BACKGROUND

University of Minnesota Twin Cities

Assistant Professor in Electrical and Computer Engineering (ECE) August 2012-
Graduate Faculty in Computer Science and Engineering (CSci) April 2013-

University of Illinois at Urbana-Champaign (UIUC)

Ph.D. in Electrical and Computer Engineering August 2012

- Dissertation: *Novel Many-core Architectures for Energy-efficiency*
- Advisor: Prof. Josep Torrellas

M.S. in Electrical and Computer Engineering December 2009

- Thesis: *Managing Many-core Aging*
- Advisor: Prof. Josep Torrellas

İstanbul Teknik Üniversitesi (İTÜ)

B.S. (Double Major) in Computer Engineering June 2005

- Thesis: *Automatic Verilog Code Generation Through Grammatical Evolution*
- Advisor: Prof. Şima Etaner Uyar

B.S. in Electronics and Telecommunication Engineering June 2004

- Thesis: *Analysis of Low Offset Current Differencing Input Stages of Current Mode Circuits*
- Advisor: Prof. Ali Toker

Österreichisches Sankt Georgs Kolleg (Austrian School), İstanbul 1992-2000

PUBLICATIONS

[1] L. Wang, S. K. Khatamifard, **U. R. Karpuzcu**, and S. Kose. Mitigation of NBTI Induced Performance Degradation in On-Chip Digital LDOs. *IEEE/ACM Design, Automation & Test in Europe, DATE*, March 2018. Acceptance rate: 23.7%.

[2] F. Betzel, S. K. Khatamifard, H. Suresh, D. J. Lilja, J. Sartori, and **U. R. Karpuzcu**. Approximate Communication: Approximation Techniques for Communication Reduction in Parallel Systems. *ACM Computing Surveys*, 51(1), January 2018.

[3] S. K. Khatamifard, H. Najafi, A. Ghoreyshi, **U. R. Karpuzcu**, and D. J. Lilja. StochMem: Towards Seamless Stochastic Computing Systems with Analog Memories. *Computer Architecture Letters (CAL)*, January 2018. In press.

[4] S. K. Khatamifard, I. Akturk, and **U. R. Karpuzcu**. On Approximate Speculative Lock Elision. *IEEE Transactions on Multiscale Computing Systems, Special Issue on Emerging Technologies and Architectures for Manycore Computing*, November 2017. In press.

[5] S. K. Khatamifard, M. Razaviyayn, and **U. R. Karpuzcu**. BioArch: A Reconfigurable Hardware Accelerator Designed for Bioinformatics Workloads. *Accepted for presentation in The Cold Spring Harbor Laboratory Conference on Genome Informatics*, November 2017. 42 out of approx. 228 submissions (%18.4) accepted as talk.

[6] S. K. Khatamifard, M. Razaviyayn, and **U. R. Karpuzcu**. Binary Neural Networks for Hashing Denovo Transcriptome Sequences. *Accepted for poster presentation in The Southern California Machine Learning Symposium (SoCal ML)*, October 2017.

[7] S. K. Khatamifard, L. Wang, W. Yu, S. Kose, and **U. R. Karpuzcu**. ThermoGater: Thermally-Aware Distributed On-Chip Voltage Regulation. *IEEE/ACM International Symposium on Computer Architecture, ISCA*, June 2017. Acceptance rate: 16.8%.

[8] I. Akturk and **U. R. Karpuzcu**. AMNESIAC: Trading Computation for Communication for Energy Efficiency. *ACM International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS*, April 2017. Acceptance rate: 17.4%.

[9] Z. Chowdhury, J. D. Harms, S. K. Khatamifard, M. Zabihi, Y. Lv, A. P. Lyle, S. S. Sapatnekar, **U. R. Karpuzcu**, and Jian-Ping Wang. Efficient In-Memory Processing Using Spintronics. *Computer Architecture Letters (CAL)*, 2017. In press.

[10] Longfei Wang, S. K. Khatamifard, Orhun Uzun, **U. R. Karpuzcu**, and S. Kose. Efficiency, Stability, and Reliability Implications of Unbalanced Current Sharing among Distributed On-Chip Voltage Regulators. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 25(11), 2017.

[11] I. Akturk, R. Akram, M. Majharul, A. Muzahid, and **U. R. Karpuzcu**. Accuracy Bugs: A New Class of Concurrency Bugs to Exploit Algorithmic Noise Tolerance. *ACM Transactions on Architecture and Code Optimization, TACO (invited to HiPEAC)*, 13(4), December 2016.

[12] S. K. Khatamifard, M. Resch, N. S. Kim, and **U. R. Karpuzcu**. VARIUS-TC: A Modular Architecture-Level Model of Parametric Variation for Thin-Channel Switches. In *IEEE International Conference on Computer Design, ICCD*, October 2016. Acceptance rate: 28.9%.

[13] D. Skarlatos, R. Thomas, A. Agrawal, S. Qin, R. Pilawa-Podgurski, **U. R. Karpuzcu**, R. Teodorescu, N. S. Kim, and J. Torrellas. Snatch: Opportunistically Reassigning Power Allocation between Processor and Memory in 3D Stacks. In *IEEE/ACM International Symposium on Microarchitecture, MICRO*, October 2016. Acceptance rate: 22%.

[14] A. Paul, S. P. Park, D. Somasekhar, Y. M. Kim, N. Borkar, **U. R. Karpuzcu**, and C. H. Kim. System-Level Power Analysis of a Multicore Multipower Domain Processor With On-Chip Voltage Regulators. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 24(12), 2016.

[15] H. R. Ghasemi, **U. R. Karpuzcu**, and N. S. Kim. Comparison of Single-ISA Heterogeneous versus Wide Dynamic Range Processors for Mobile Applications. In *IEEE International Conference on Computer Design, ICCD*, October 2015. Acceptance rate: 31%.

[16] I. Akturk, S. K. Khatamifard, and **U. R. Karpuzcu**. On Quantification of Accuracy Loss in Approximate Computing. *12th Annual Workshop on Duplicating, Deconstructing and Debunking colocated with ISCA*, July 2015.

[17] I. Akturk, N. S. Kim, and **U. R. Karpuzcu**. Decoupling Control and Data Processing for Approximate Near-threshold Voltage Computing. *IEEE Micro Special Issue on Heterogeneous Computing*, July/August 2015.

[18] A. Sinkar, H. Ghasemi, M. Schulte, **U. R. Karpuzcu**, and N. S. Kim. Low-Cost Per-Core Voltage Domain Support for Power-Constrained High-Performance Processors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 22(4), April 2014.

[19] **U. R. Karpuzcu**. AMNESIAC: Amnesic Automatic Computer. In *Wild & Crazy Ideas Session at ACM International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS*, March 2014.

[20] **U. R. Karpuzcu**, I. Akturk, and N. S. Kim. Accordion: Toward Soft Near-threshold Voltage Computing. In *IEEE/ACM International Symposium on High Performance Computer Architecture, HPCA*, February 2014. Acceptance rate: 25.6%.

[21] **U. R. Karpuzcu**, N. S. Kim, and J. Torrellas. Coping With Parametric Variation at Near-Threshold Voltages. *IEEE Micro Special Issue on Reliability*, July/August 2013.

[22] **U. R. Karpuzcu**, A. Sinkar, N. S. Kim, and J. Torrellas. Toward Energy-Efficient Many-Cores for Near-threshold Voltage Computing. In *IEEE/ACM International Symposium on High Performance Computer Architecture, HPCA*, February 2013. Acceptance rate: 21%.

[23] **U. R. Karpuzcu**, K. Kolluru, N. S. Kim, and J. Torrellas. VARIUS-NTV: A Microarchitectural Model to Capture the Increased Sensitivity of Many-Cores to Process Variations at Near-Threshold Voltages. In *IEEE International Conference on Dependable Systems and Networks, DSN*, June 2012. Acceptance rate: 17%.

[24] B. Greskamp, **U. R. Karpuzcu**, and J. Torrellas. LeadOut: Composing Low Overhead Frequency Enhancing Techniques for Single Thread Performance in Configurable Multicores. In *IEEE/ACM International Symposium on High Performance Computer Architecture, HPCA*, January 2010. Acceptance rate: 18%.

[25] **U. R. Karpuzcu**, B. Greskamp, and J. Torrellas. The BubbleWrap Many-Core: Popping Cores for Sequential Acceleration. In *IEEE/ACM International Symposium on Microarchitecture, MICRO*, December 2009. Acceptance rate: 24.9%. Recipient of The **Best Paper Award**.

[26] B. Greskamp, **U. R. Karpuzcu**, and J. Torrellas. BubbleWrap: Popping CMP Cores for Per-Thread Performance. In *Wild & Crazy Ideas Session at ACM International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS*, March 2009. Recipient of The Best Idea Award.

[27] B. Greskamp, L. Wan, **U. R. Karpuzcu**, J. Cook, J. Torrellas, D. Chen, and C. Zilles. BlueShift: Designing Processors for Timing Speculation from the Ground Up. In *IEEE/ACM International Symposium on High Performance Computer Architecture, HPCA*, February 2009. Acceptance rate: 19%.

[28] Man-Lap Li, P. Ramachandran, **U. R. Karpuzcu**, S. K. S. Hari, and S. Adve. Accurate Microarchitecture-level Fault Modeling for Studying Wear-out Faults. In *IEEE/ACM International Symposium on High Performance Computer Architecture, HPCA*, February 2009. Acceptance rate: 19%.

[29] **U. R. Karpuzcu**. Automatic Verilog Code Generation Through Grammatical Evolution. In *Genetic and Evolutionary Computation Conference*, GECCO, *Undergraduate Student Workshop*, 2005.

RESEARCH EXPERIENCE

Lead, ALTAI Group, UMN August 2012 -

Exploring how to improve the energy efficiency of computing in the face of limitations induced by contemporary device scaling via

(i) Pushing traditional (CMOS-based) computing to its limits by

- **Approximate Near-threshold Voltage Computing** [20, 17, 12],
- **Approximate Synchronization** [16, 11, 2, 4],
- **Architectural Exploration of Thermally-Aware On-Chip Voltage Regulation** [7, 1, 10],
- **Trading Computation for Communication for Energy Efficiency** [19, 8]; and

(ii) Computing with post-CMOS devices and paradigms by

- **Scalable In-Memory Processing Using Spintronics** [9],
- **Application Domain Specific Architectures for Bioinformatics** [5, 6],
- **Memory System Design for Stochastic Computing** [3].

Graduate Research Assistant, i-acoma Group, UIUC May 2008 - August 2012

Adviser: Prof. Josep Torrellas

Near-threshold Voltage Computing (NTC): Explored (μ)architectural implications of NTC, which facilitates energy-efficient execution for throughput-critical applications by reducing the supply voltage to a value only slightly higher than the threshold voltage [23, 22, 21].

Many-core Energy Efficiency and Reliability: Explored (μ)architectural implications of increasing chip power density over technology generations. Introduced the BubbleWrap many-core [25, 26], a novel architecture trading processor aging rate for energy efficiency.

Timing Speculation: Contributed to the development of a CAD (computer aided design) tool tailored for timing speculation [27], and to the exploration of where timing speculation fits in the design space to accelerate single-thread execution [24].

Graduate Research Intern, Intel Labs, Hillsboro Summer 2011

Mentor: Dr. Chris Wilkerson

Developed an analytical model and simulation infrastructure to assess the impact of supply voltage noise at near-threshold voltages.

Graduate Research Intern, AMD Research, Austin Summer 2009

Mentor: Dr. Jaewoong Chung

To provide basic compiler support for AMD's ASF (Advanced Synchronization Facility), developed a shim software layer mapping the transactional memory branch of gcc's runtime to ASF ISA.
US Patent 9110691, "Compiler Support Technique for Hardware Transactional Memory Systems", J. Chung, R. U. Karpuzcu, D. Christie, M. P. Hohmuth, S. Diestelhorst, M. T. Pohlack. Date of filing: November, 2010; Date of publication: August, 2015.

Fulbright Fellow, ECE, UIUC August 2006 – May 2008

Adviser: Prof. Sarita Adve

Developed the initial version of SWATSim [28], a hierarchical fault-injection infrastructure to study system-level manifestations of permanent faults.

Undergraduate Intern, İTÜ ETA Foundation ASIC Design Center, İstanbul Summer 2003
Mentor: Prof. Ali Zeki
Designed a Miller OTA and a frequency divider.

TEACHING EXPERIENCE

Instructor, ECE, University of Minnesota
- EE5340 Physics of Computing: Basics (formerly EE5940/8950) Spring'17,15,14
- EE4363/CSci4203 Computer Architecture & Machine Organization Spring'18,16; Fall'16,14,13
- EE5364/CSci5204 Advanced Computer Architecture Fall'17,15,12

Discussion Section Instructor, ECE, University of Minnesota
- EE2301 Introduction to Digital Design Fall'13-

Guest Lecturer & Teaching Assistant, ECE, UIUC
- ECE/CS533 Parallel Computer Architecture Spring'09

(INVITED) TALKS

Amnesic Automatic Computer: Trading Computation for Communication for Energy Efficiency, ARM Research Summit, Cambridge, UK, September 2017.

ThermoGater: Thermally-Aware Distributed On-Chip Voltage Regulation, International Symposium on Computer Architecture, ISCA, Toronto, Canada, June 2017.

AMNESIAC: Trading Computation for Communication for Energy Efficiency, ACM International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS, Xian, China, April 2017.

Accuracy Bugs: A New Class of Concurrency Bugs to Exploit Algorithmic Noise Tolerance, HiPEAC, Stockholm, Sweden, January 2017.

On Quantification of Accuracy Loss in Approximate Computing, Dagstuhl Seminar 15491, Approximate and Probabilistic Computing: Design, Coding, Verification, Saarbrucken, Germany, November 29 – December 4 2015.

Rethinking Computer Architecture in the Dark Silicon Era, "A Roadmap for EDA Research in the Dark Silicon Era" Workshop colocated with International Conference on Computer Aided Design, ICCAD, San Jose, CA, November 2014.

Boosting the Energy Efficiency of Computing, Computer Architecture Seminar Series, IBM T. J. Watson Research Center, Yorktown Heights NY, May 2014.

AMNESIAC: Amnesic Automatic Computer, Wild & Crazy Ideas Session at International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS, Salt Lake City, UT, March 2014.

Accordion: Toward Soft Near-threshold Voltage Computing, International Symposium on High Performance Computer Architecture, HPCA, Orlando, FL, February 2014.

Near-threshold Voltage Computing: A Systems Perspective, Computer Science & Engineering Colloquia Lecture Series, University of Minnesota, September 2013.

Toward Energy-Efficient Many-Cores for Near-threshold Voltage Computing, International Symposium on High Performance Computer Architecture, HPCA, Shenzhen, China, February 2013.

VARIUS-NTV: Capturing the Increased Sensitivity of Manycores to Process Variations at Near-Threshold Voltages, First Workshop on Near-threshold Voltage Computing (colocated with MICRO), Vancouver, BC, Canada, December 2012.

VARIUS-NTV: A Microarchitectural Model to Capture the Increased Sensitivity of Many-Cores to Process Variations at Near-Threshold Voltages, International Conference on Dependable Systems and Networks, DSN, Boston, MA, USA, June 2012.

Novel Many-Core Architectures for Energy-Efficiency,
Department of Information Technology and Electrical Engineering, ETH Zürich, April 2012.
Department of Computer Science, ETH Zürich, March 2012.
Department of Electrical and Computer Engineering, University of Minnesota, March 2012.
Department of Computer Engineering, Brown University, February 2012.
Department of Computer Science and Engineering, Arizona State University, February 2012.

Coping with the Larger Impact of Process Variations in Near-Threshold Computing, Intel Labs, Hillsboro,

OR, USA, December 2010.

Pushing Back the Many-Core Power Wall, Architecture Highlights 2010 – IBM Architecture PIC Student Workshop, IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, October 2010.

LeadOut: Composing Low Overhead Frequency Enhancing Techniques for Single Thread Performance in Configurable Multicores, International Symposium on High Performance Computer Architecture, HPCA, Bangalore, India, January 2010.

The BubbleWrap Many-Core: Popping Cores for Sequential Acceleration, International Symposium on Microarchitecture, MICRO, New York, NY, USA, December 2009.

Automatic Verilog Code Generation Through Grammatical Evolution, Genetic and Evolutionary Computation Conference, GECCO, Undergraduate Student Workshop, Washington DC, USA, June 2005.

SERVICE

Technical Program Committee Member

IEEE/ACM International Symposium on High Performance Computer Architecture (HPCA), 2016, 2014; IEEE/ACM International Symposium on Microarchitecture (MICRO), 2015; IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2017, 2016, 2015; IEEE International Symposium on Workload Characterization (IISWC), 2017; IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2016, 2015; IEEE/ACM International Symposium on Parallel Architectures and Compilation Techniques (PACT), 2014; IEEE International Conference on Computer Design (ICCD), 2017, 2016; IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2017; ACM International Conference on Supercomputing (ICS), 2016; Third Workshop on Approximate Computing (WAX), colocated with International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2018, 2016; Student Research Competition (SRC) at ASPLOS 2015; First & Second Workshop on Near-threshold Voltage Computing, colocated with MICRO 2012 and IEEE/ACM International Symposium on Computer Architecture (ISCA) 2014; ACM Great Lake Symposium on VLSI (GVLSI), 2018; IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2016, 2015; IEEE/ACM International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), 2015

External Review Committee Member

ISCA 2017, 2016, 2015; HPCA 2015; PACT 2017

Co-organizer

First & Second Workshop on Near-threshold Voltage Computing