# The BubbleWrap Many-Core:
## Popping Cores for Sequential Acceleration

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# Problem: The Power Wall

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## Ideal Scaling

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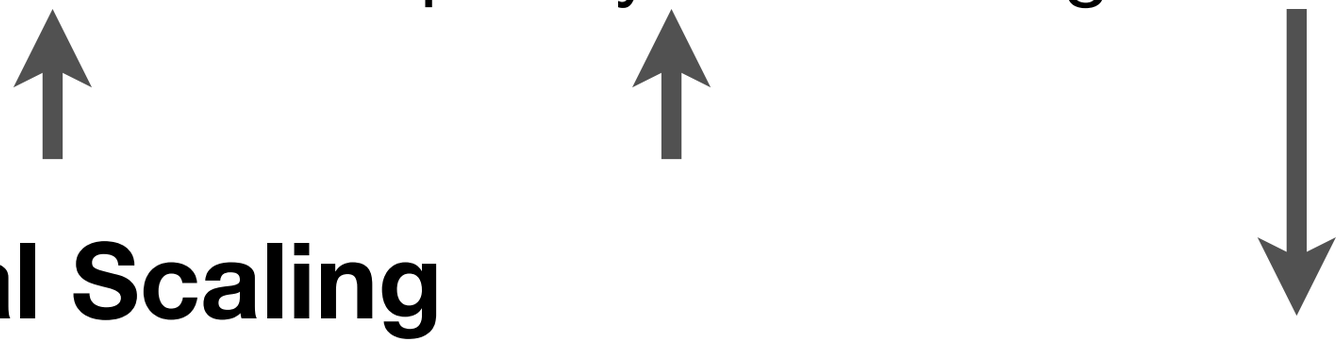

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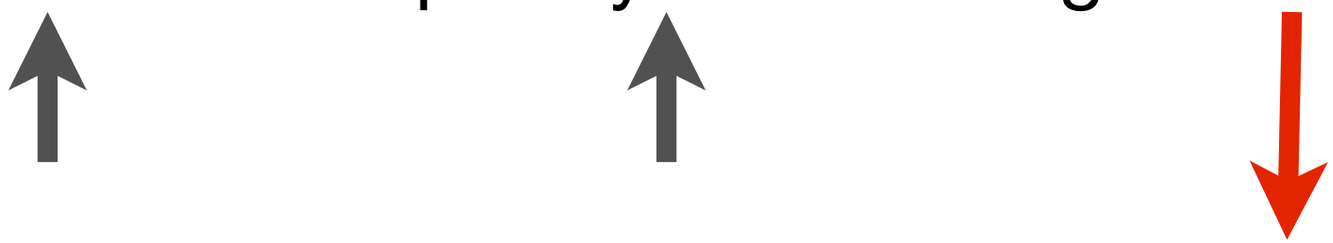


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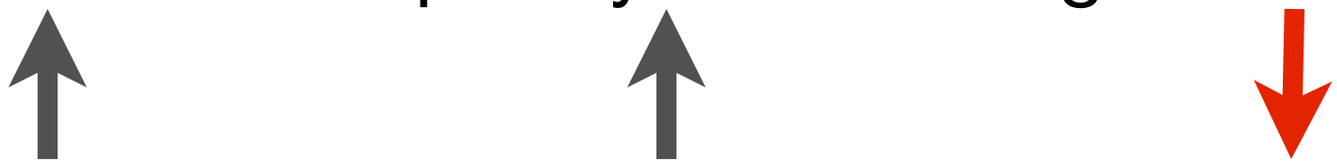


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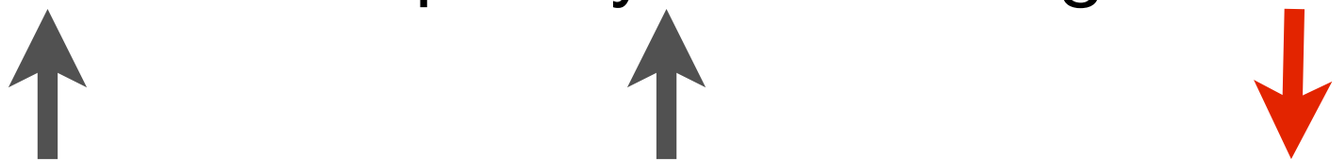


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**Dynamic Power Density is increasing**

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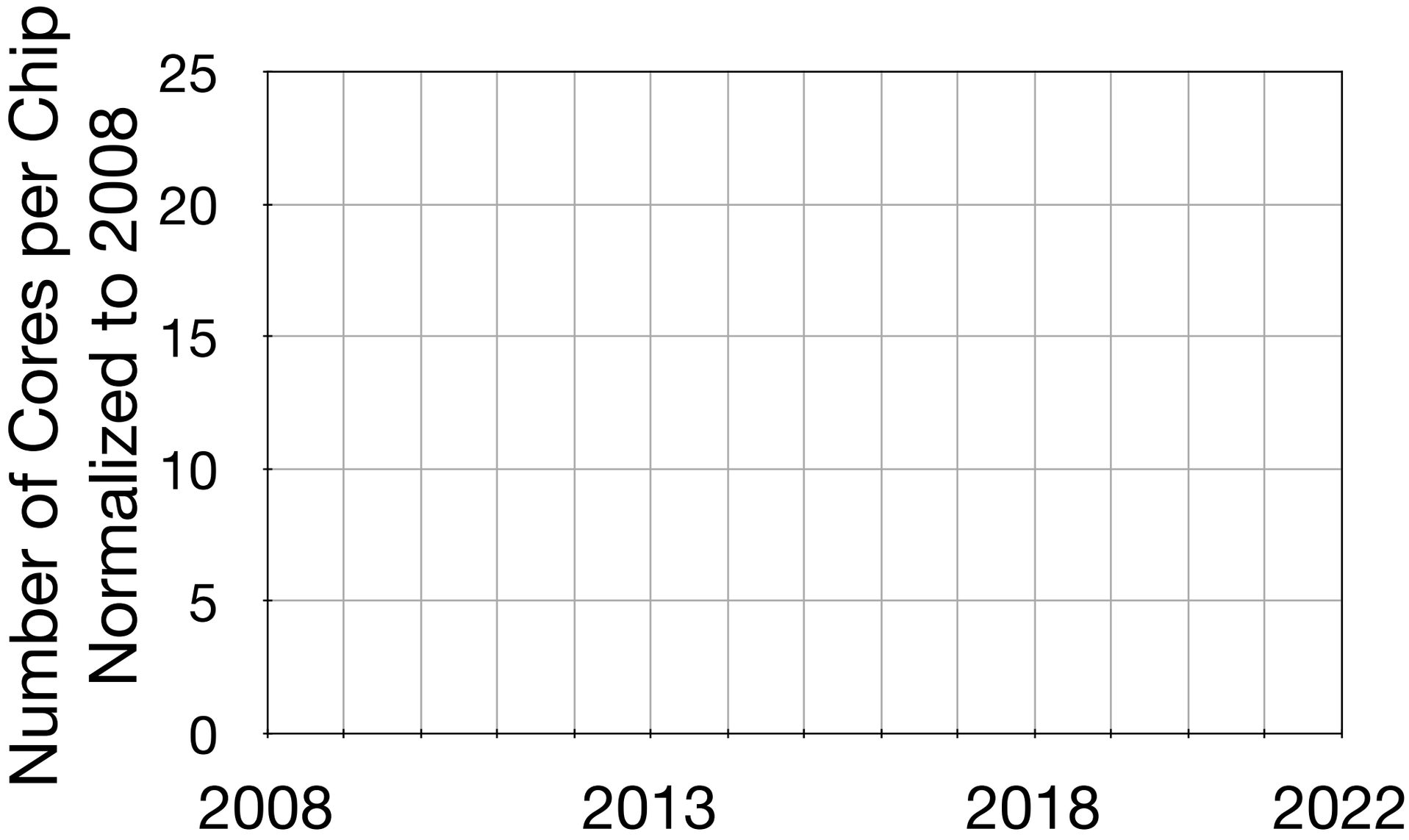


ITRS 2008

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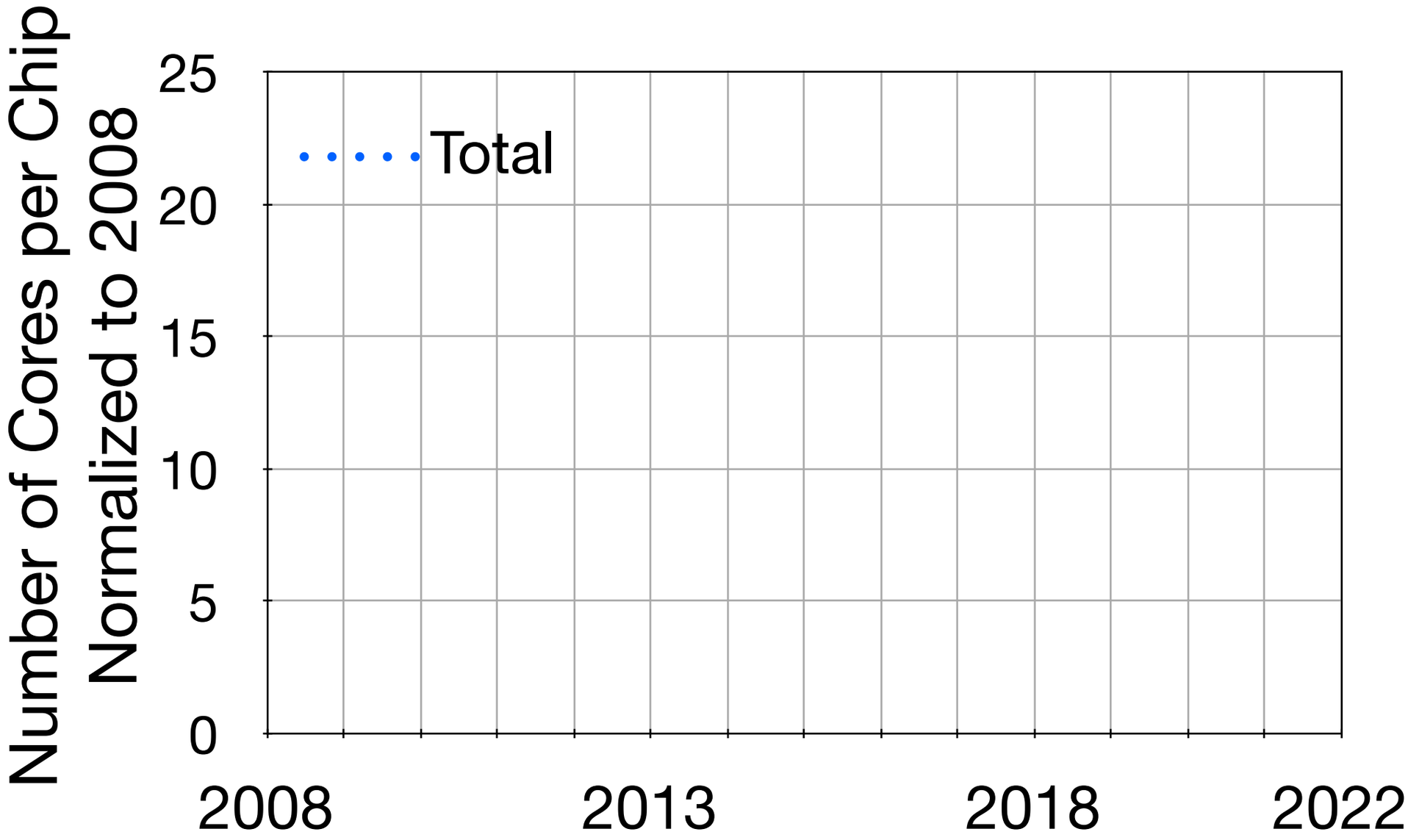


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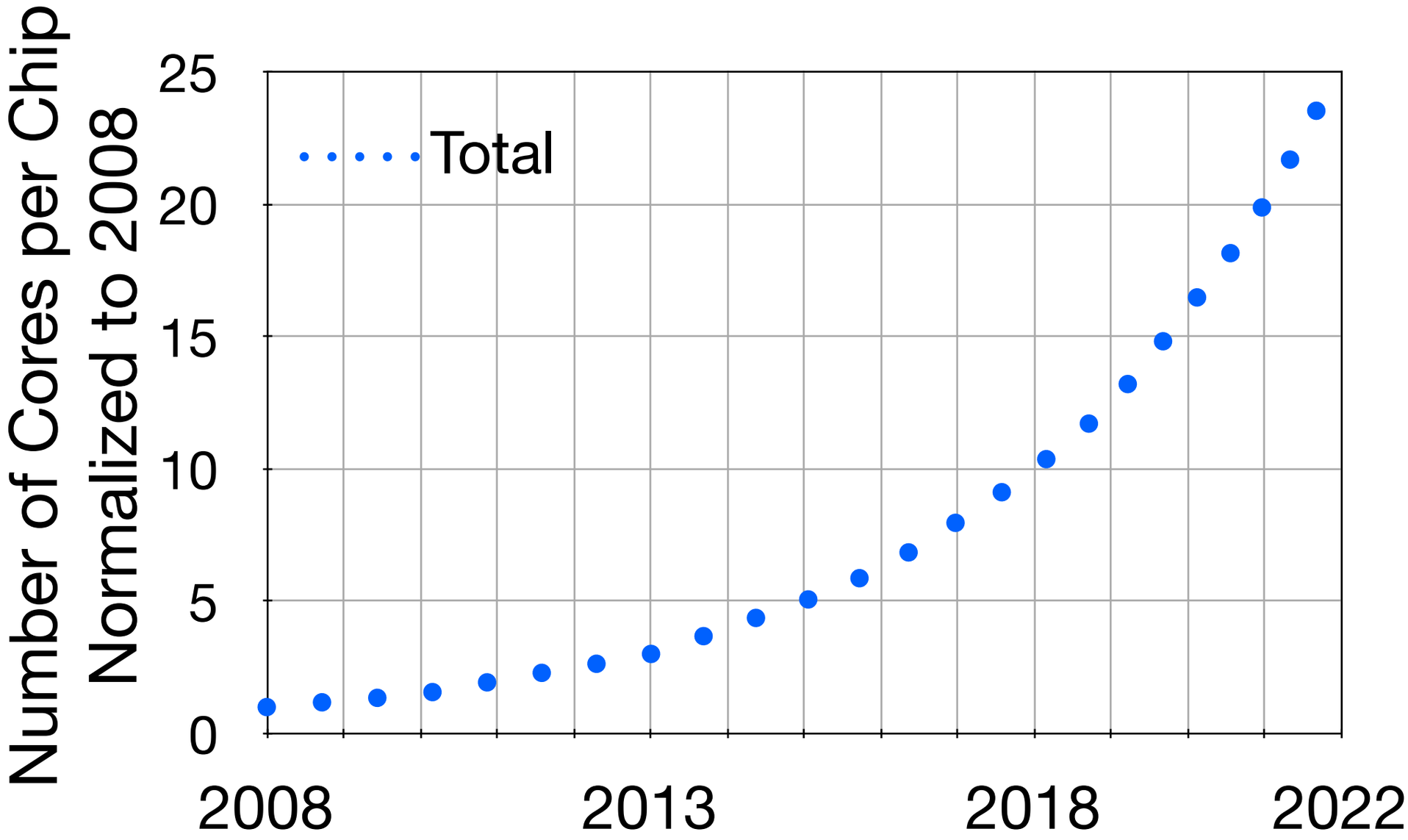


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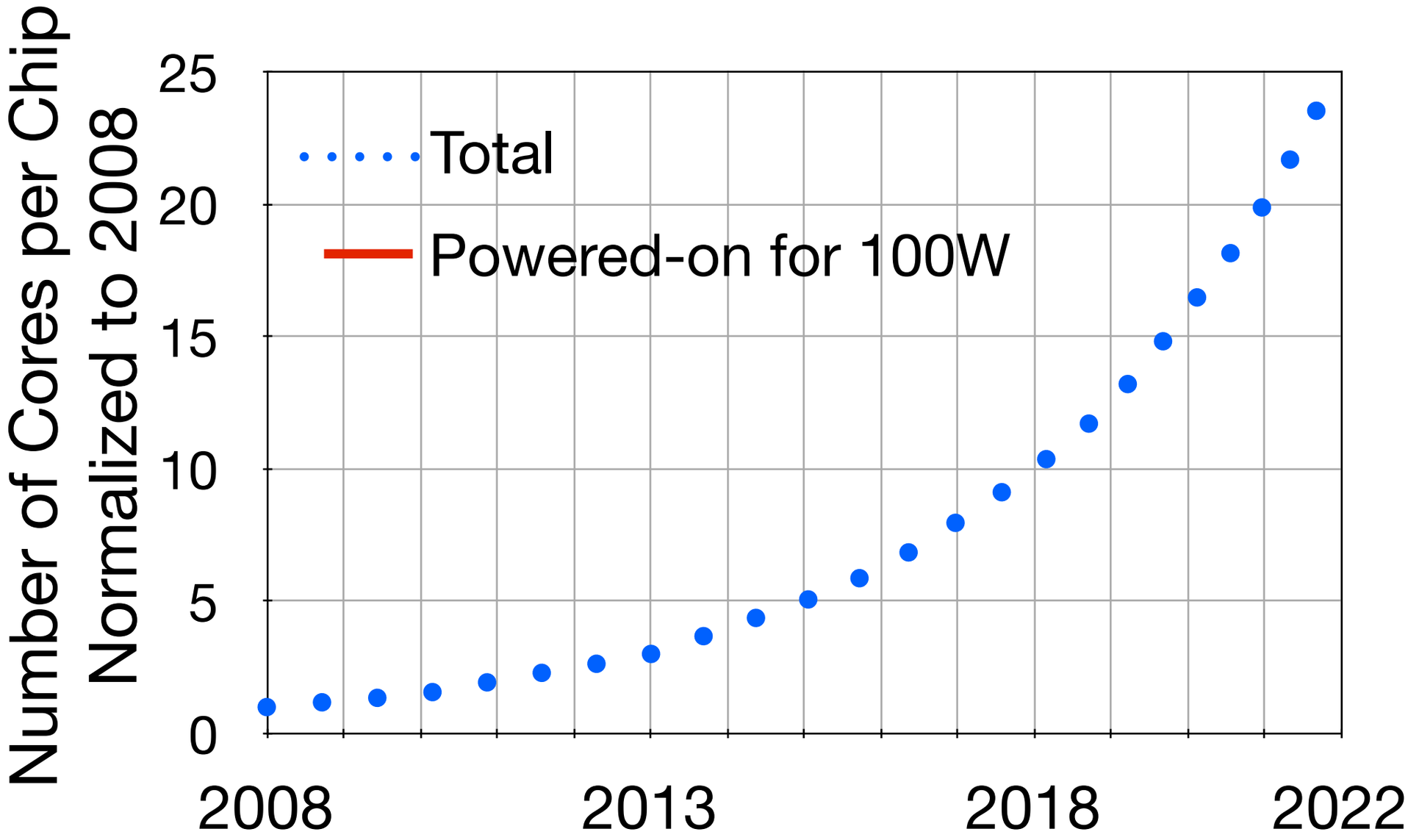


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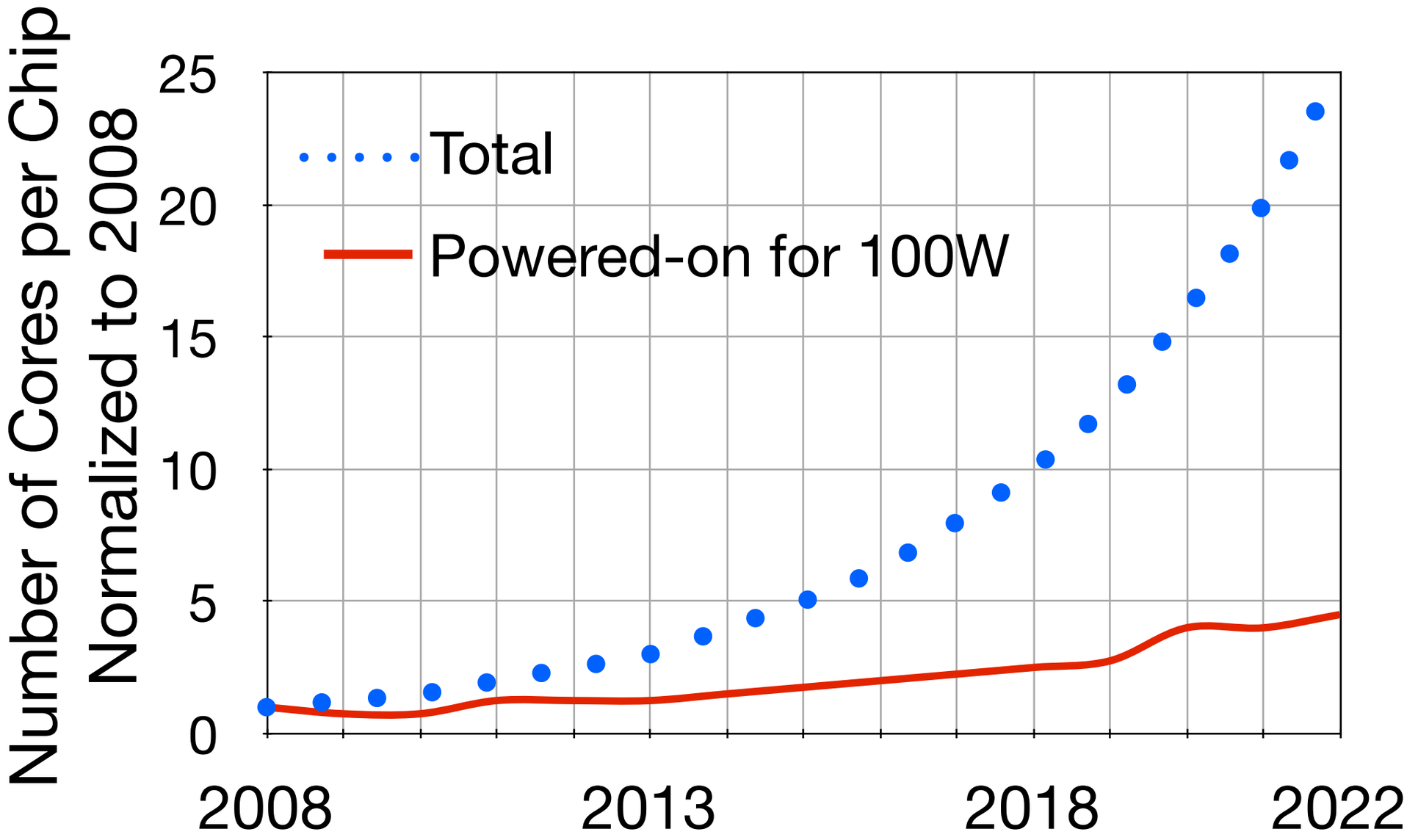


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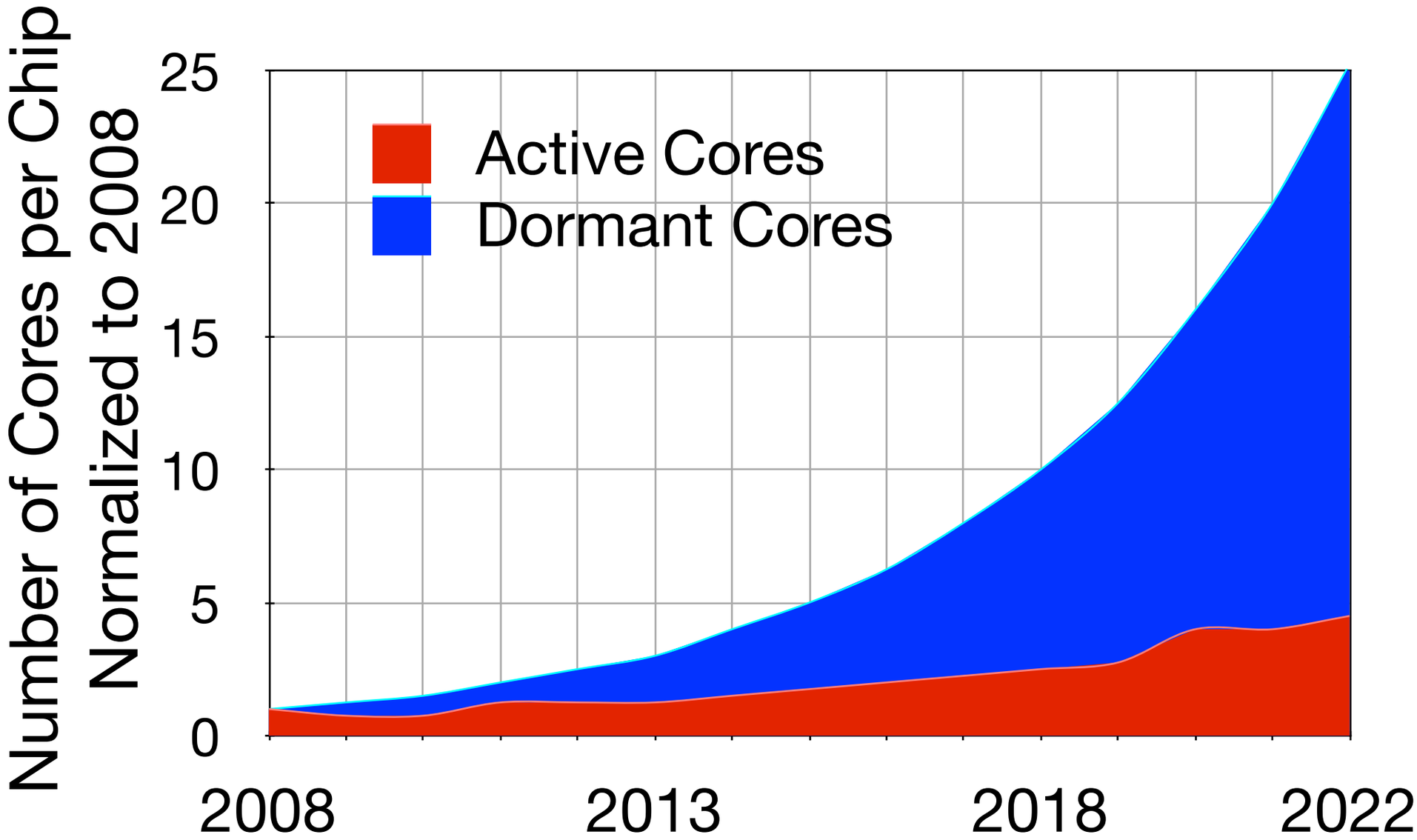


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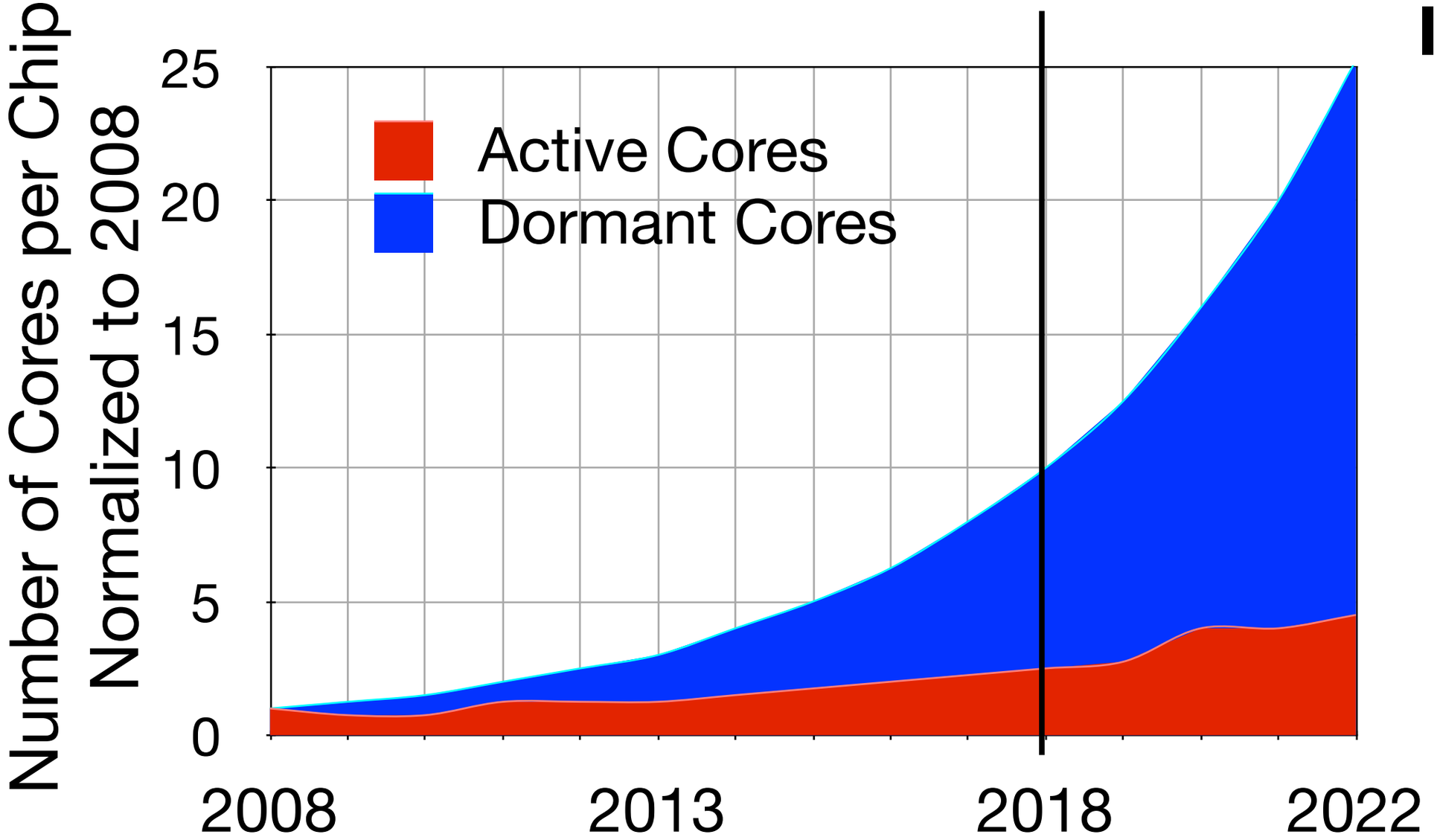


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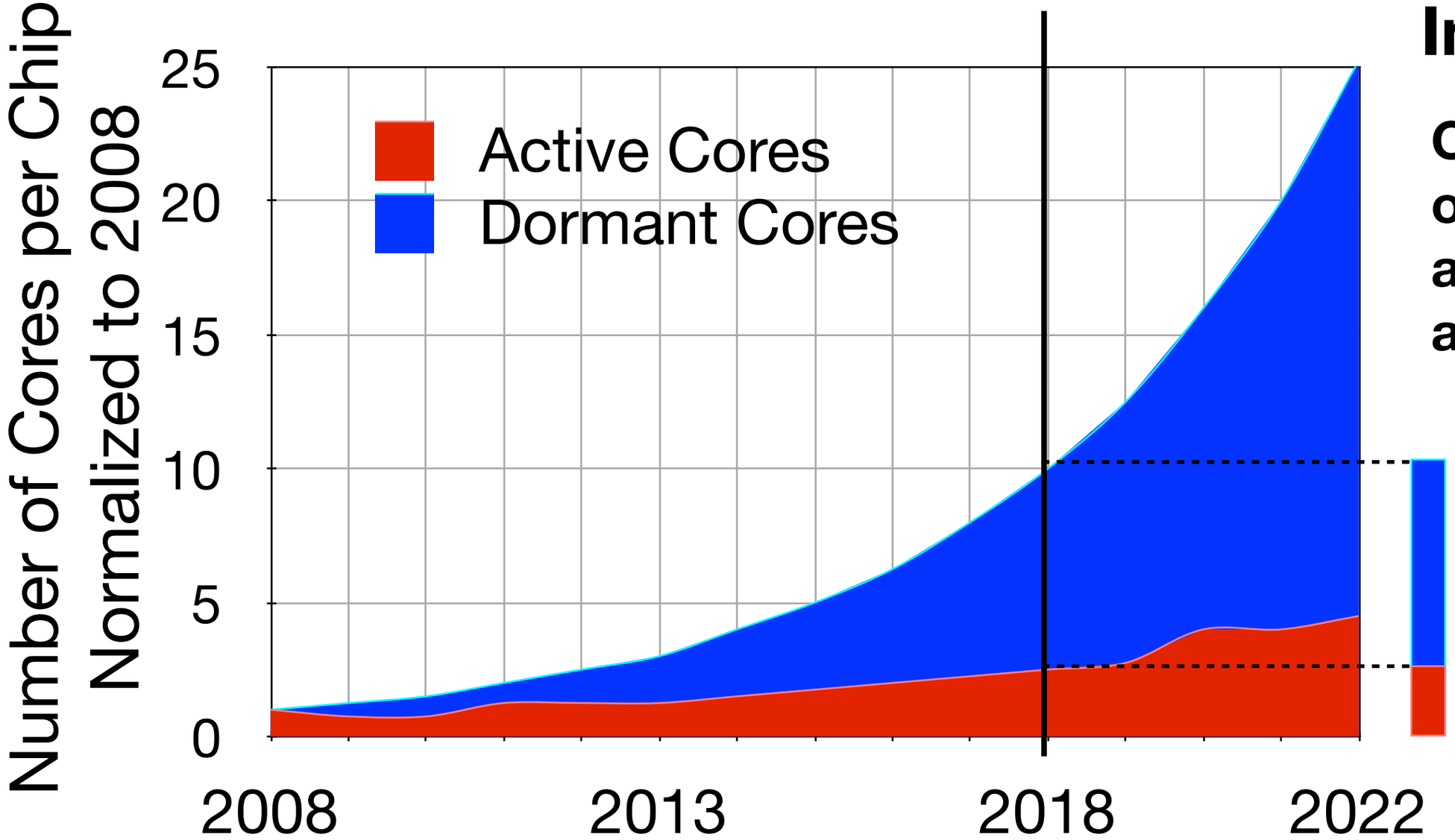


**In 9 years**

**Only ~25% of cores active at any time**

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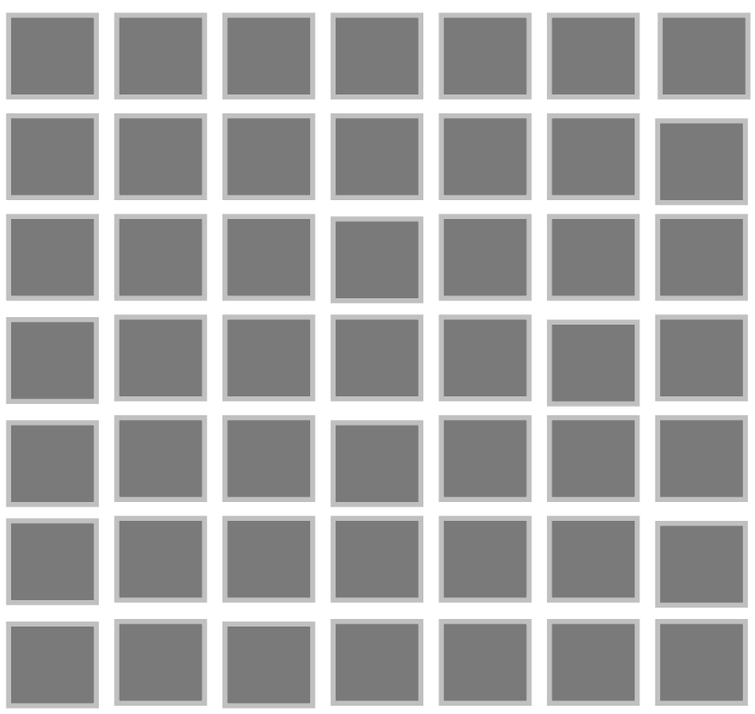

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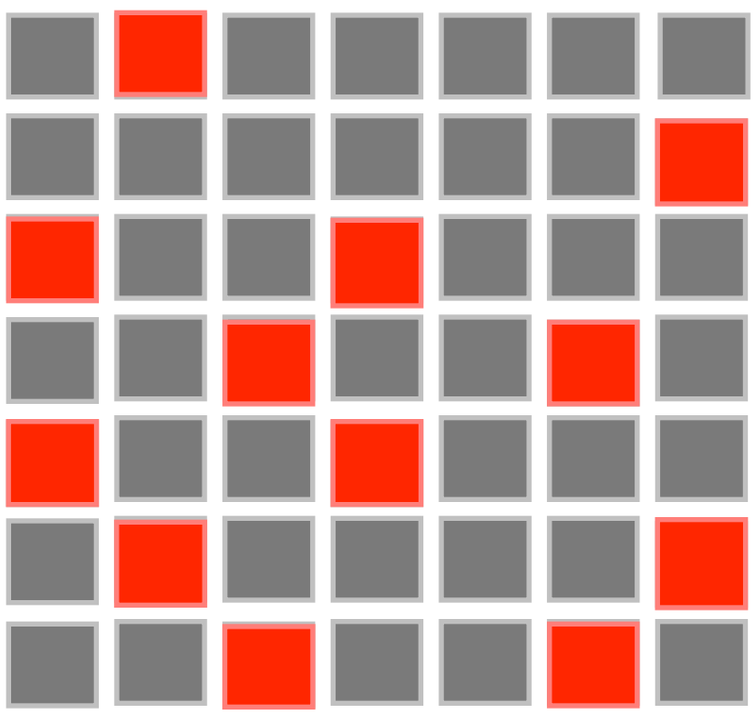

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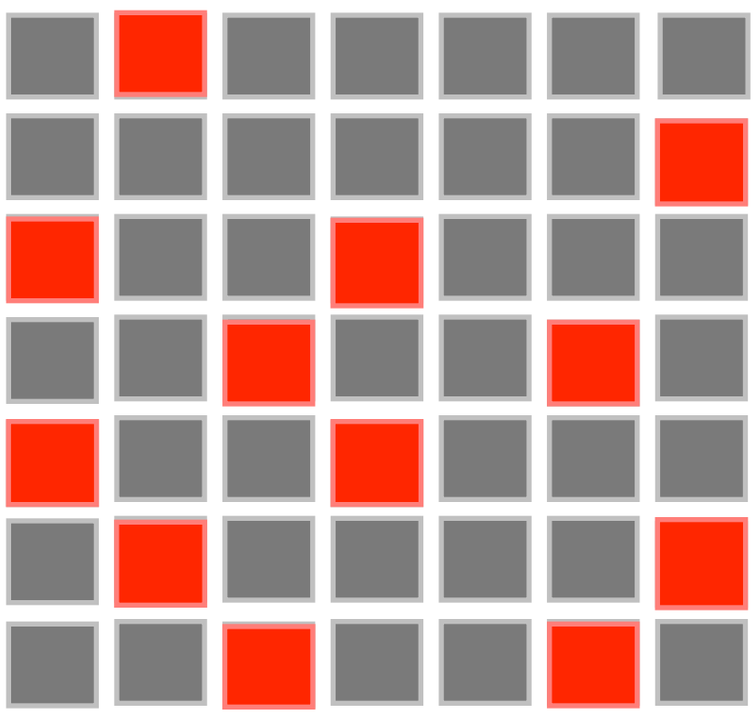

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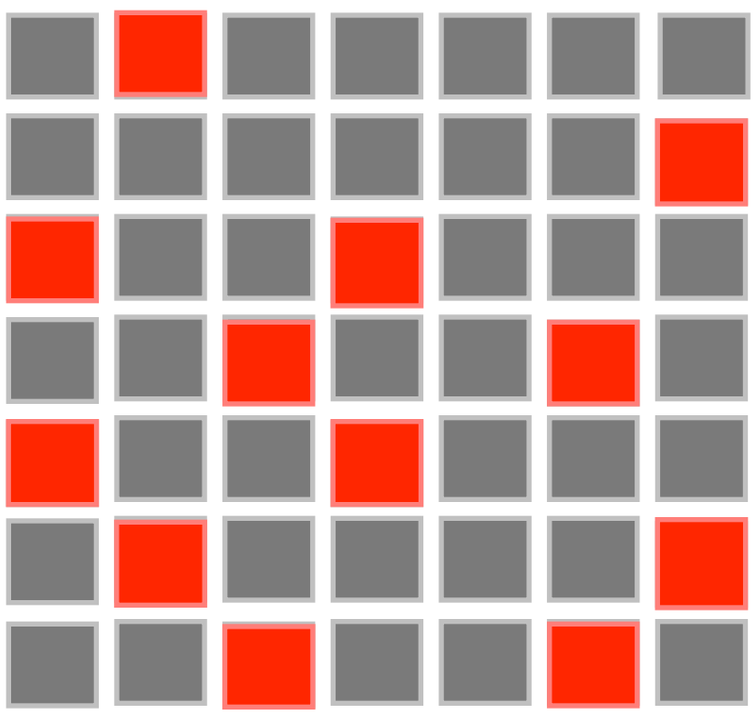

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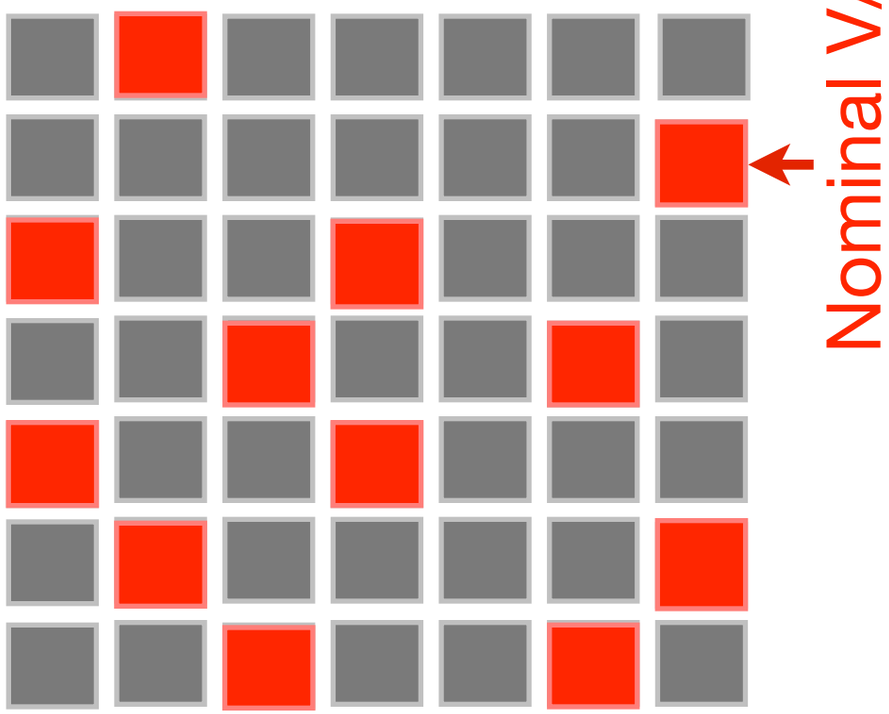


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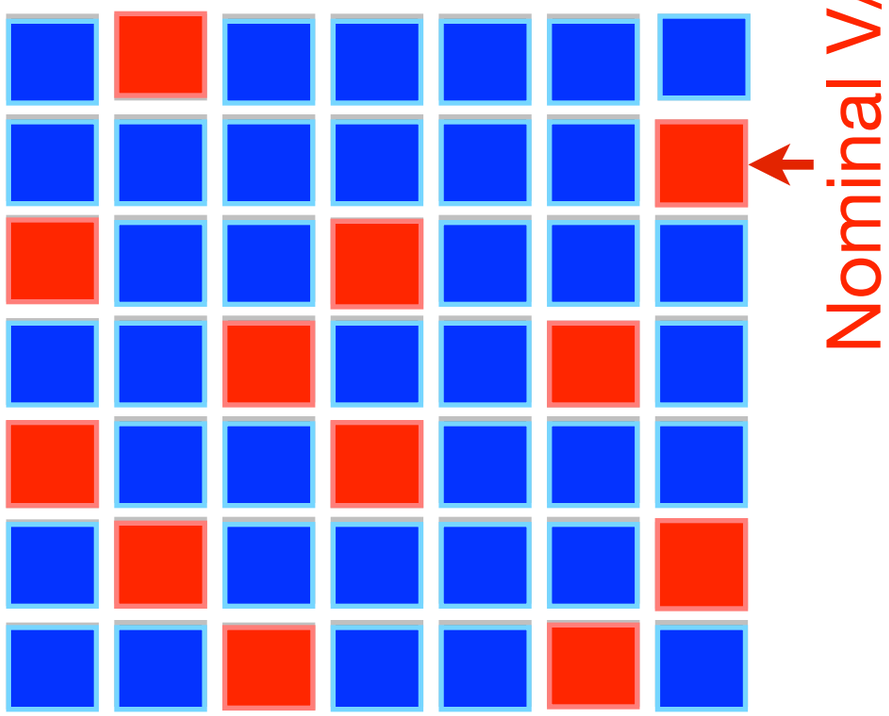


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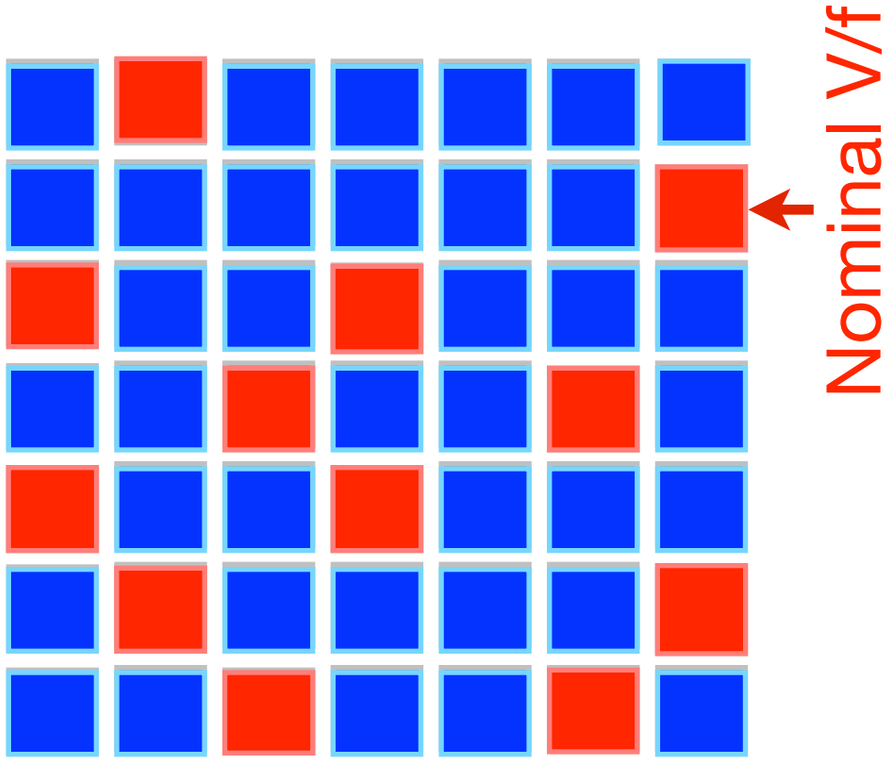


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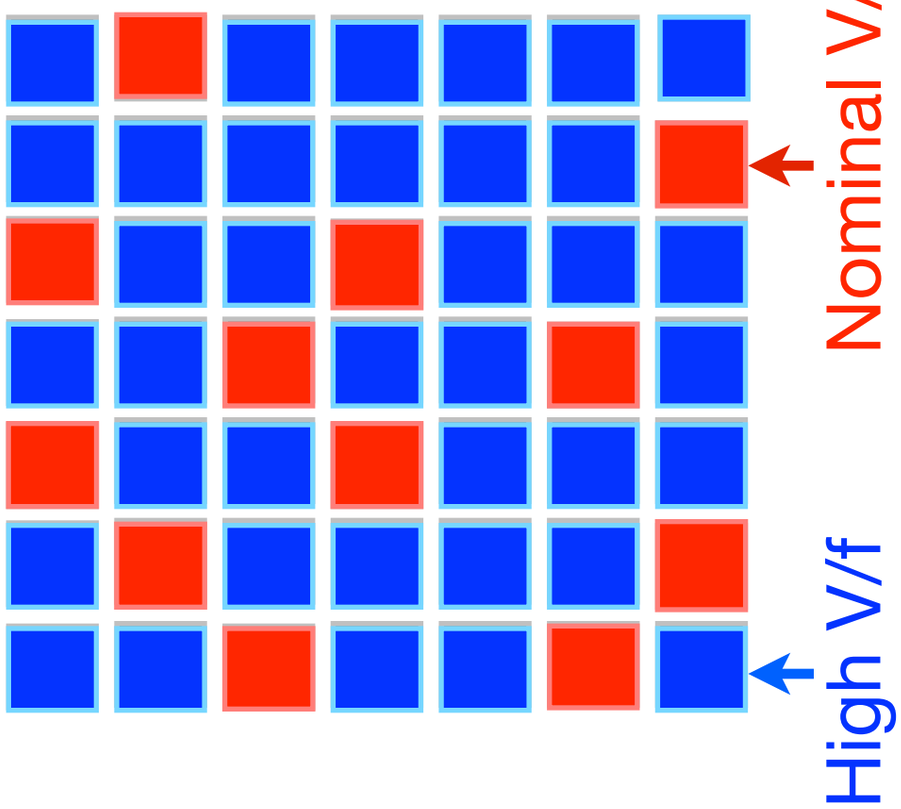


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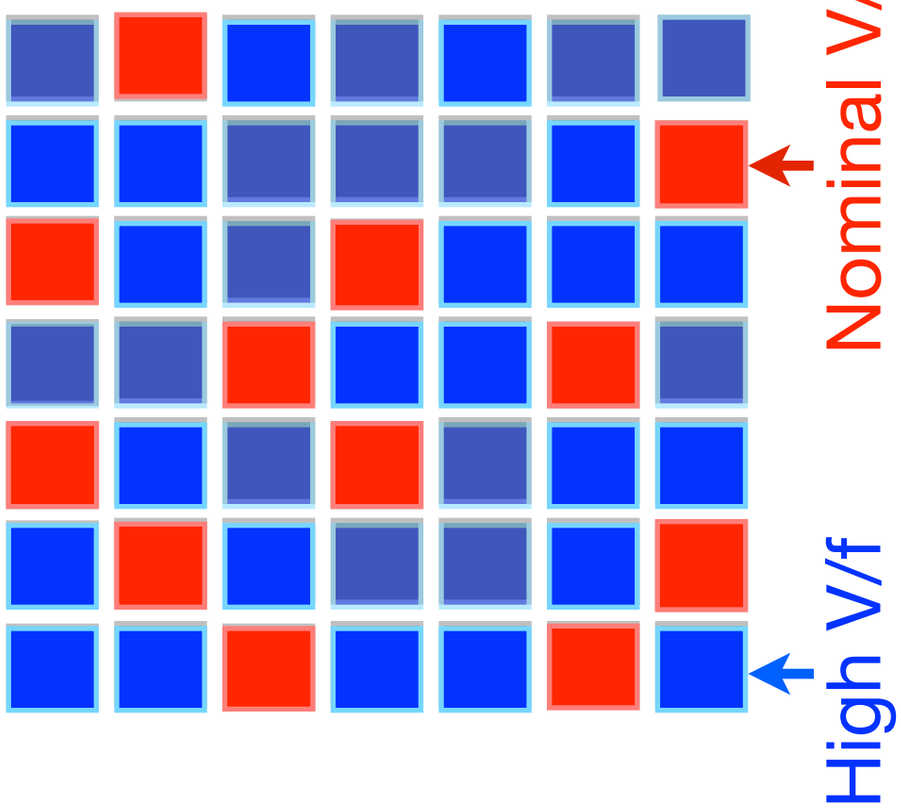


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  - Discarded early due to shorter service life (Popped like BubbleWrap)

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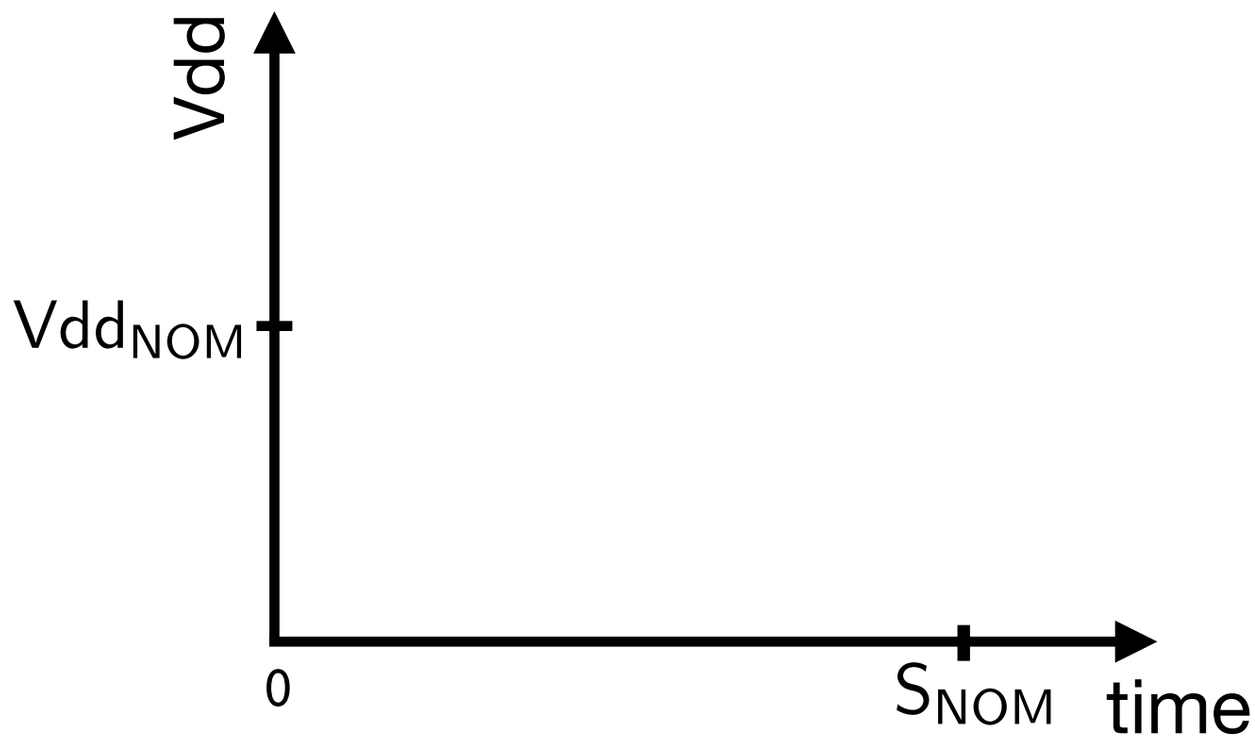
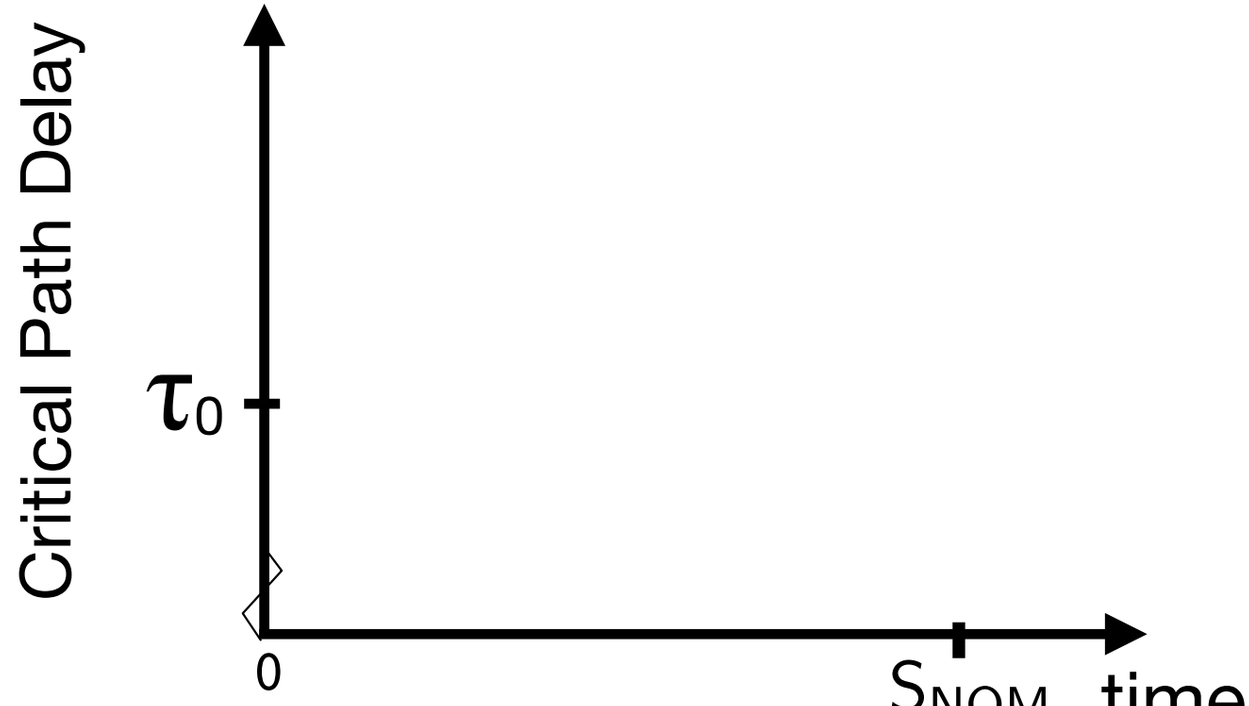
- Aging rate: Exponential dependence on Vdd and T

# Aging-induced Degradation



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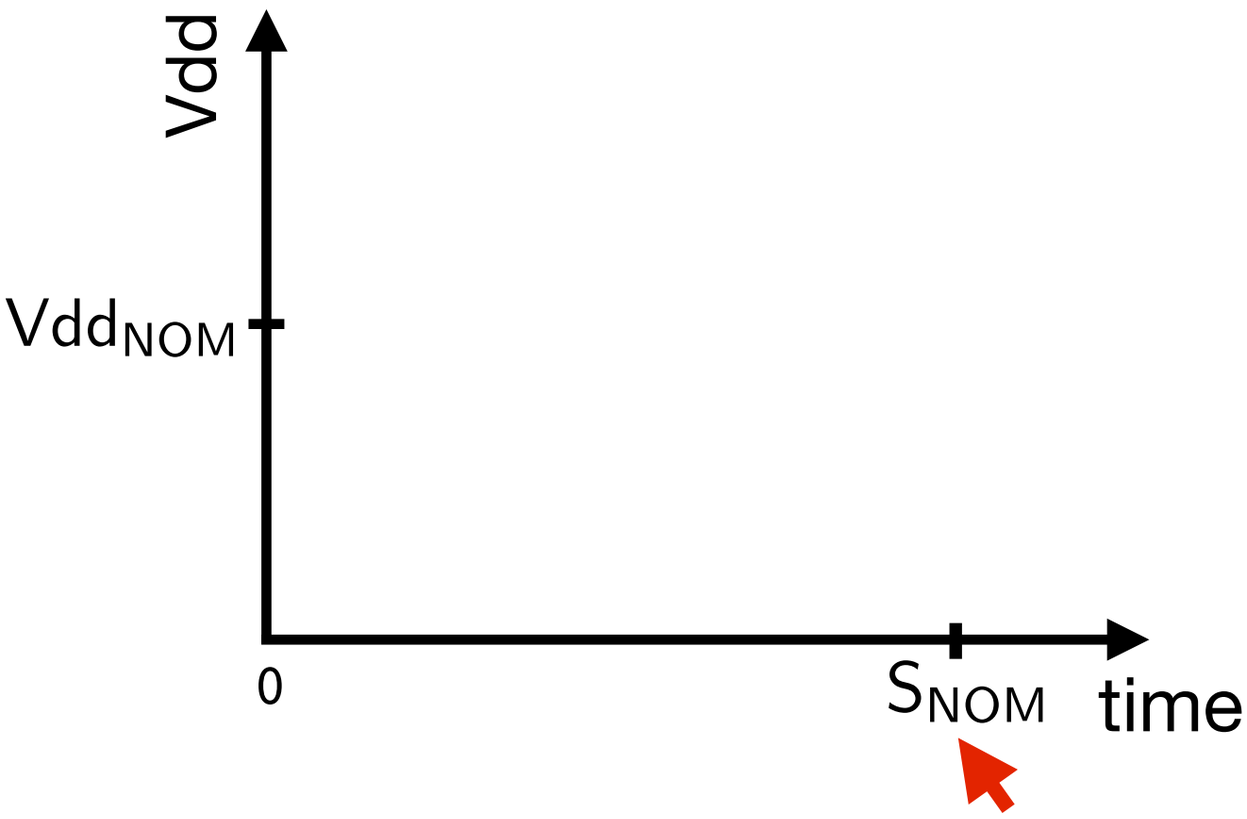


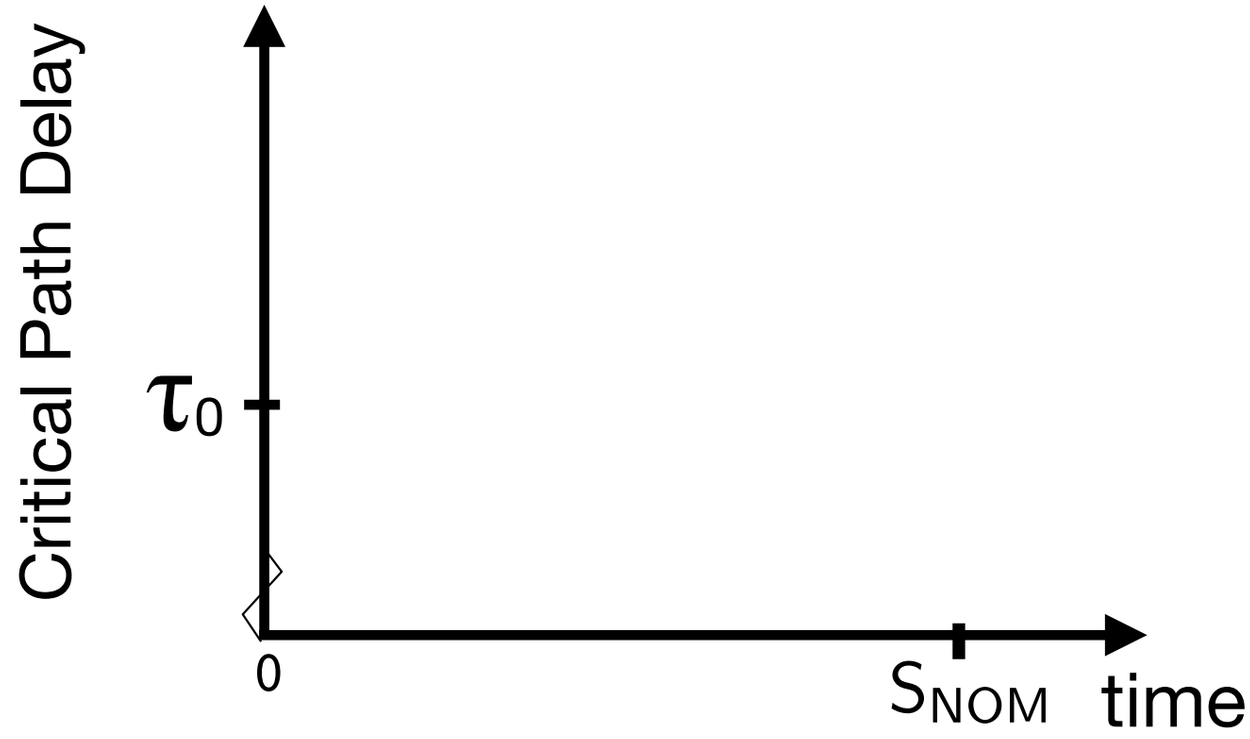

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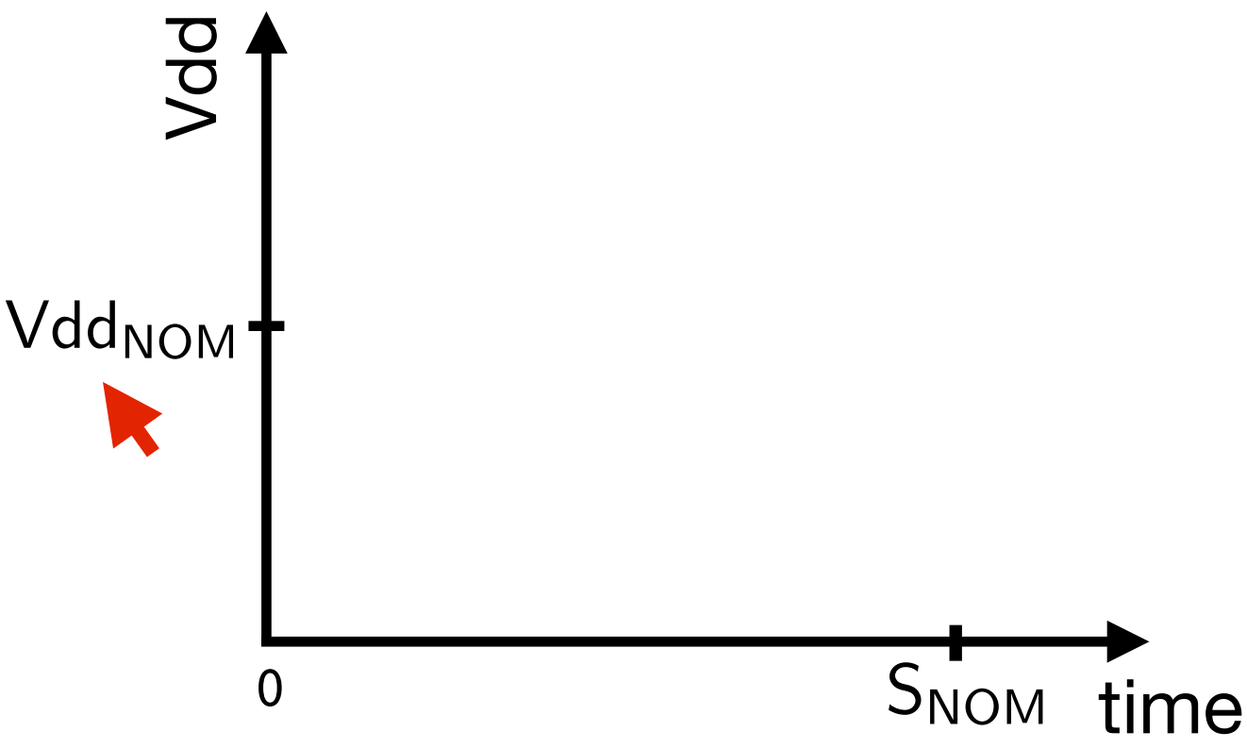


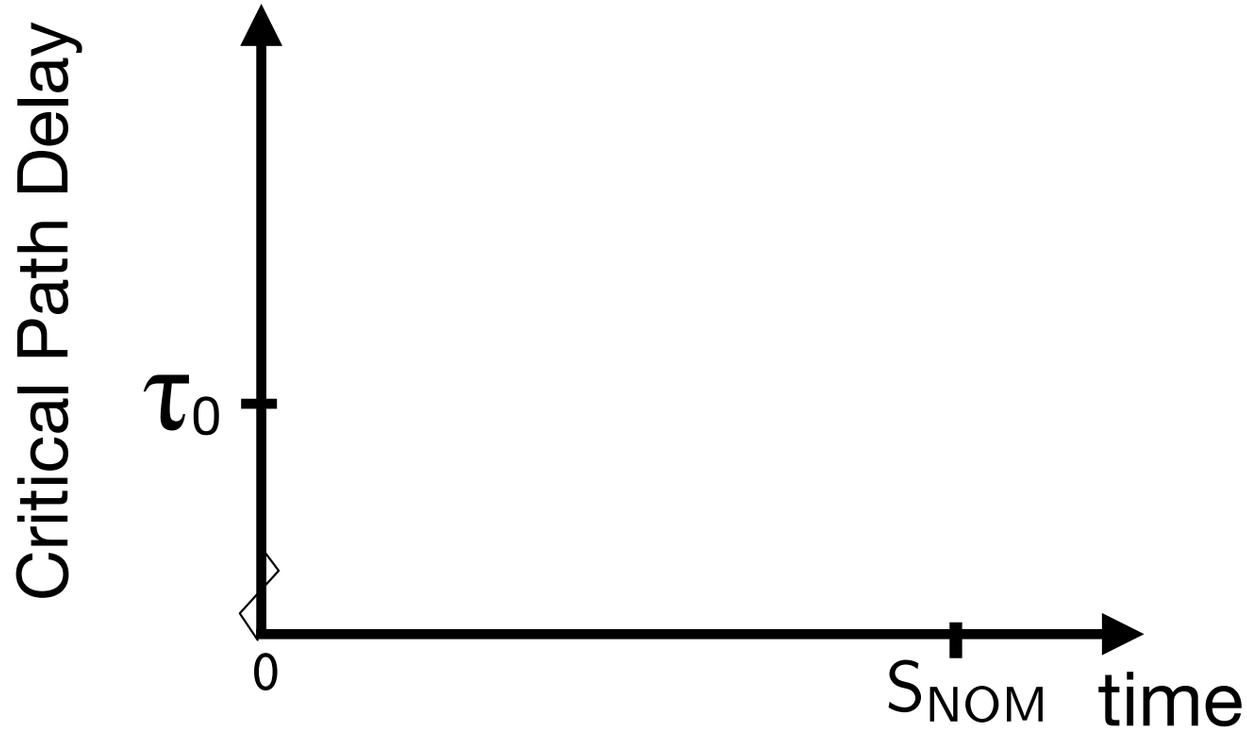

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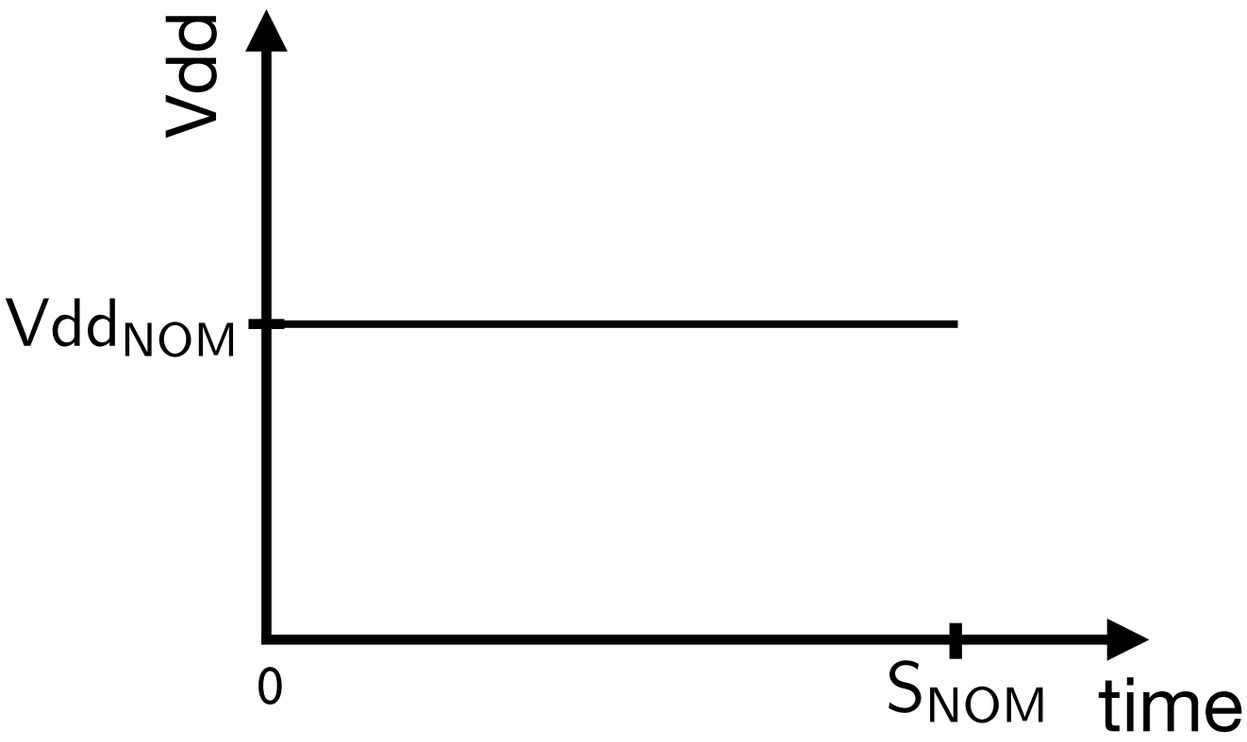


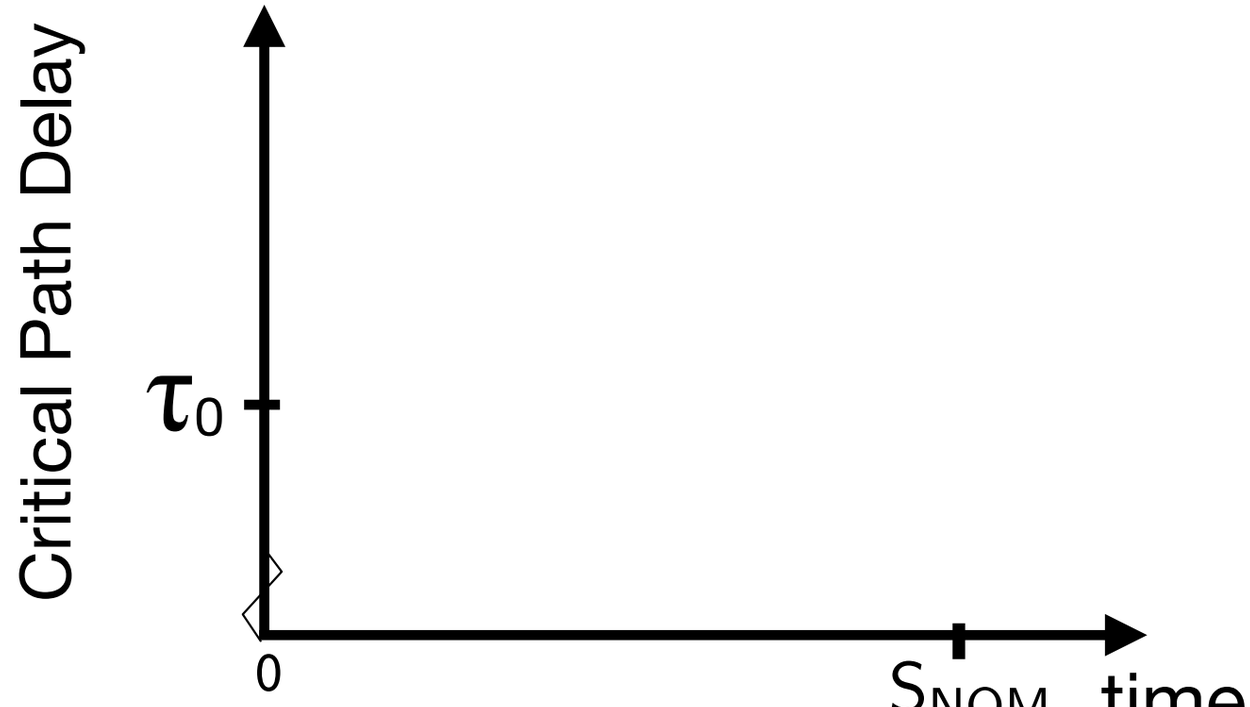

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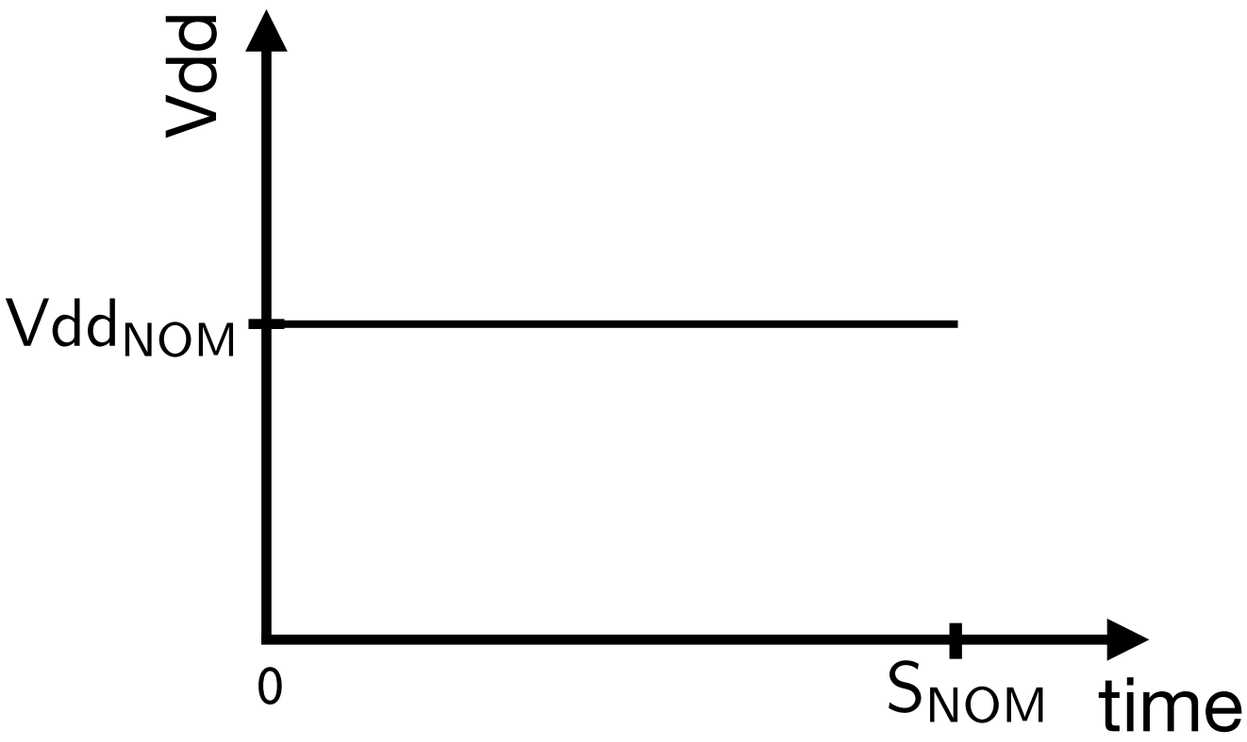


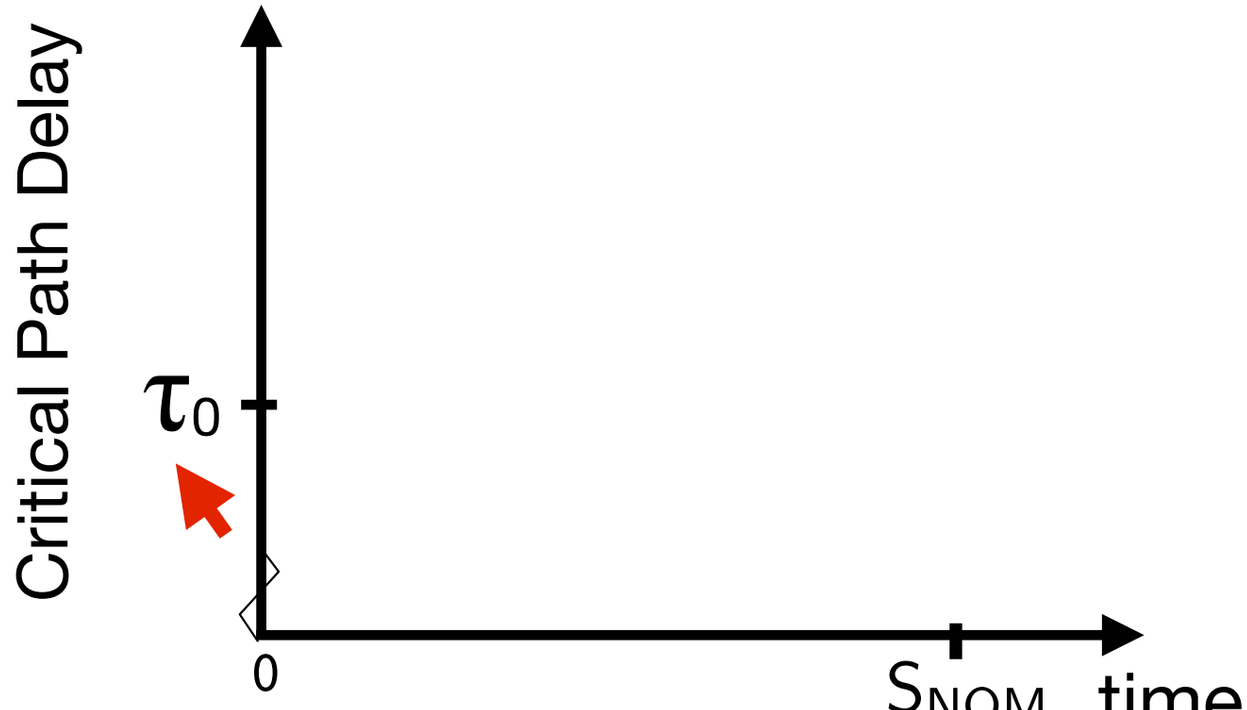

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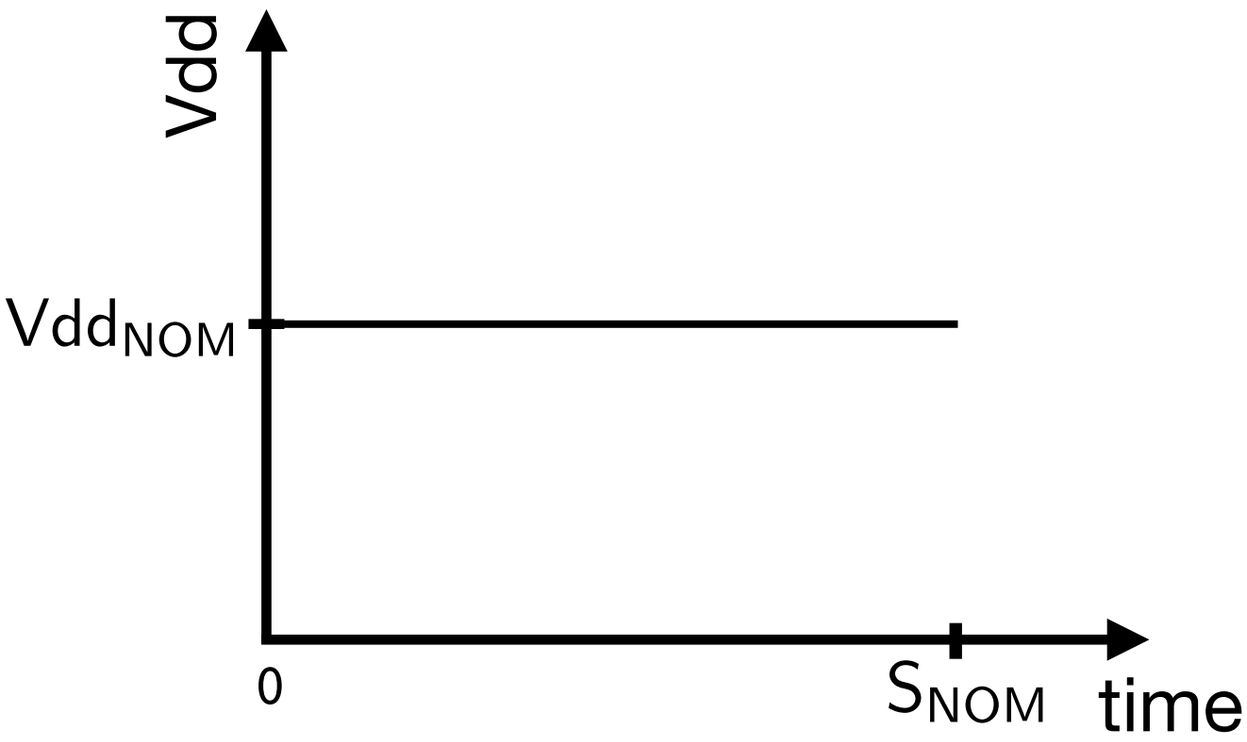


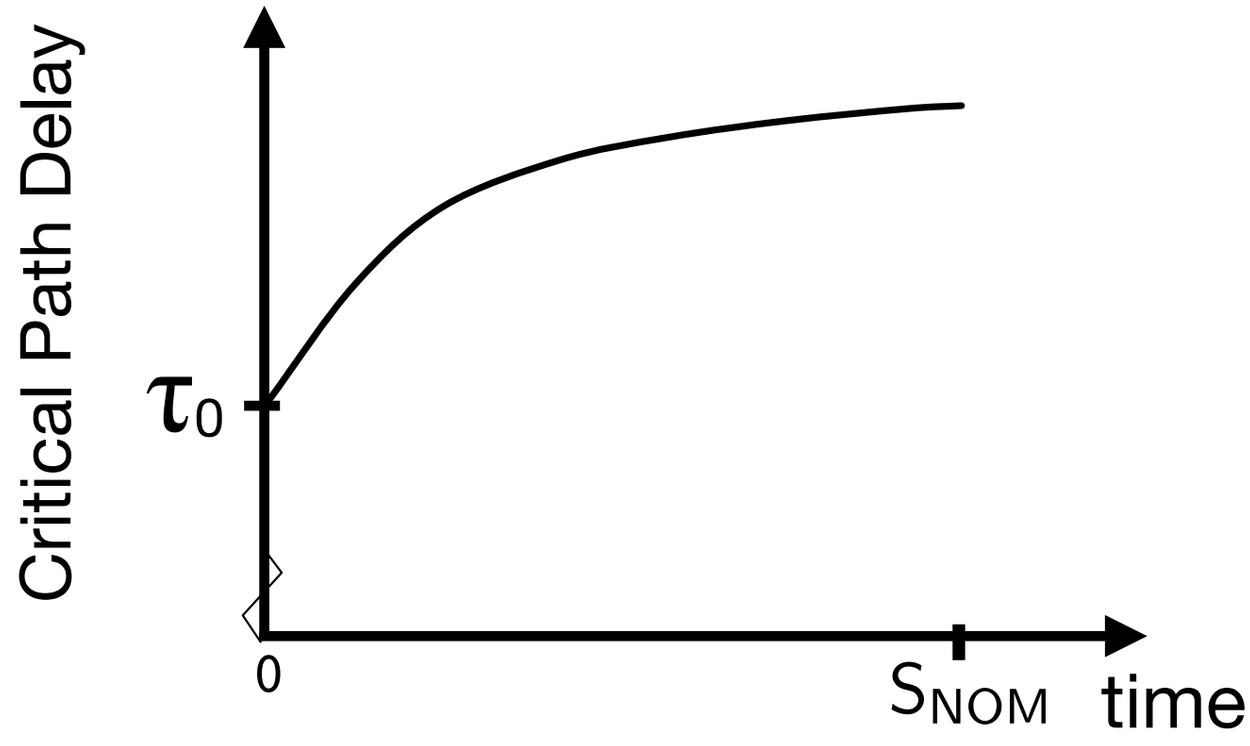


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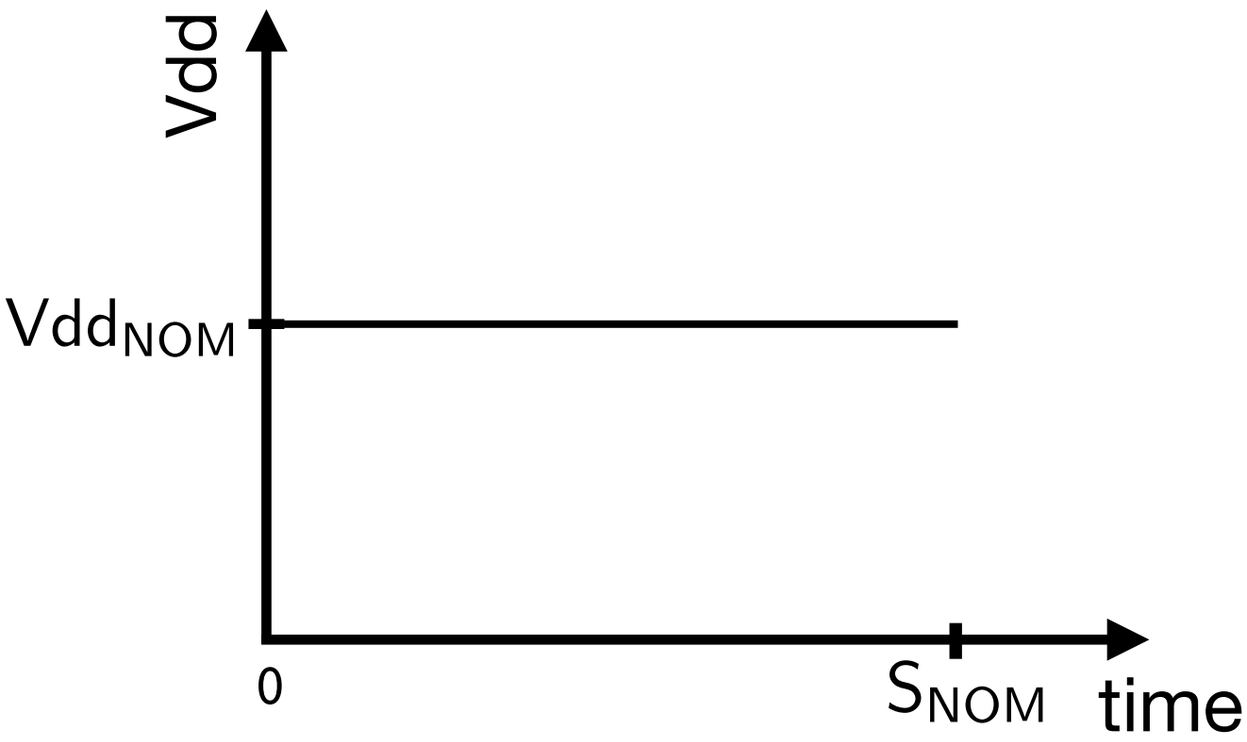


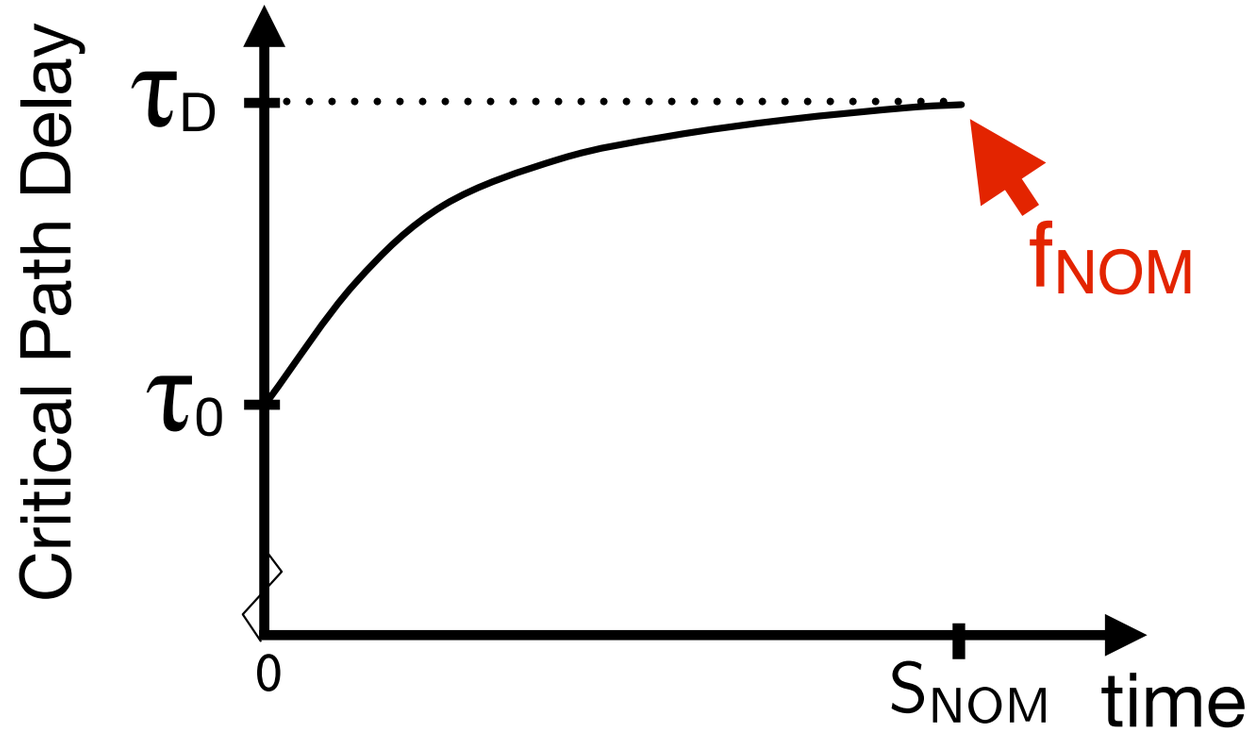


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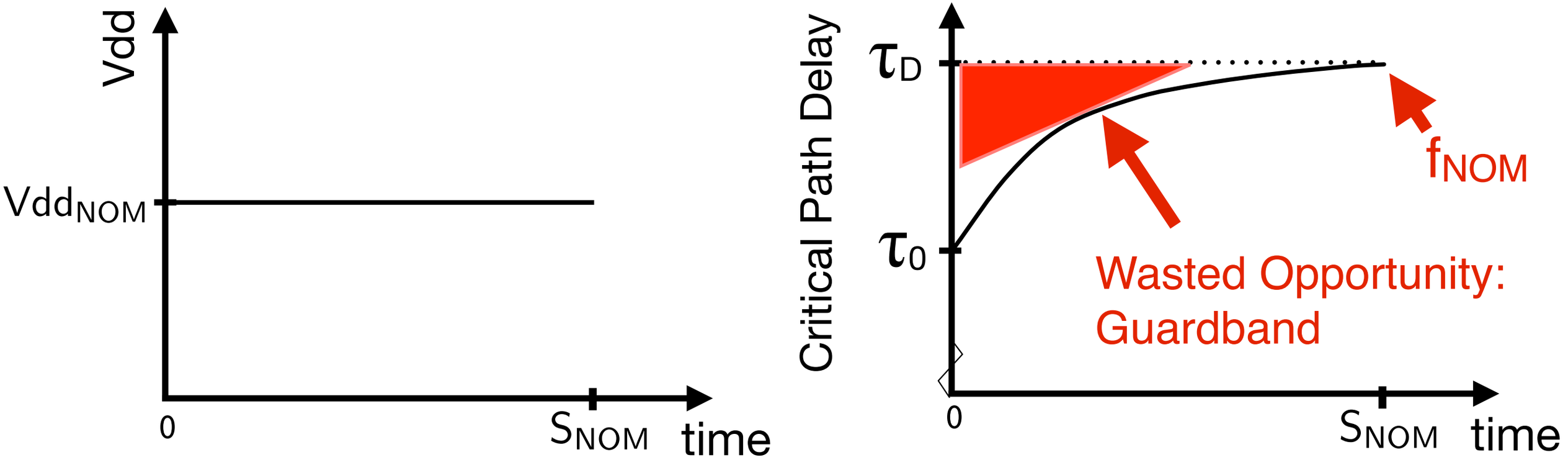


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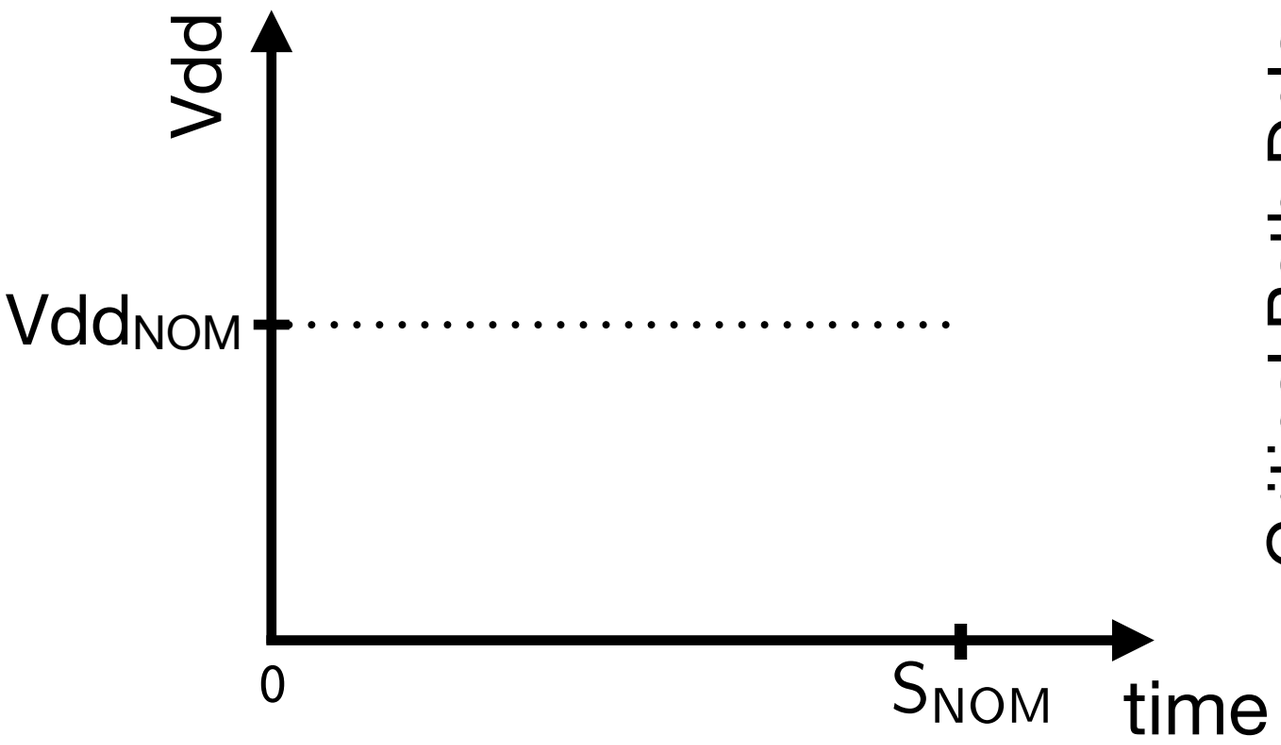
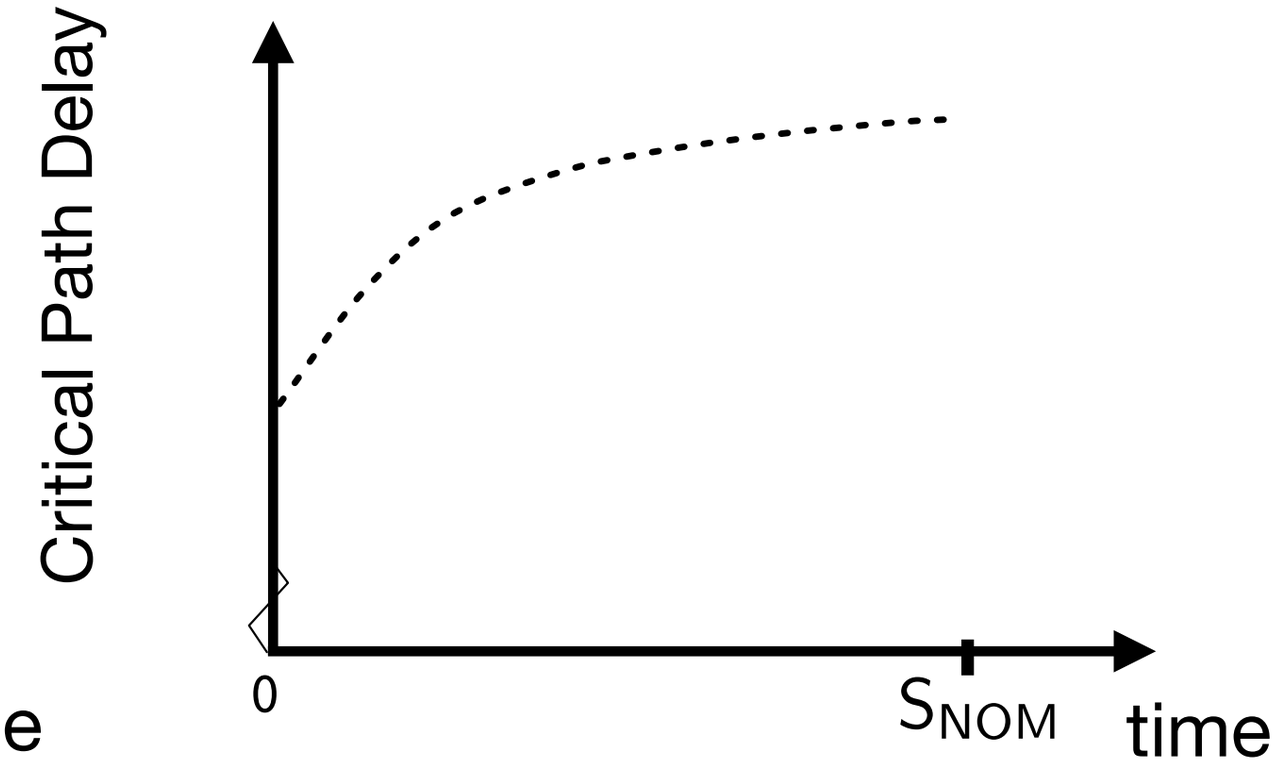
# Impact of Operation at Higher V/f on Aging



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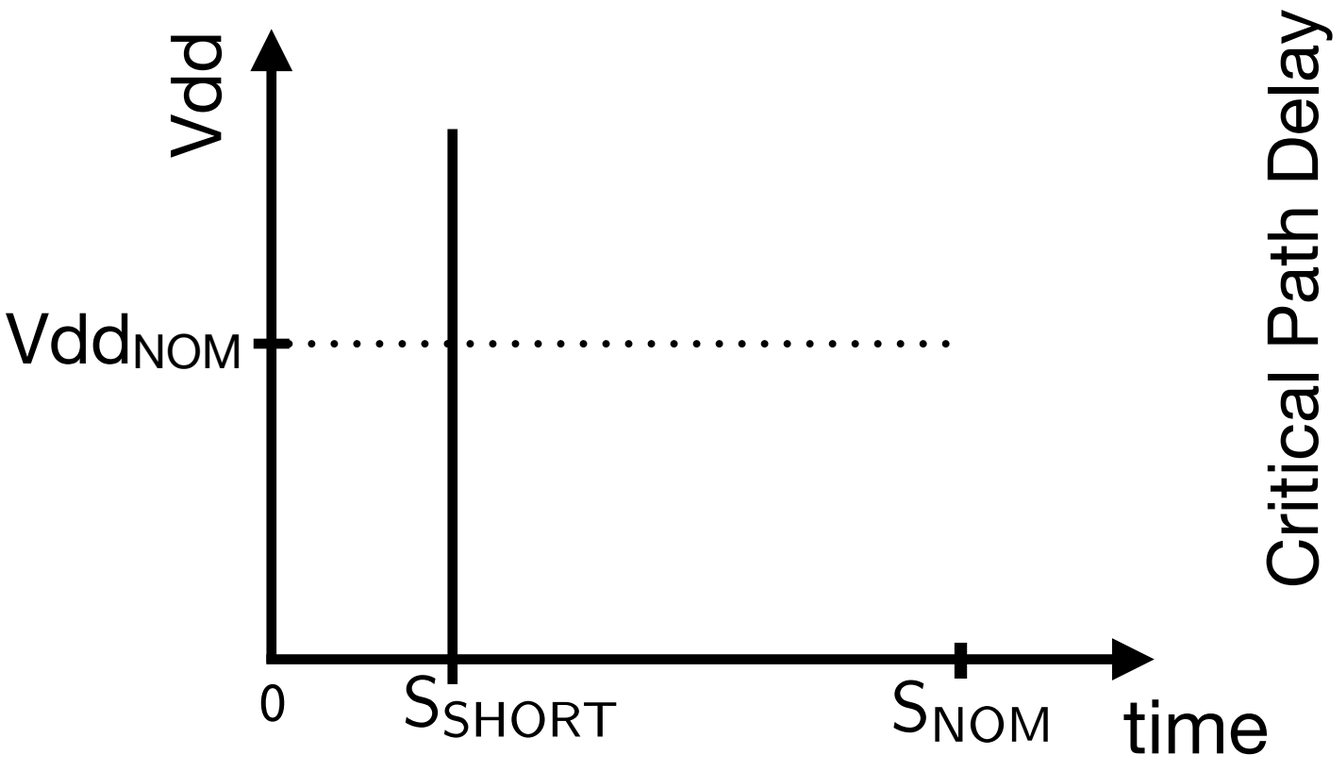


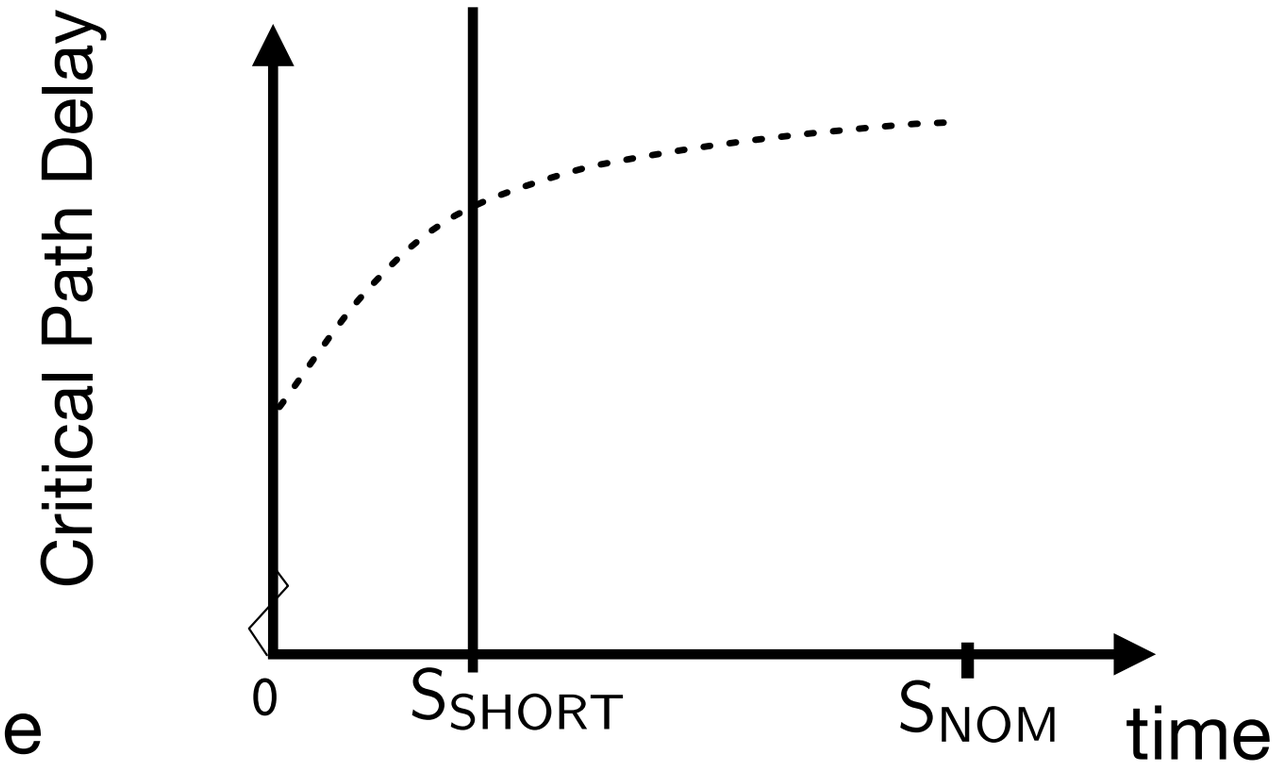

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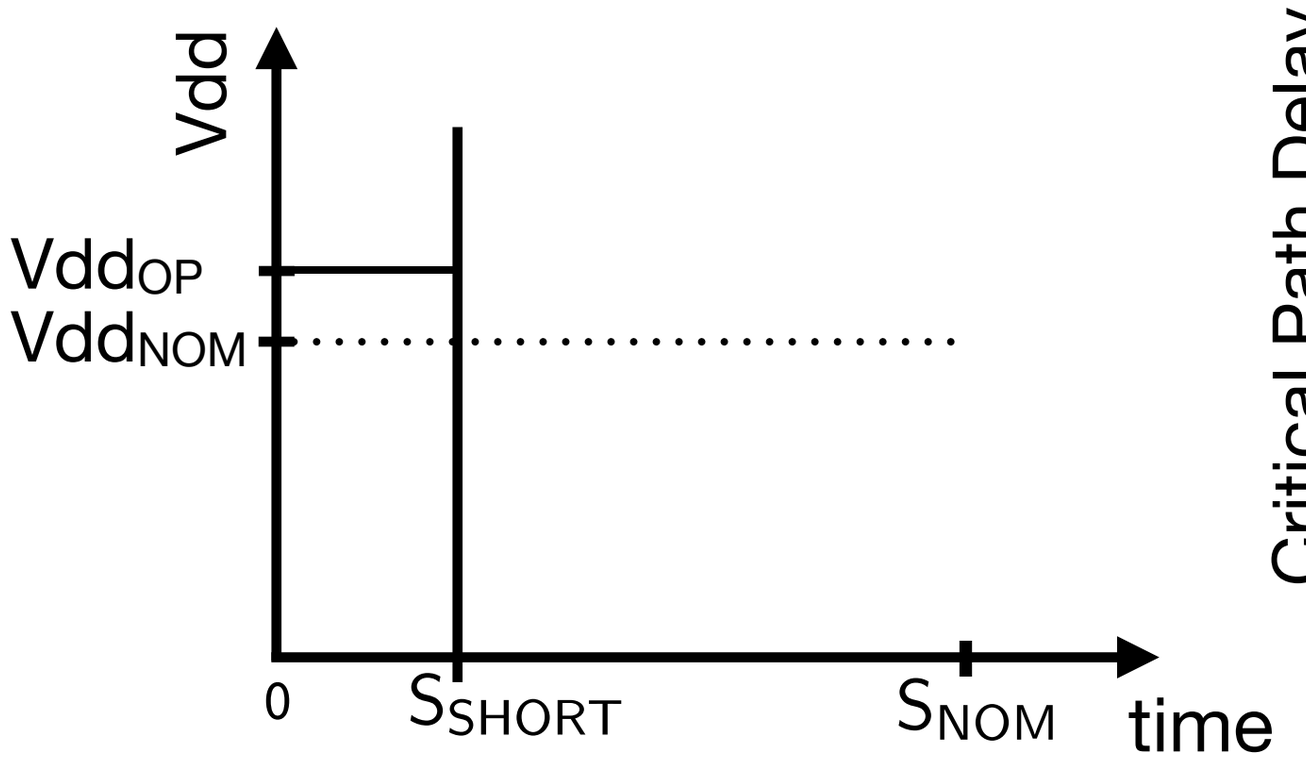


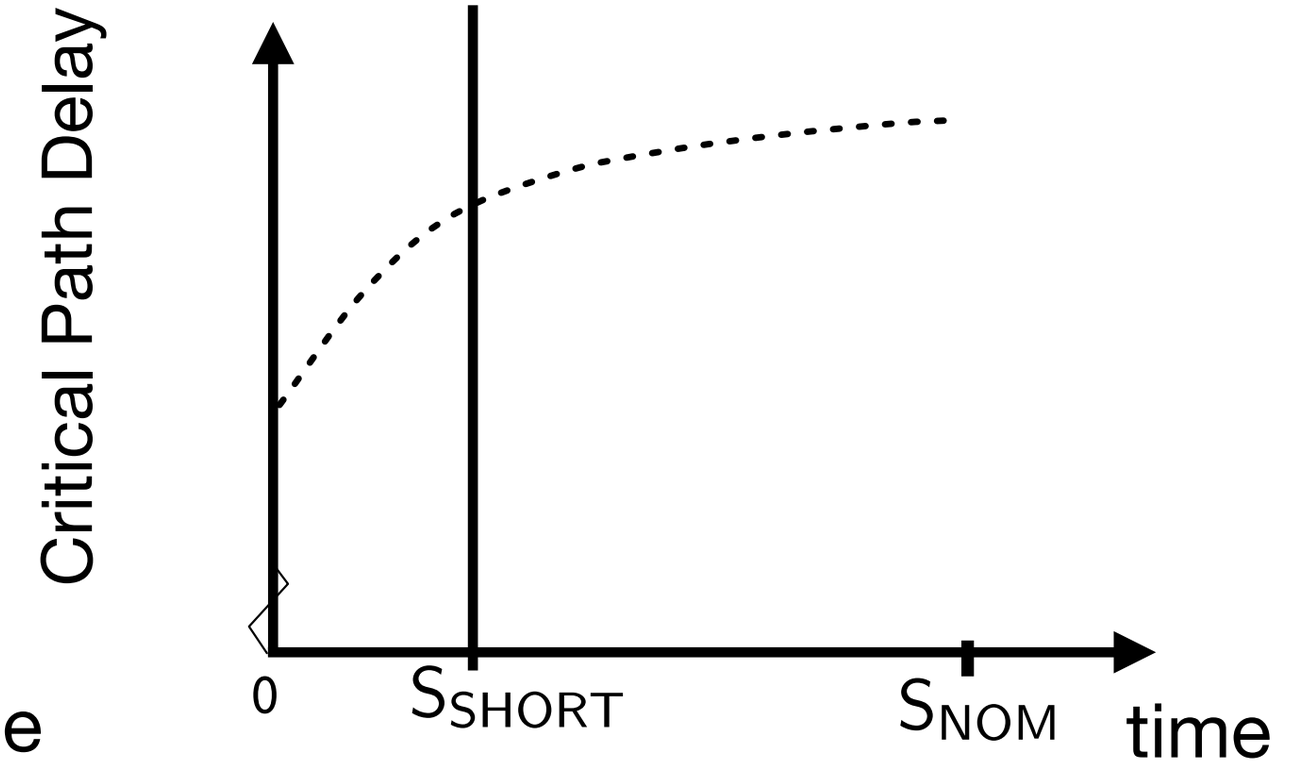


- Higher Vdd: $Vdd_{OP}$ >> $Vdd_{NOM}$

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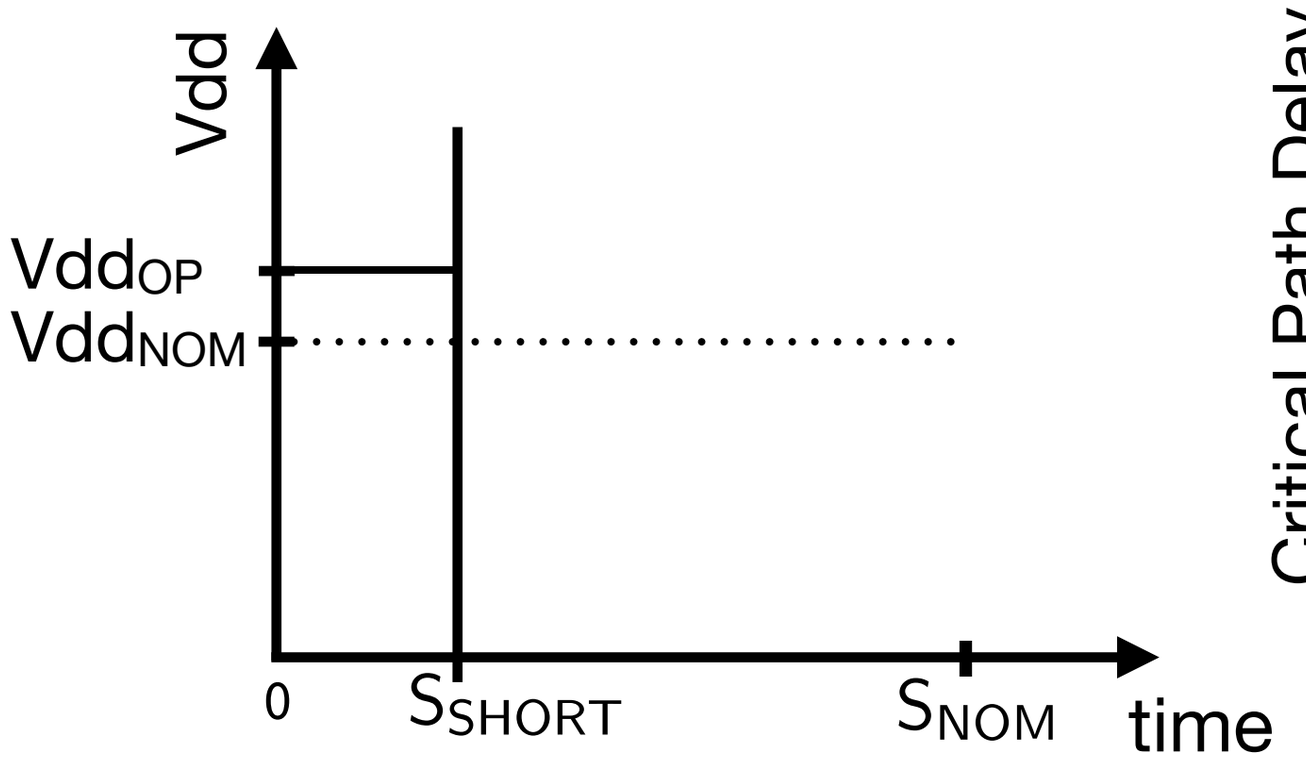


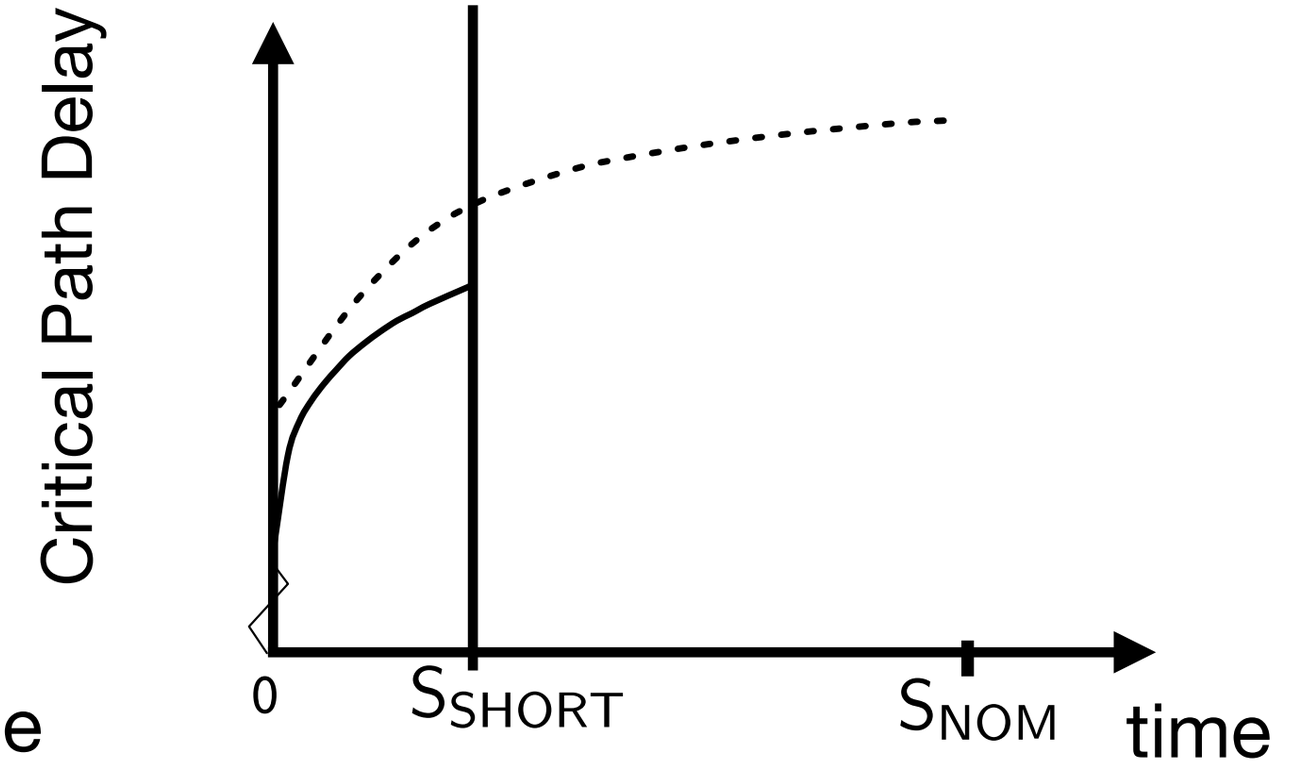


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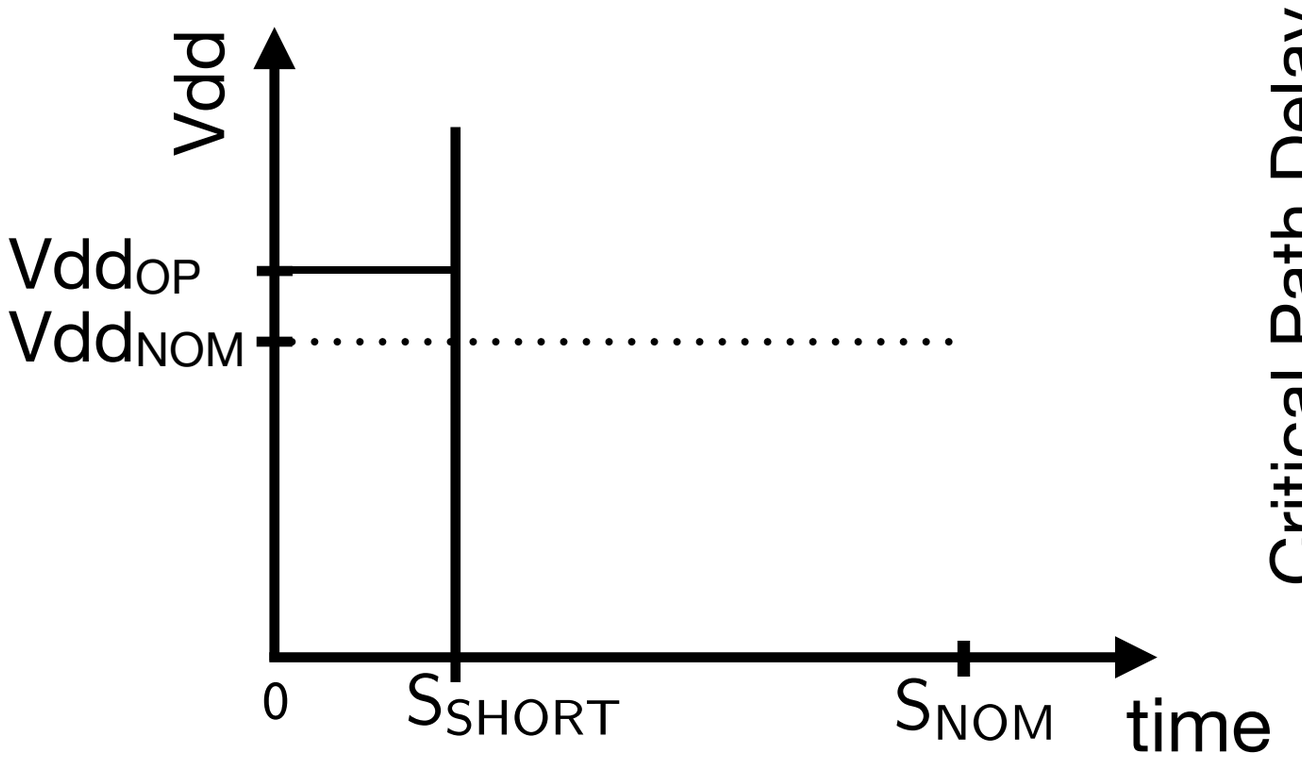
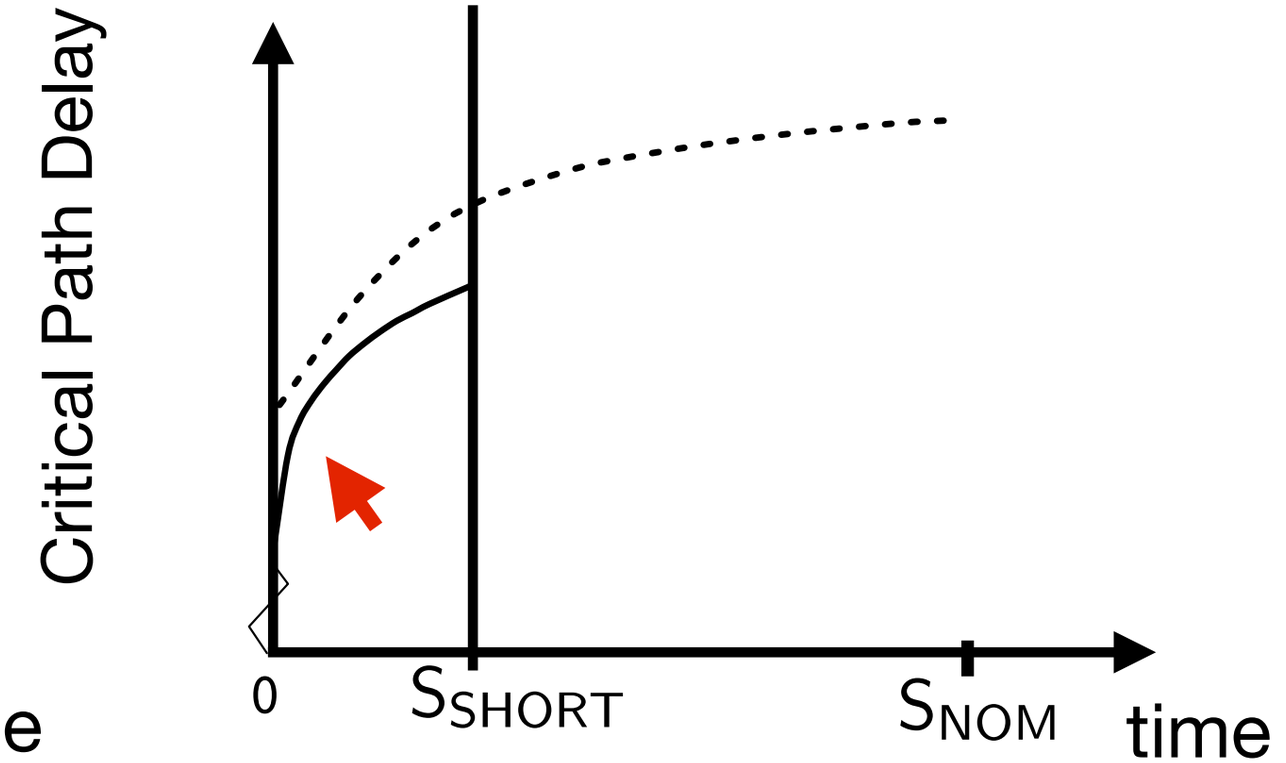
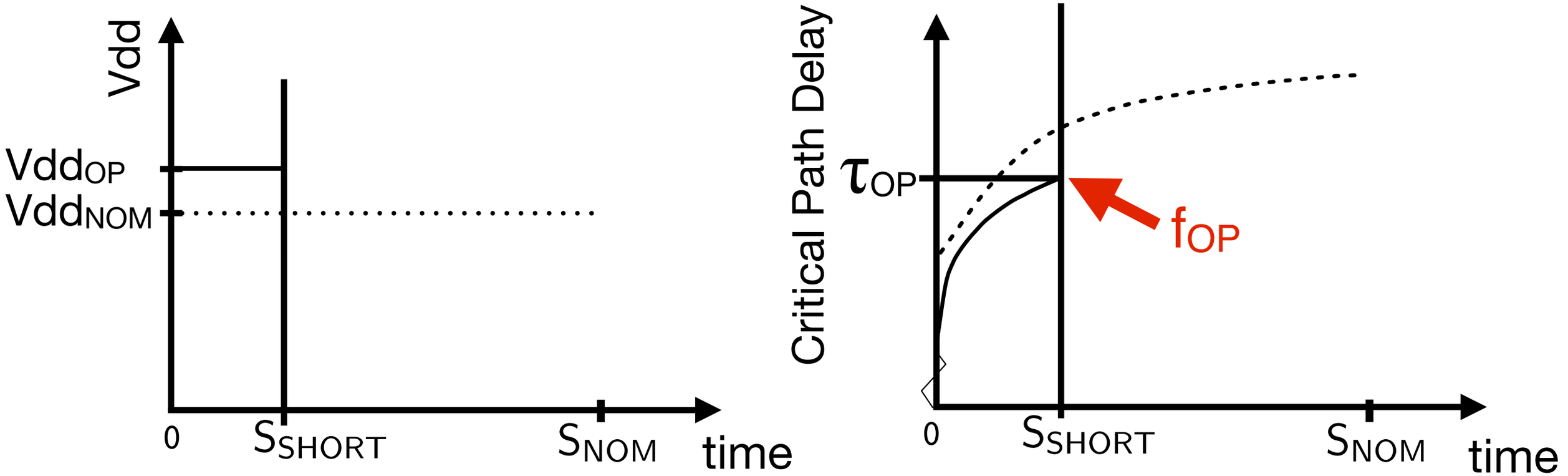



- Higher Vdd: $Vdd_{OP}$ >> $Vdd_{NOM}$
- Result: Lower critical path delay; higher aging rate

# Impact of Operation at Higher V/f on Aging

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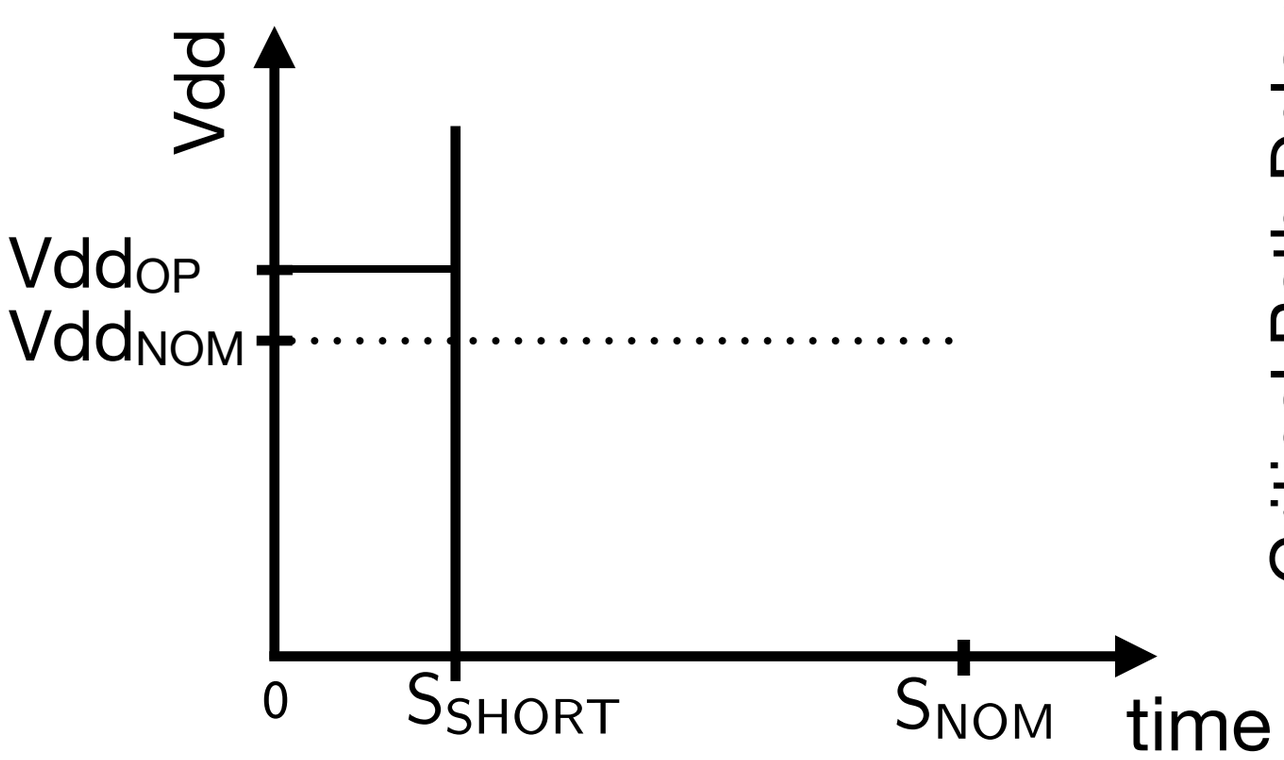


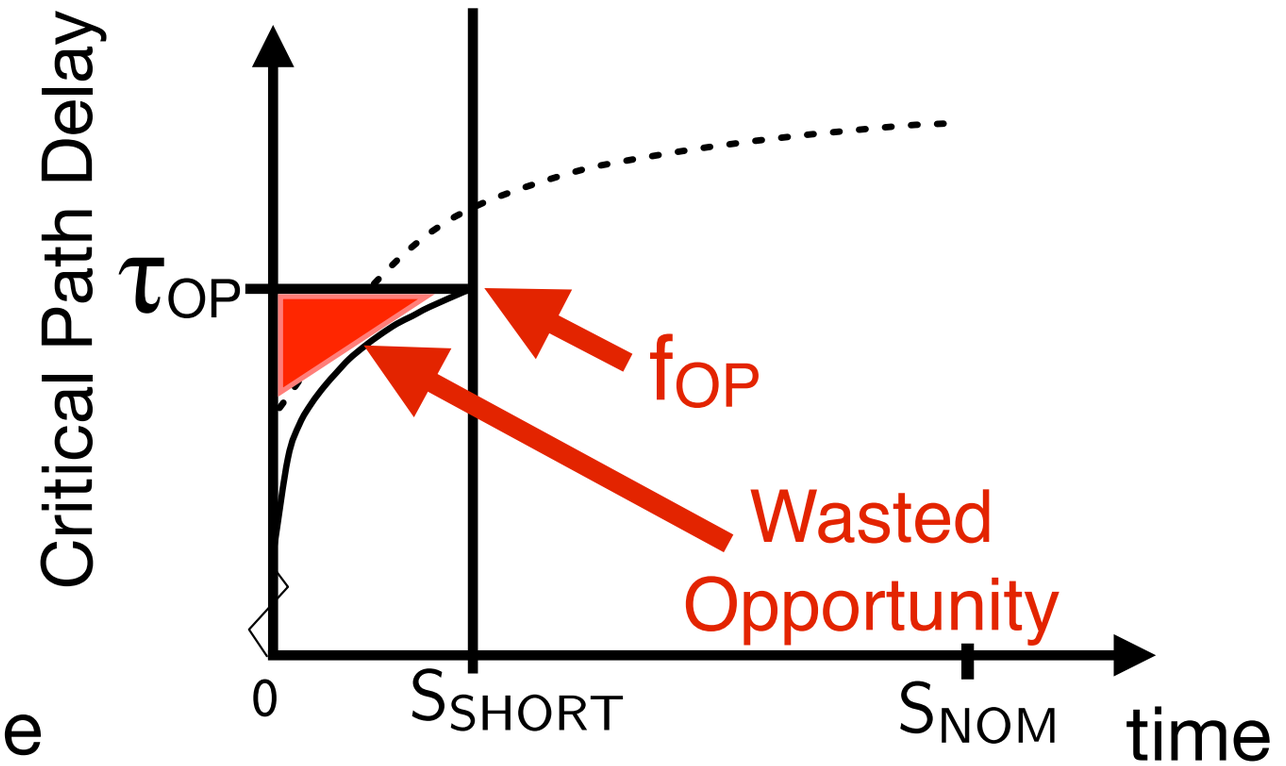


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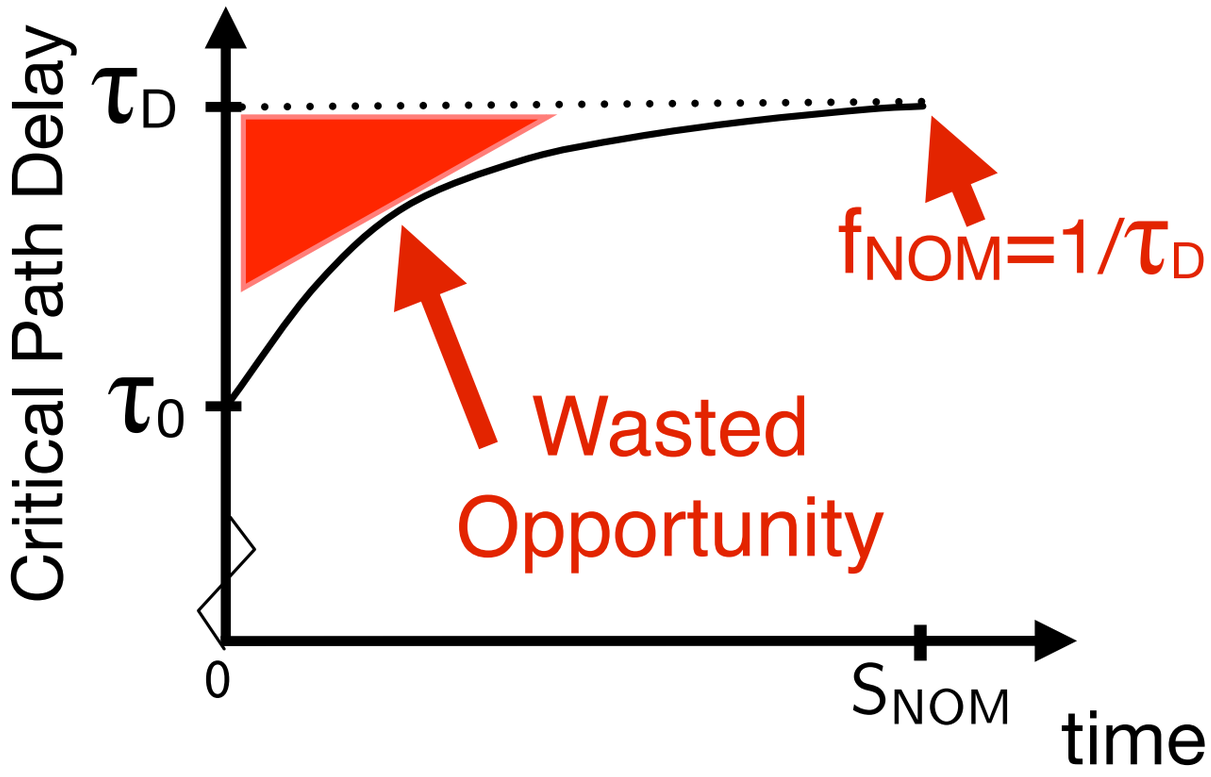
# How to Manage Aging Optimally?



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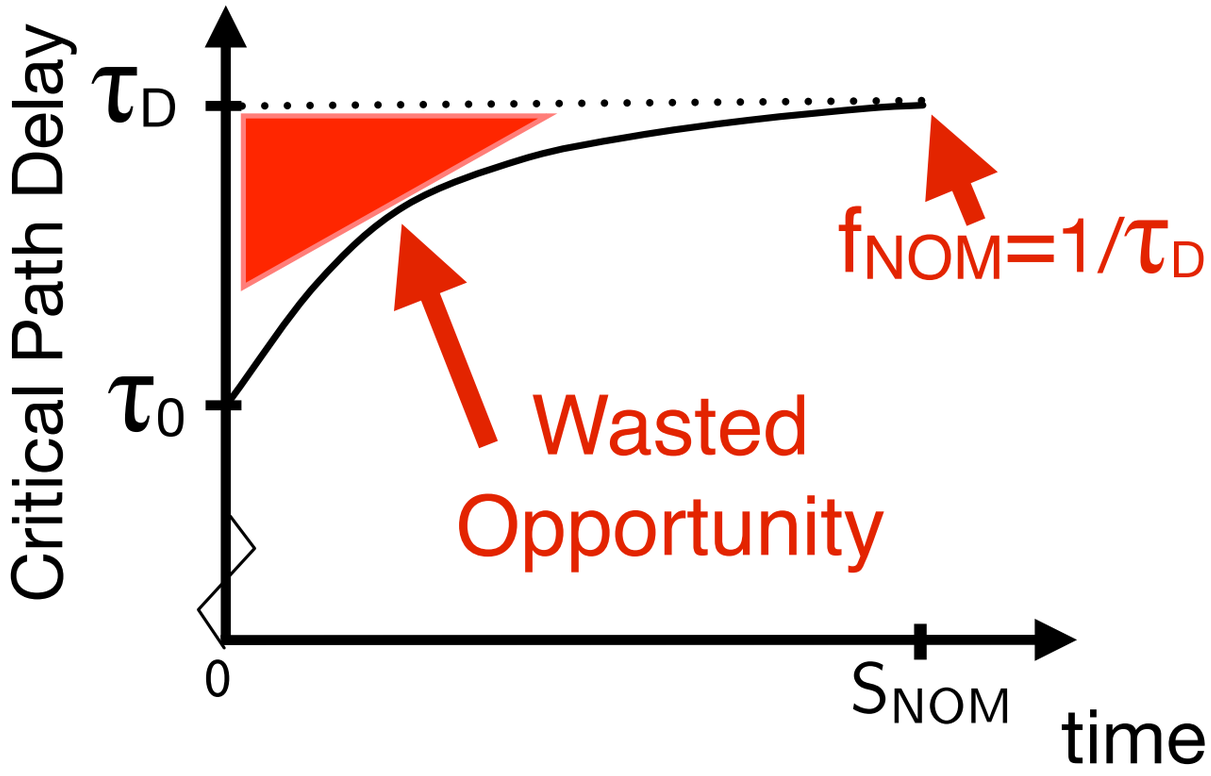
Contribution: DVS for Aging Management (DVSAM)



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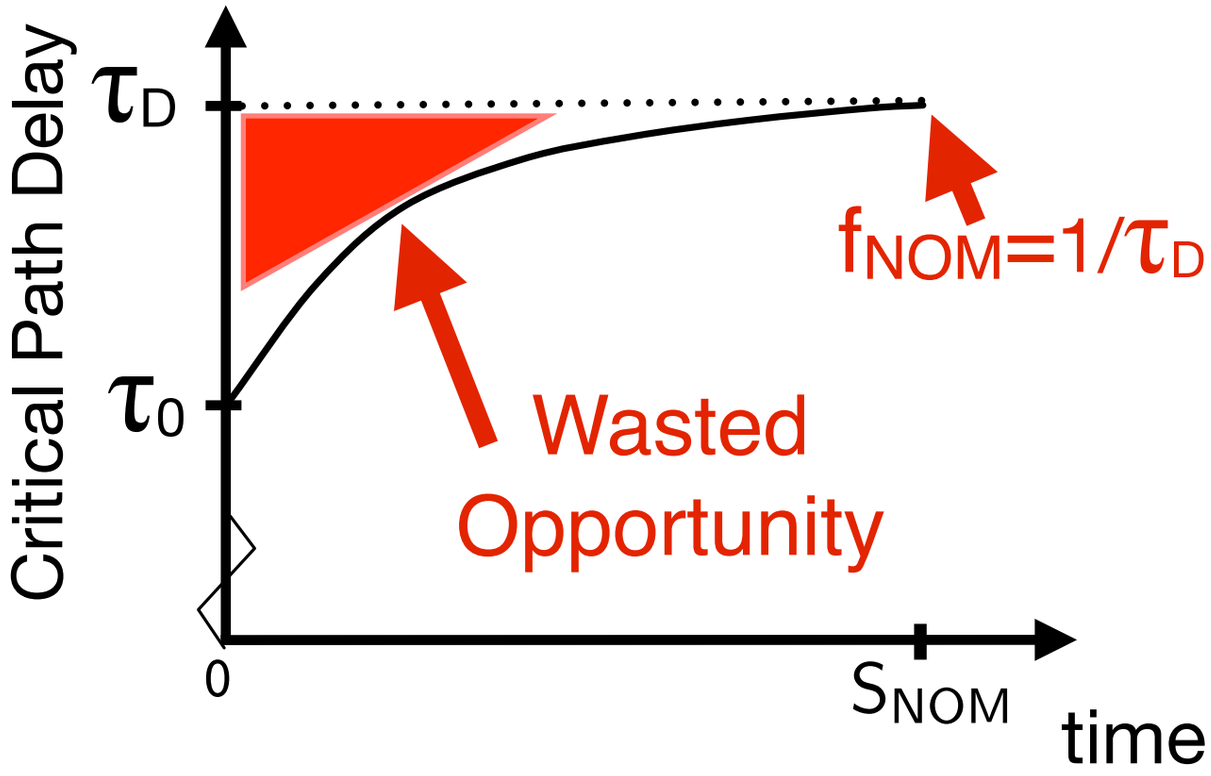


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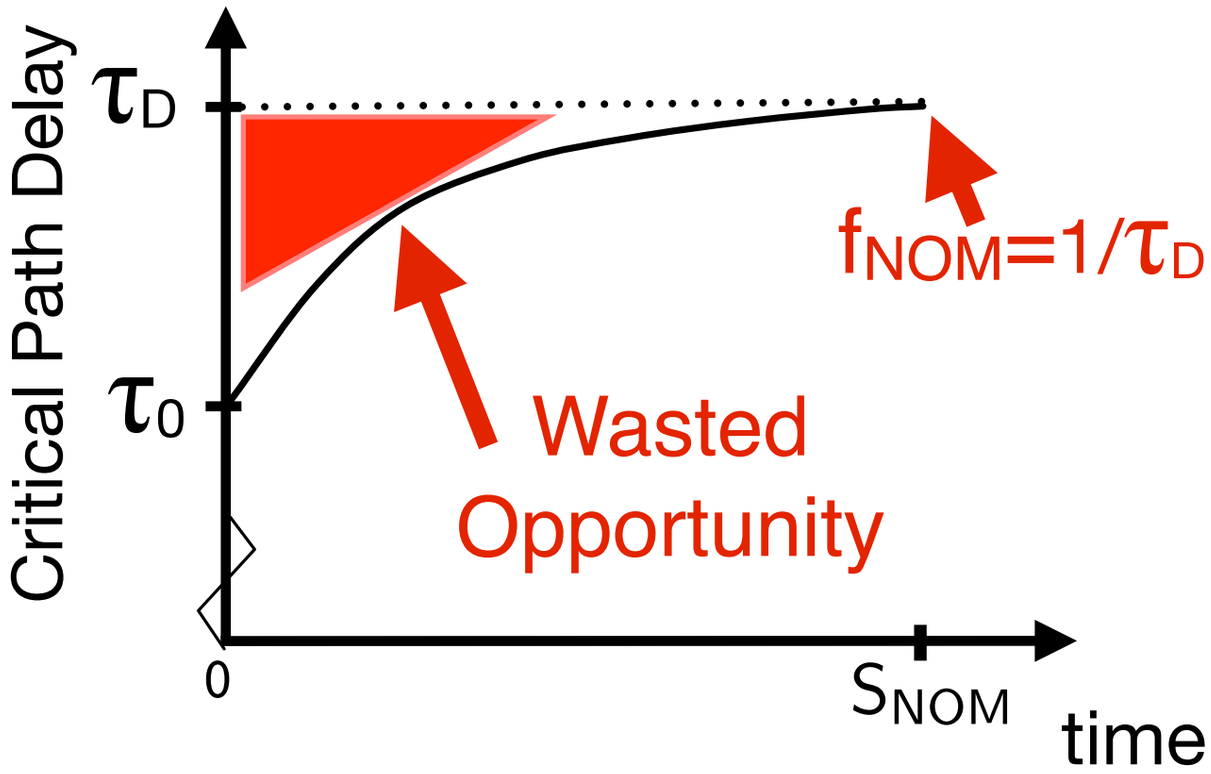


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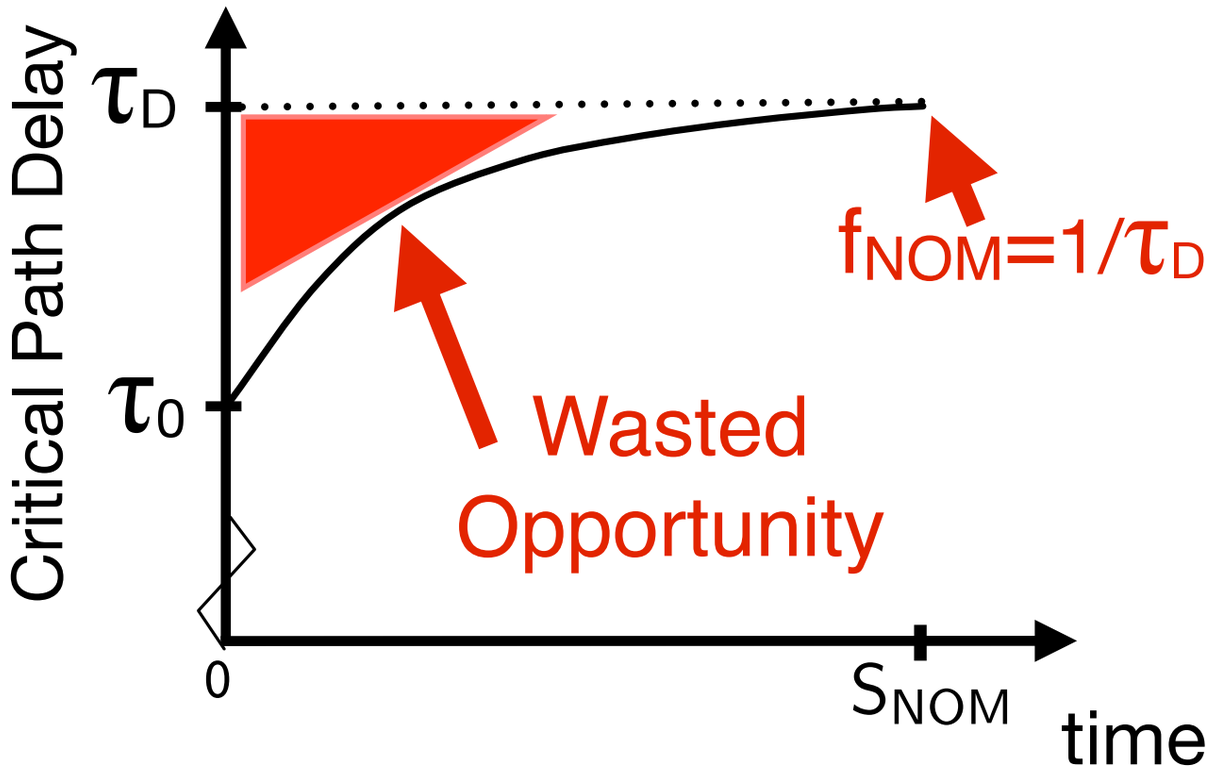


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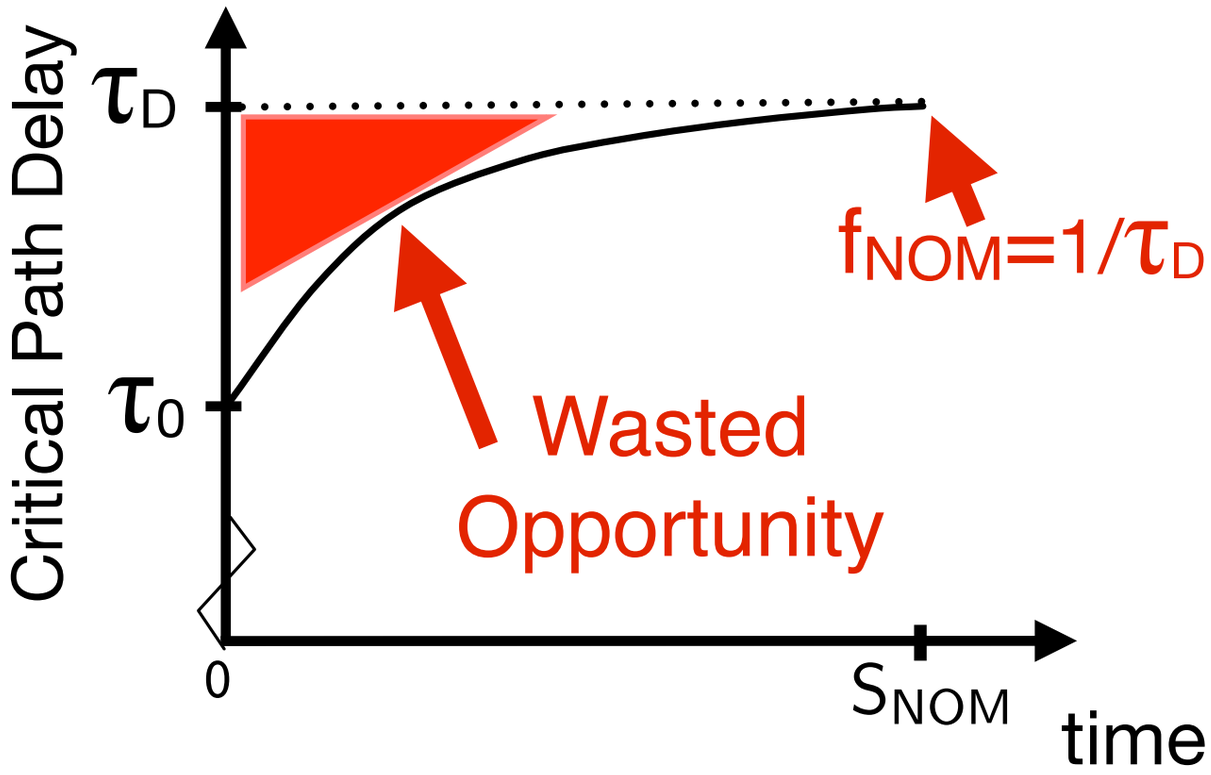


- Change Vdd with time to compensate for critical path degradation
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- DVSAM-Pow: Turn wasted opportunity to power efficiency
- DVSAM-Perf: Turn wasted opportunity to higher frequency

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Idea: Minimize power consumption at $f_{NOM} = 1/\tau_D$

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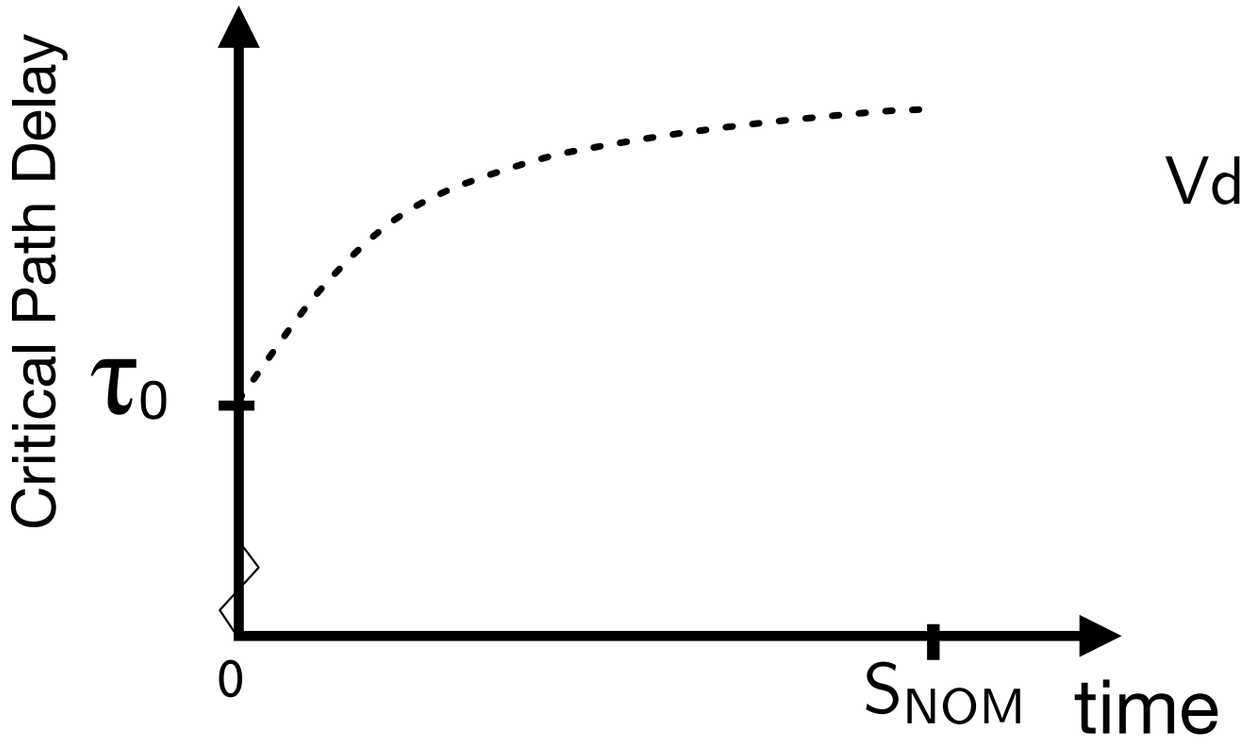


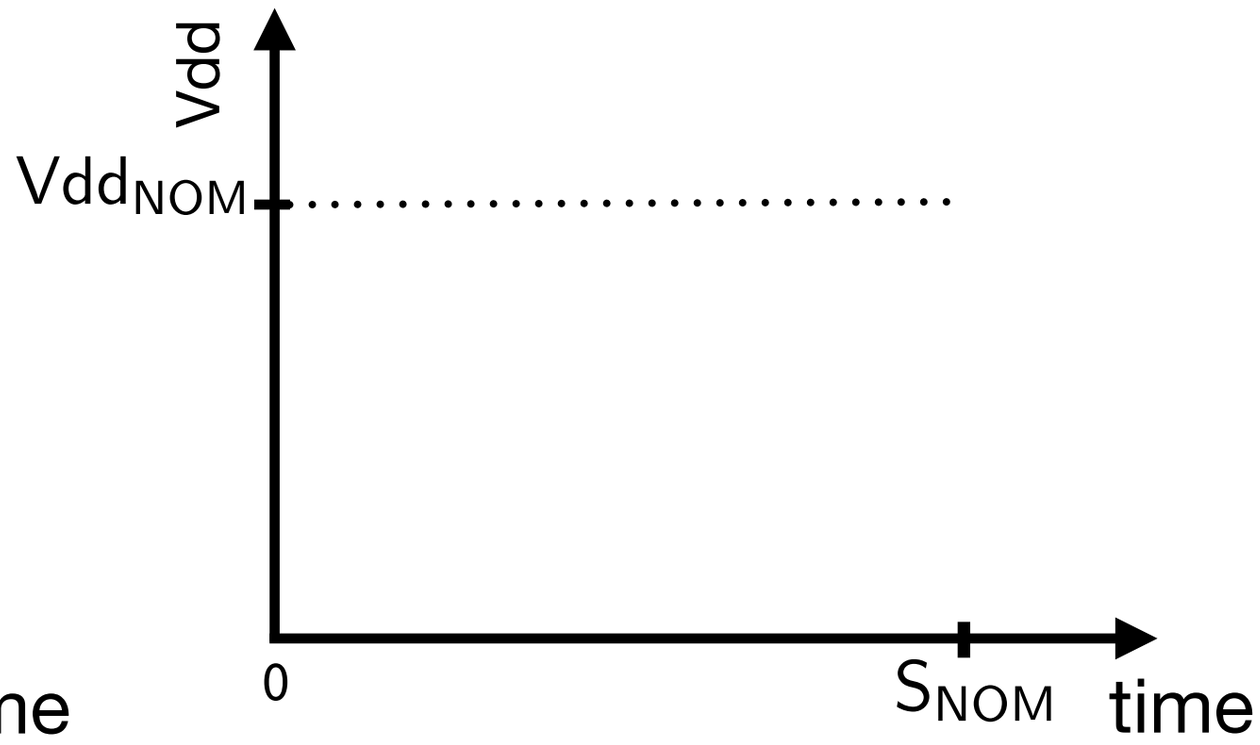

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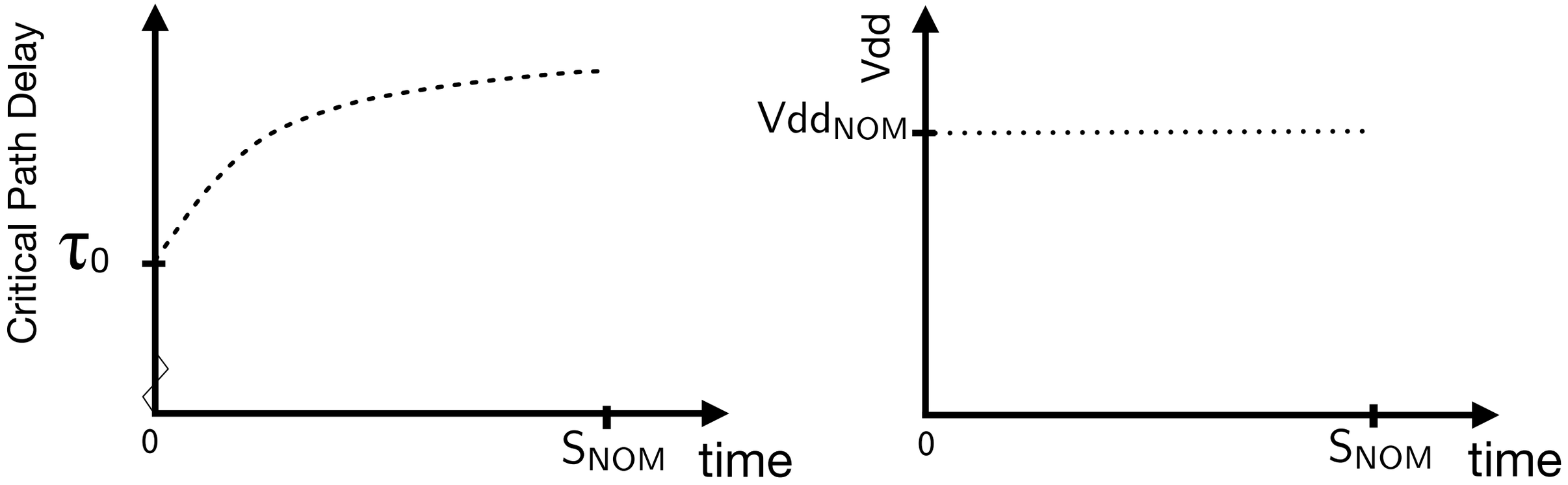


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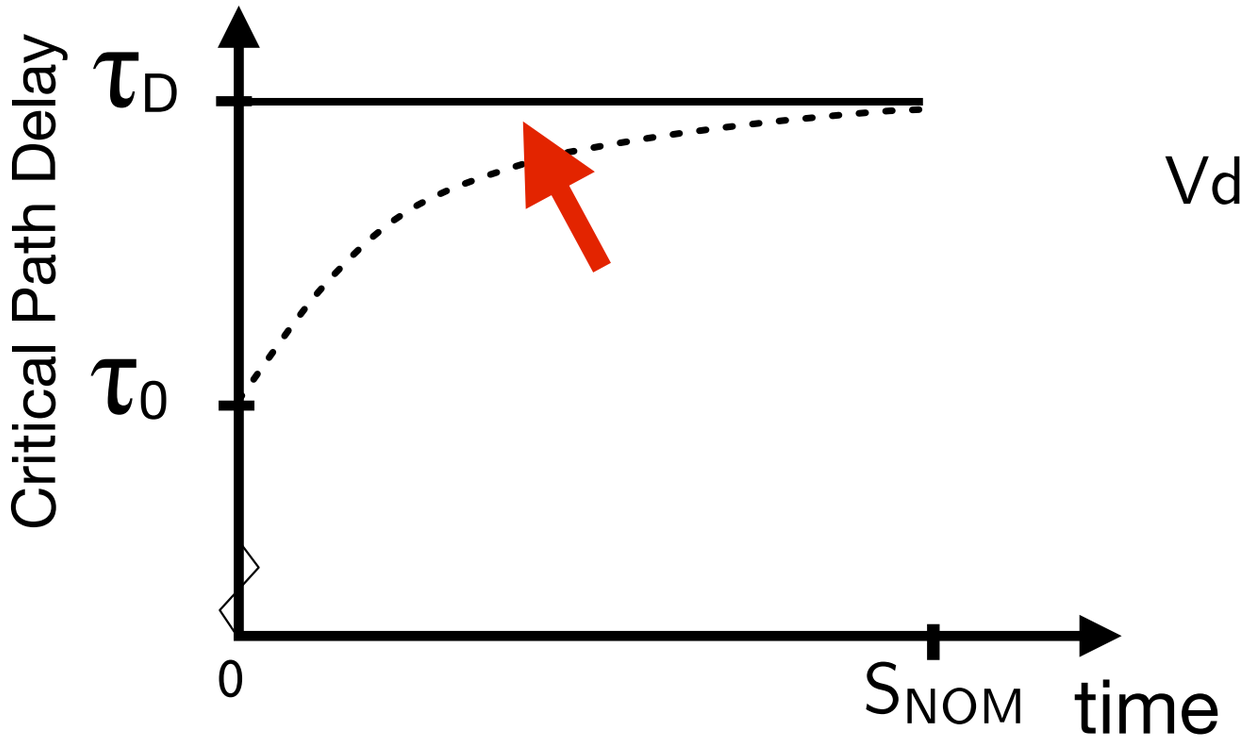


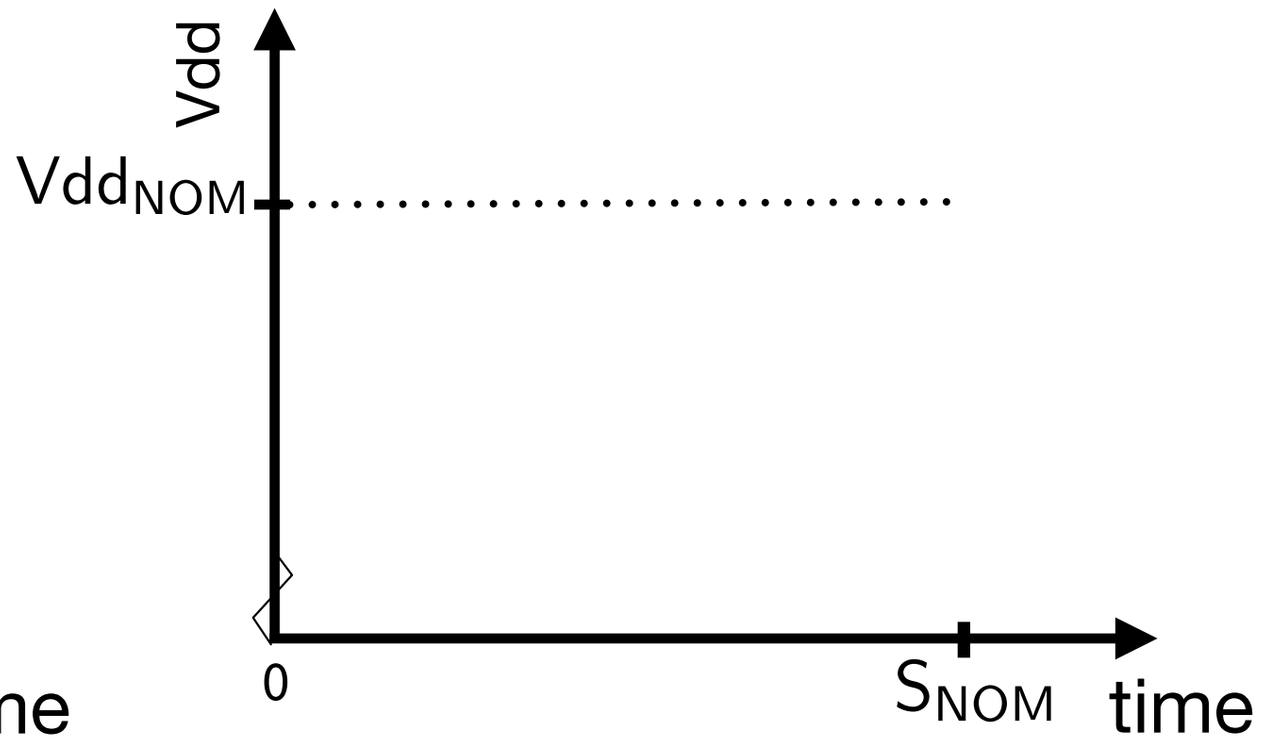


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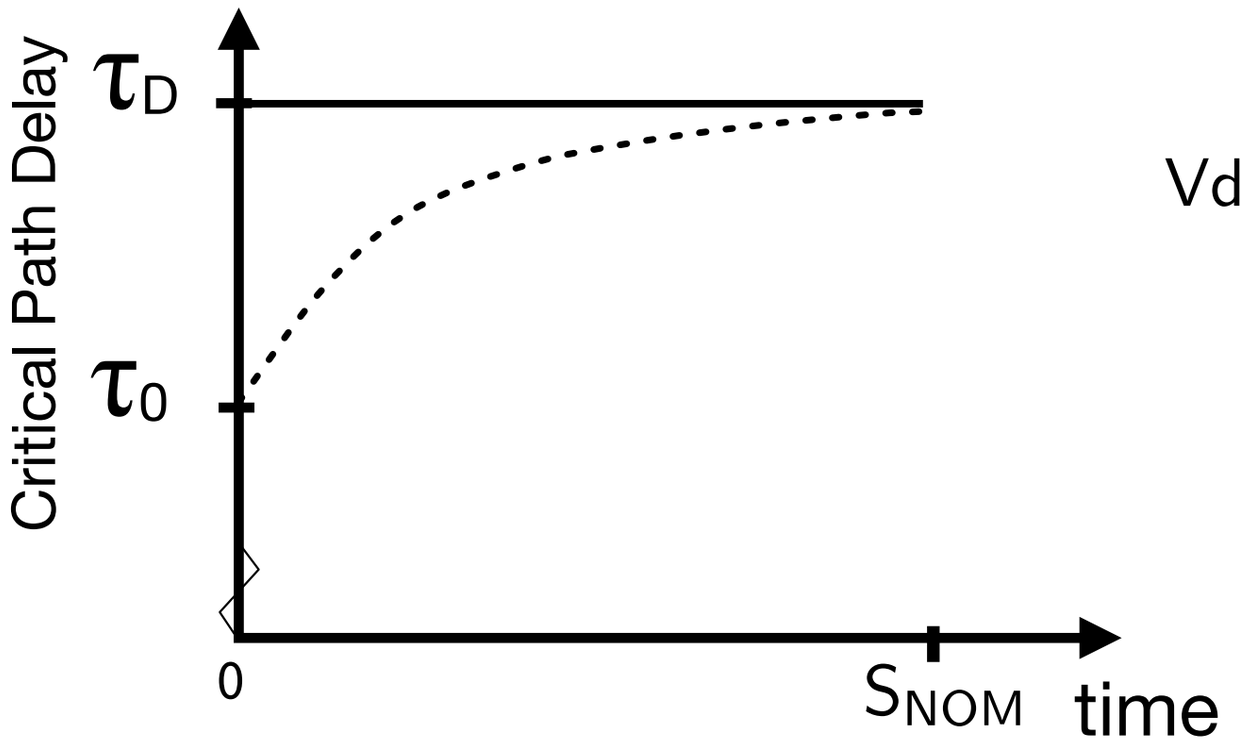


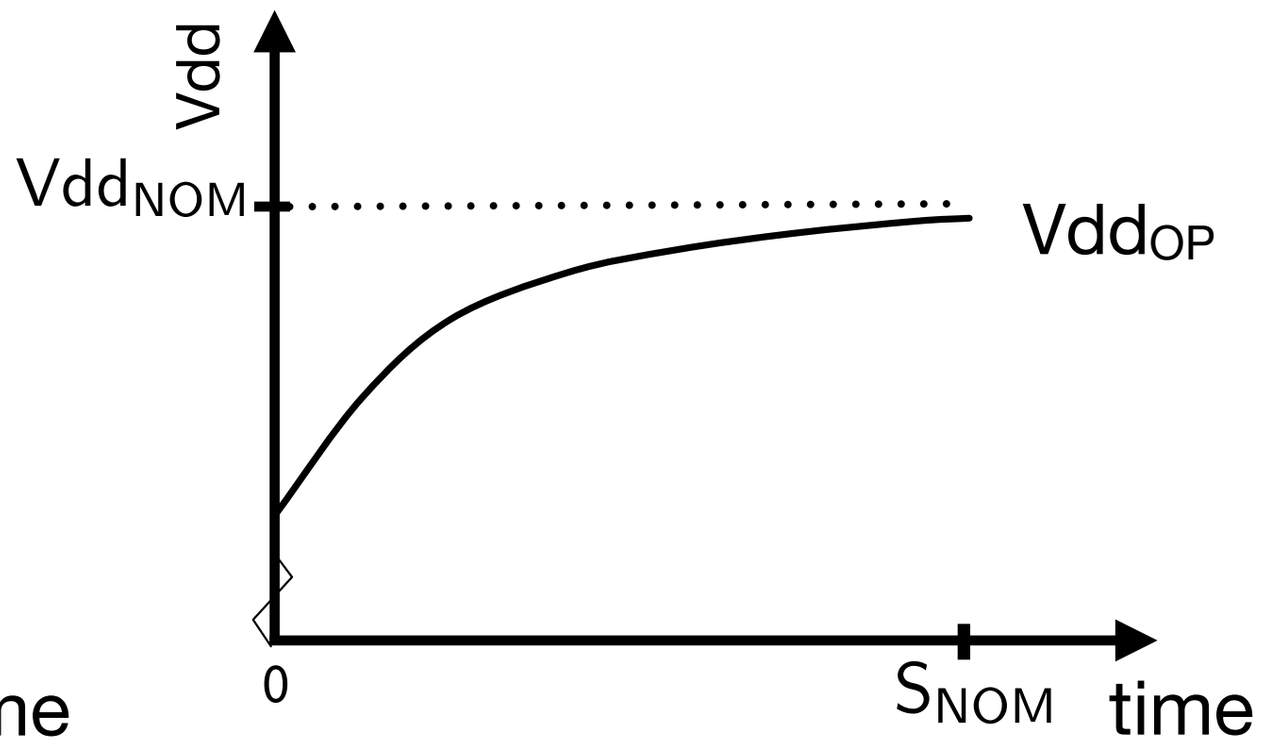


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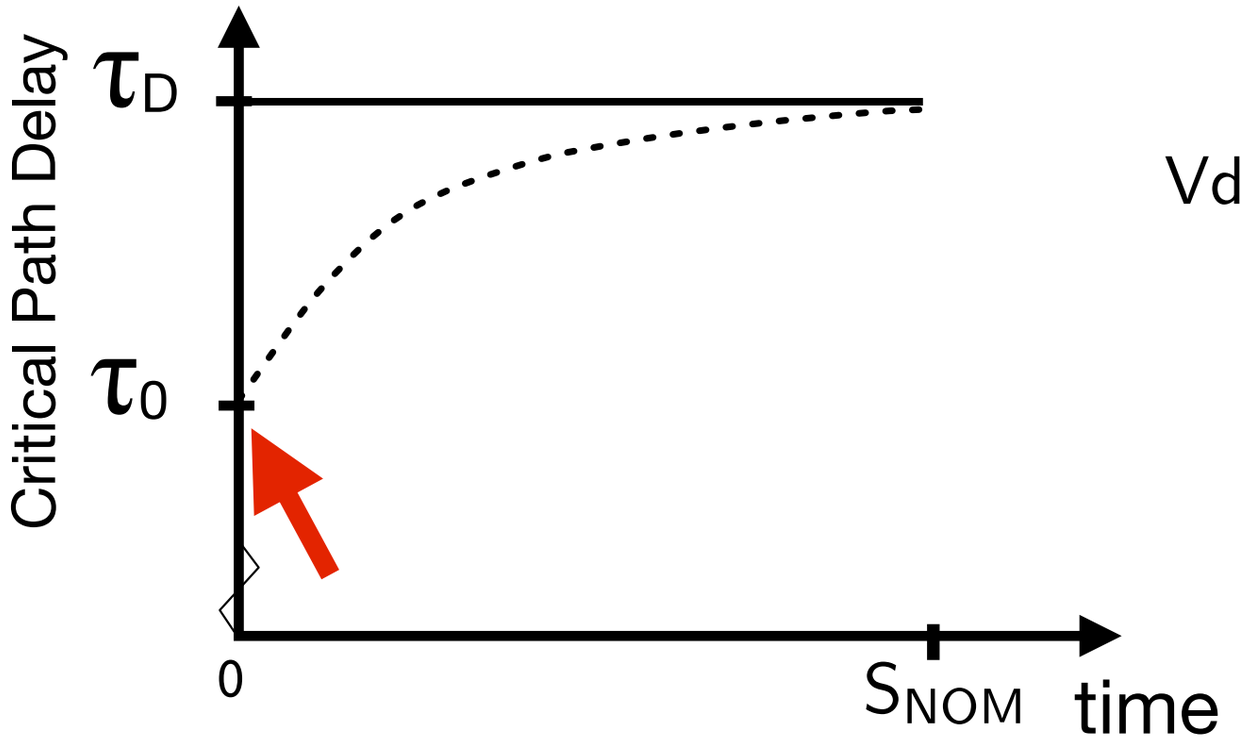


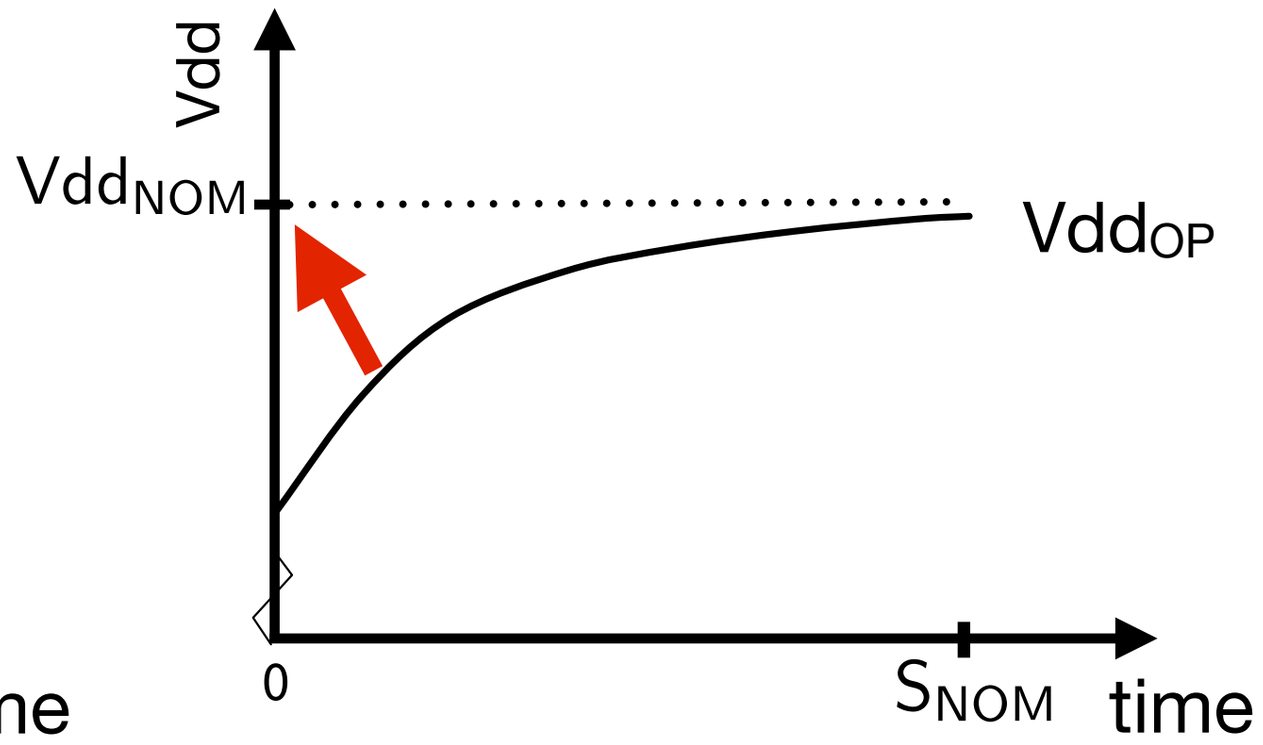


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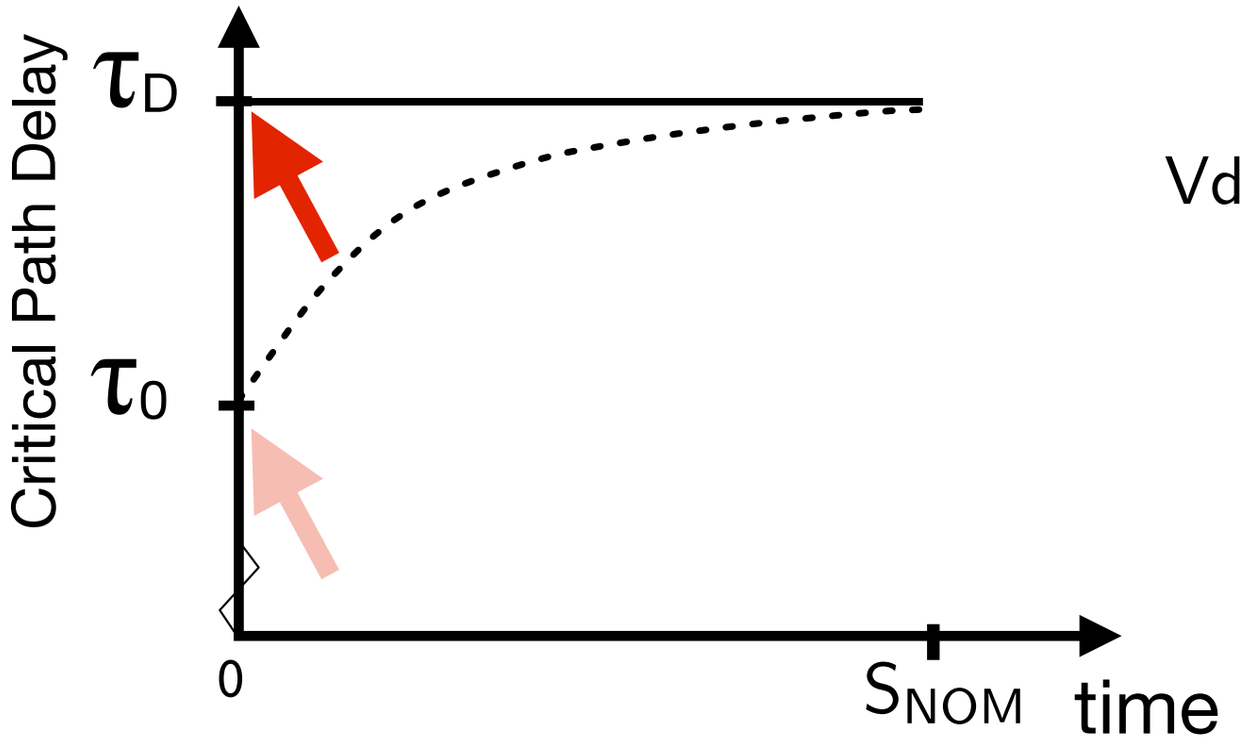


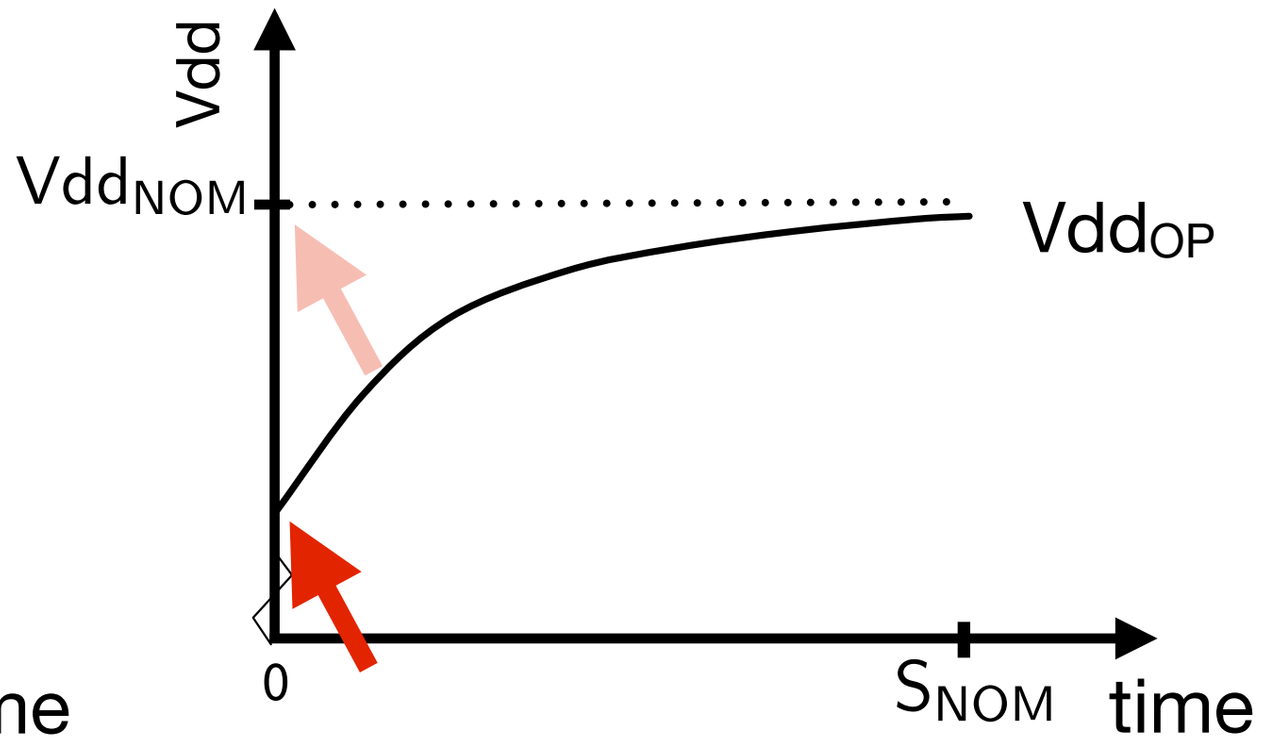


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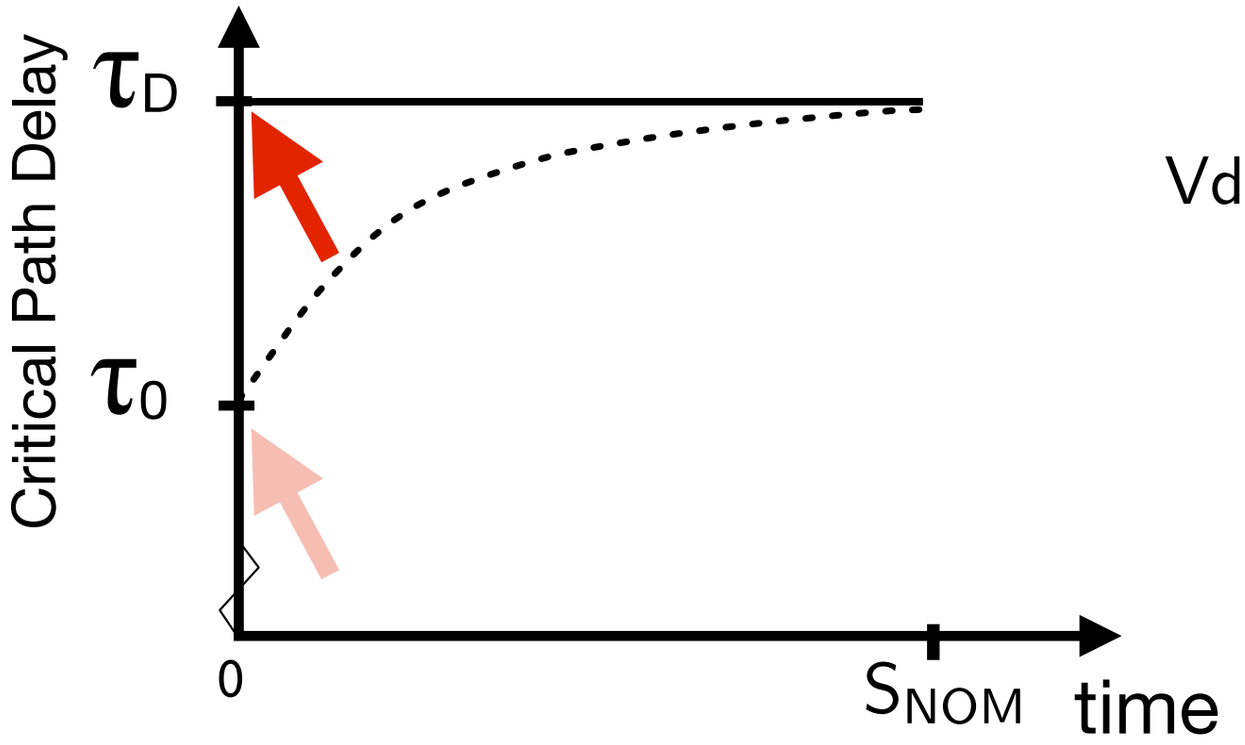


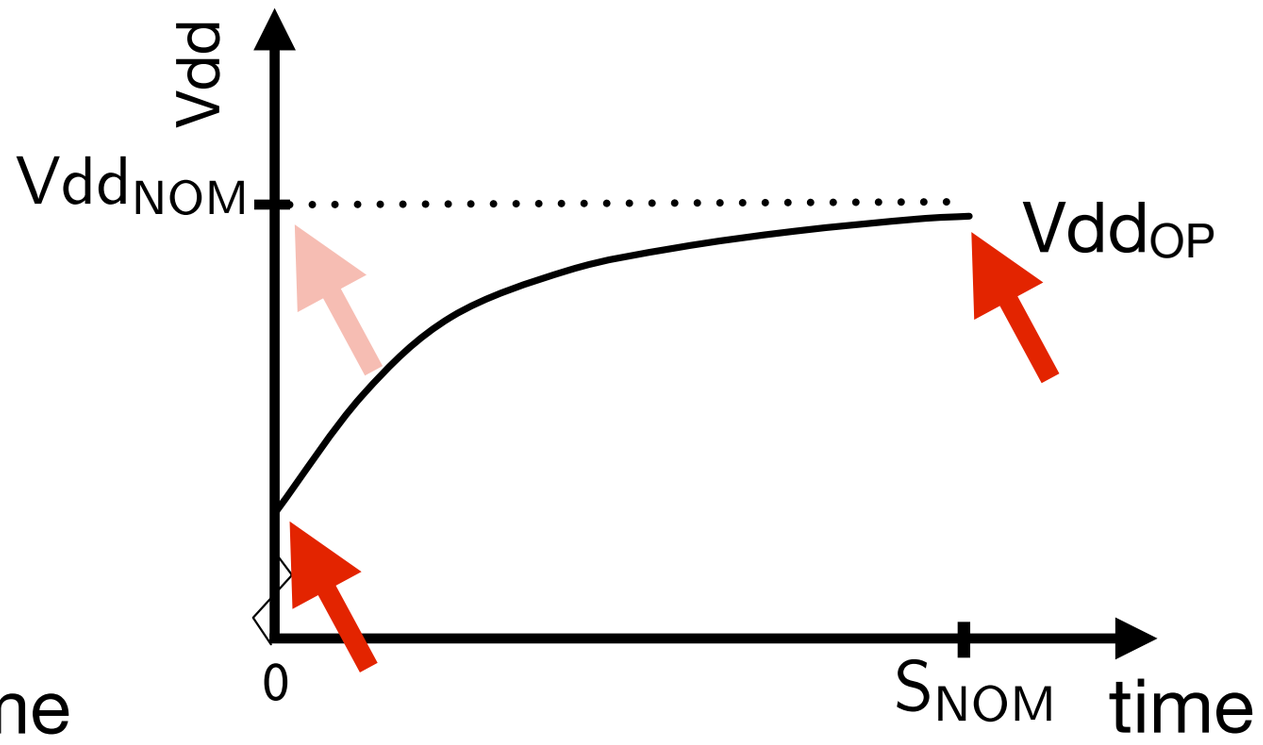


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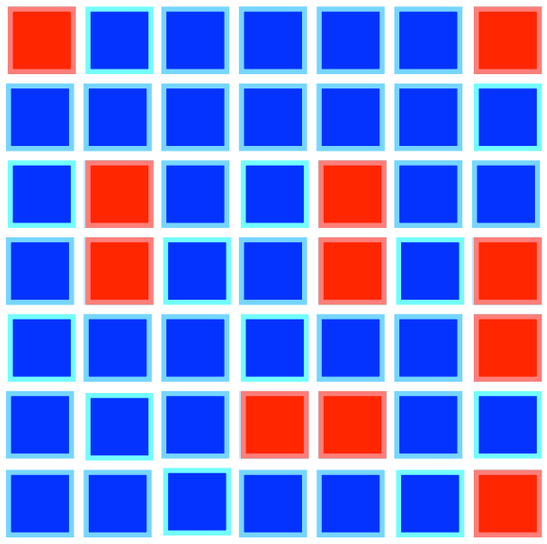

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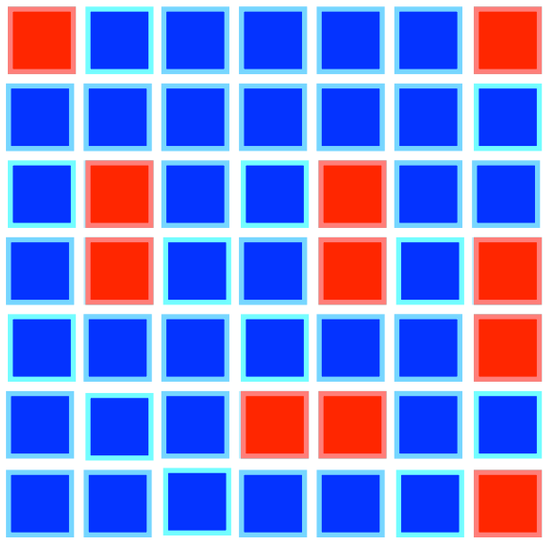

- Vdd < $Vdd_{NOM}$ and f = $f_{NOM}$ throughout $S_{NOM}$

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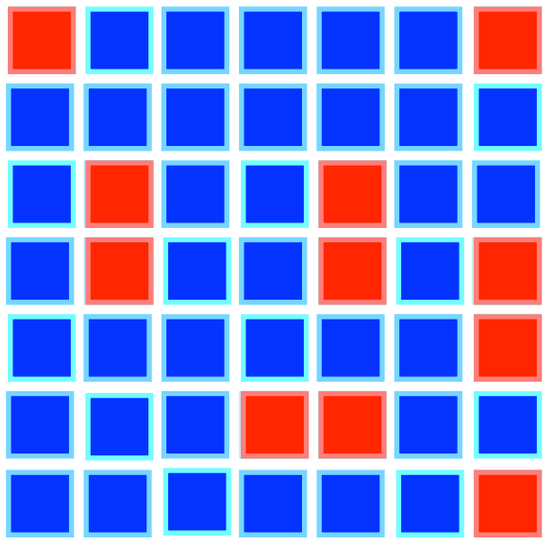

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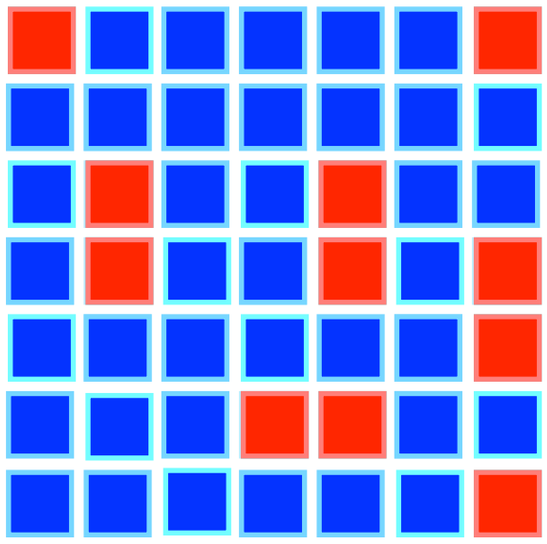

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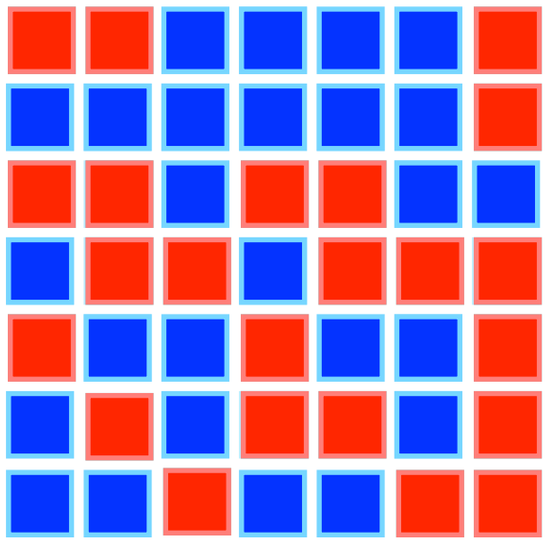

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➡ Increased throughput

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Idea: Maximize frequency for the same service life

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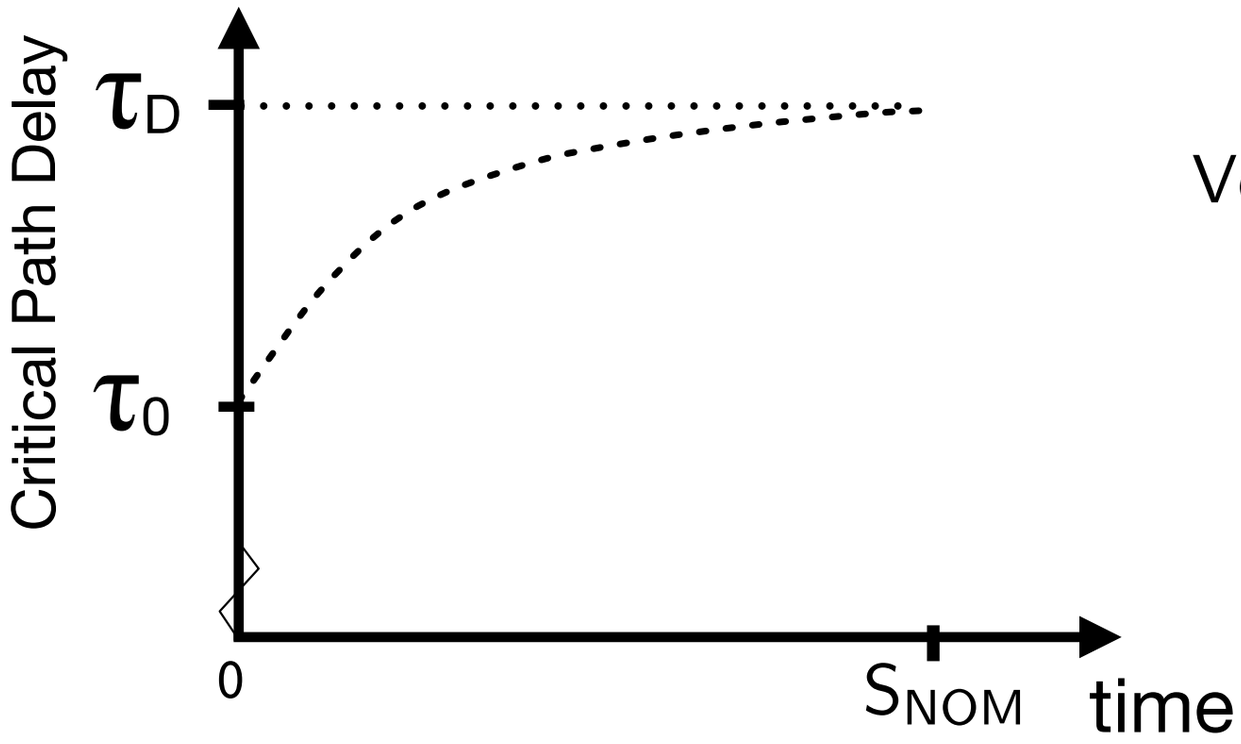


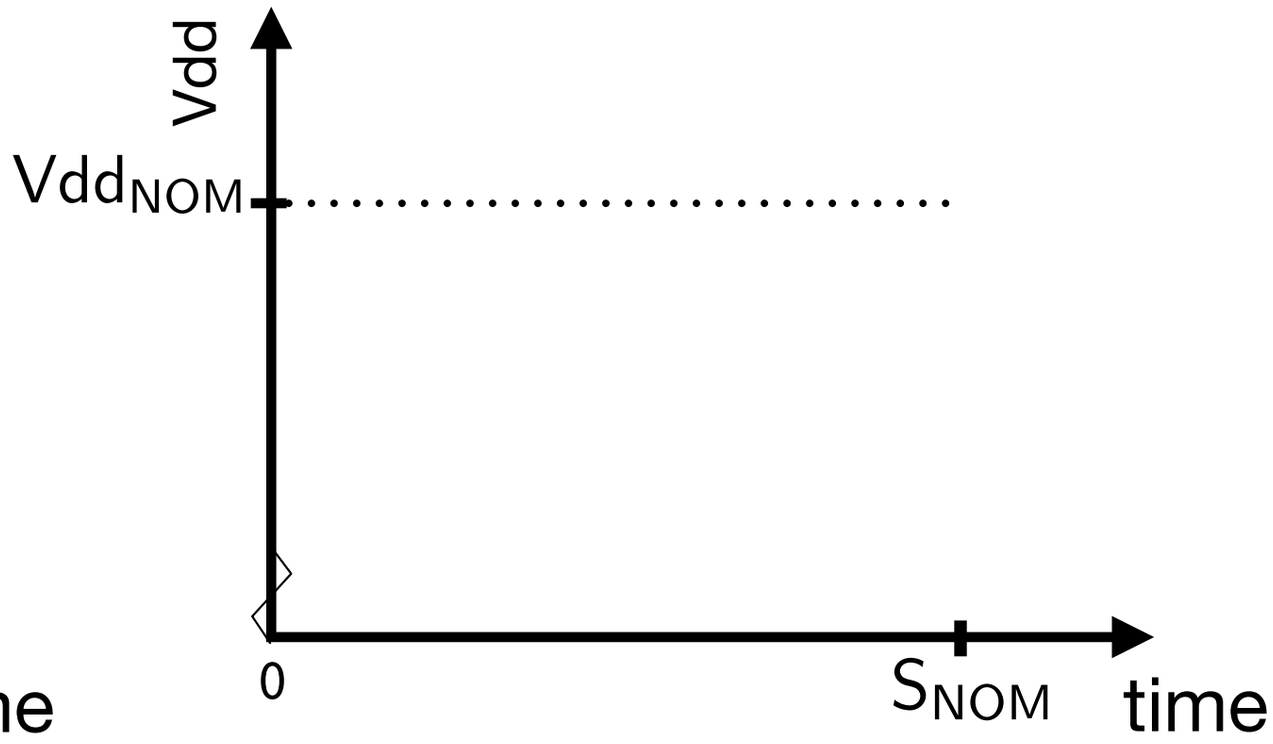

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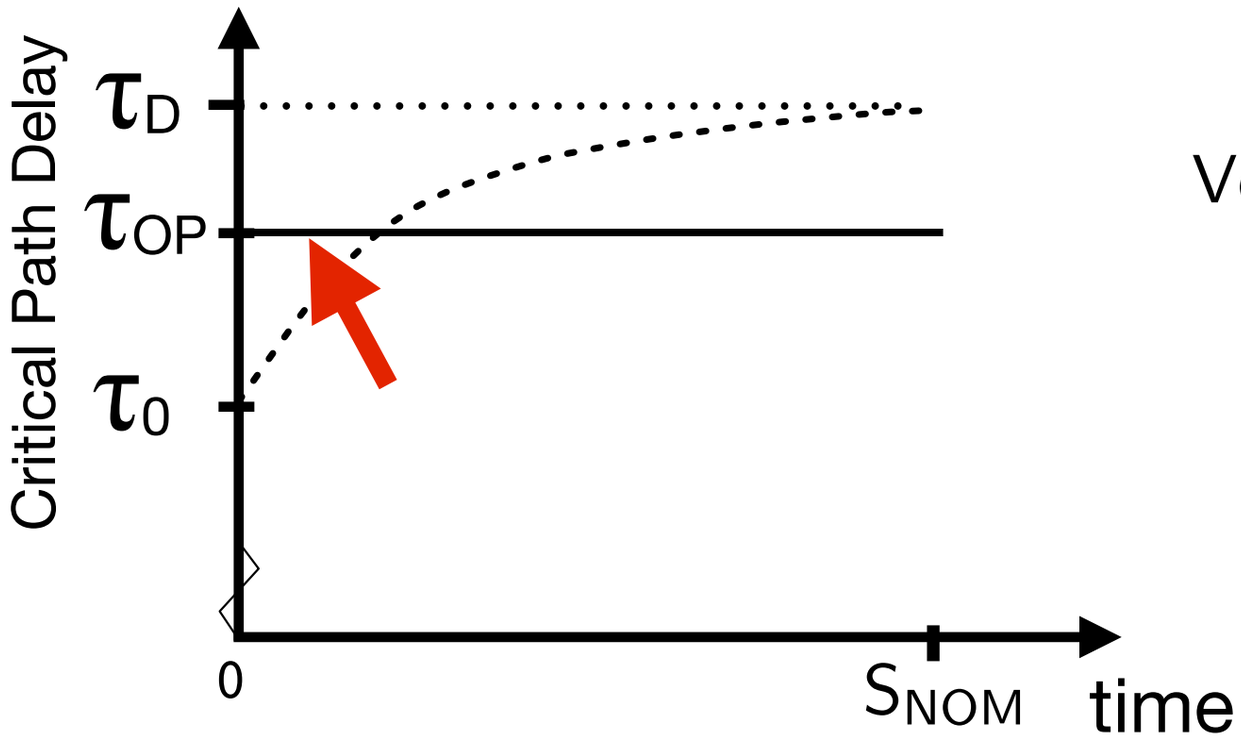


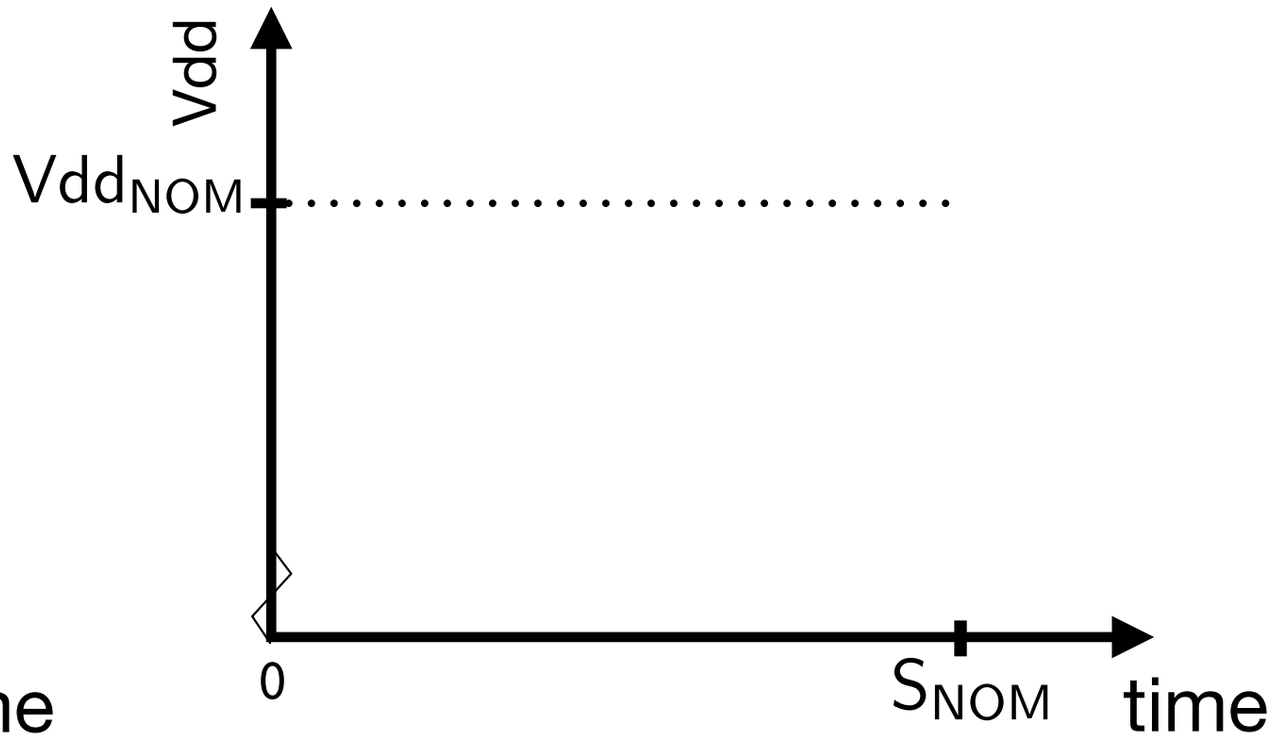


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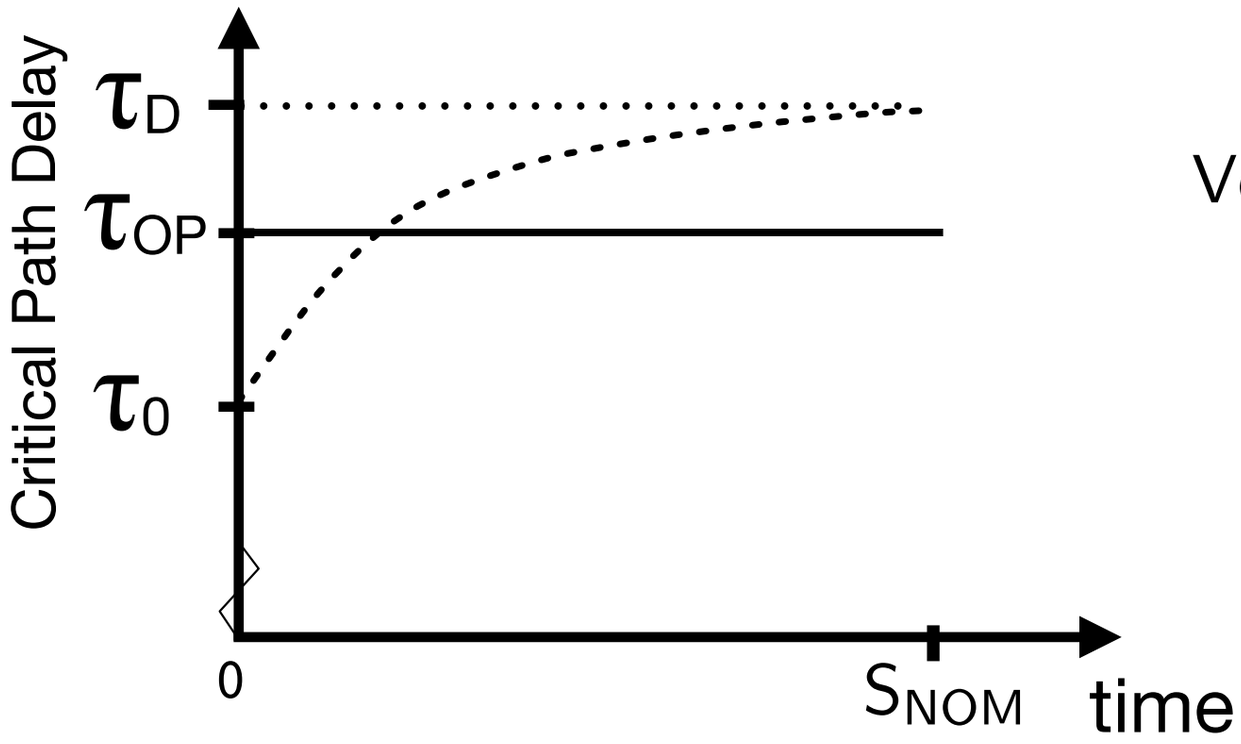


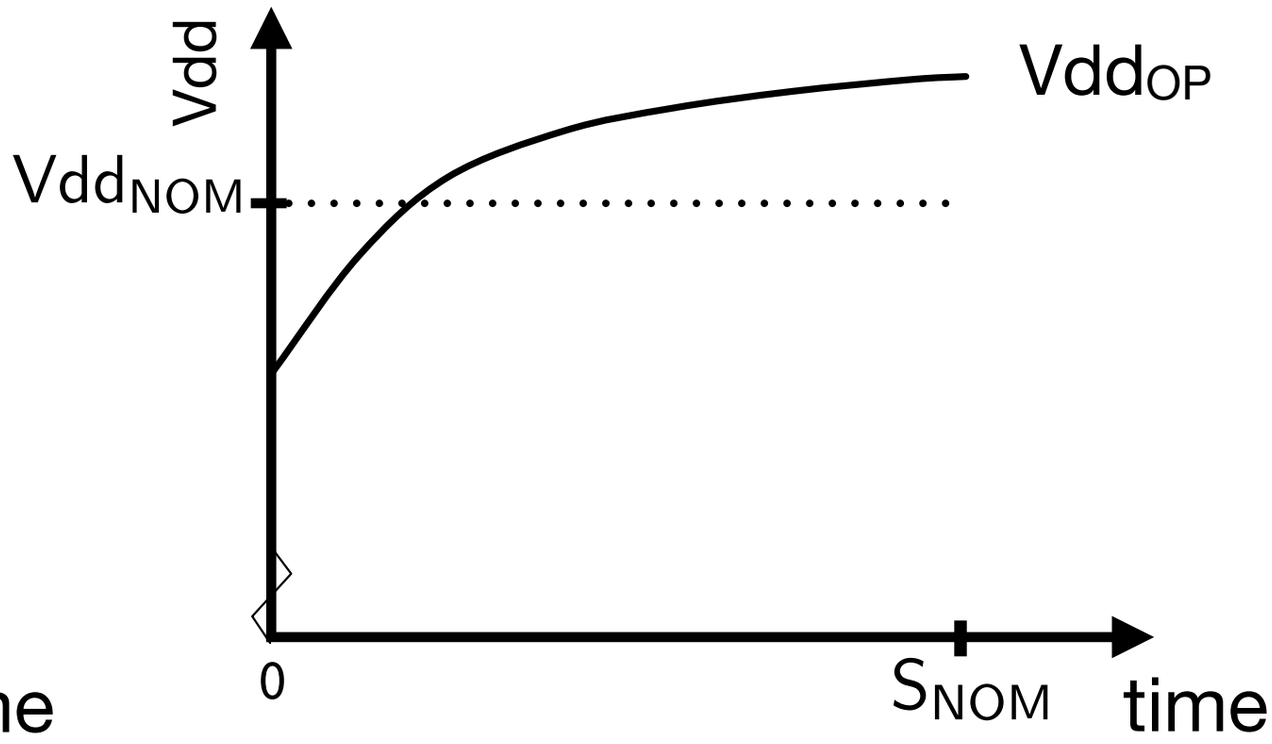


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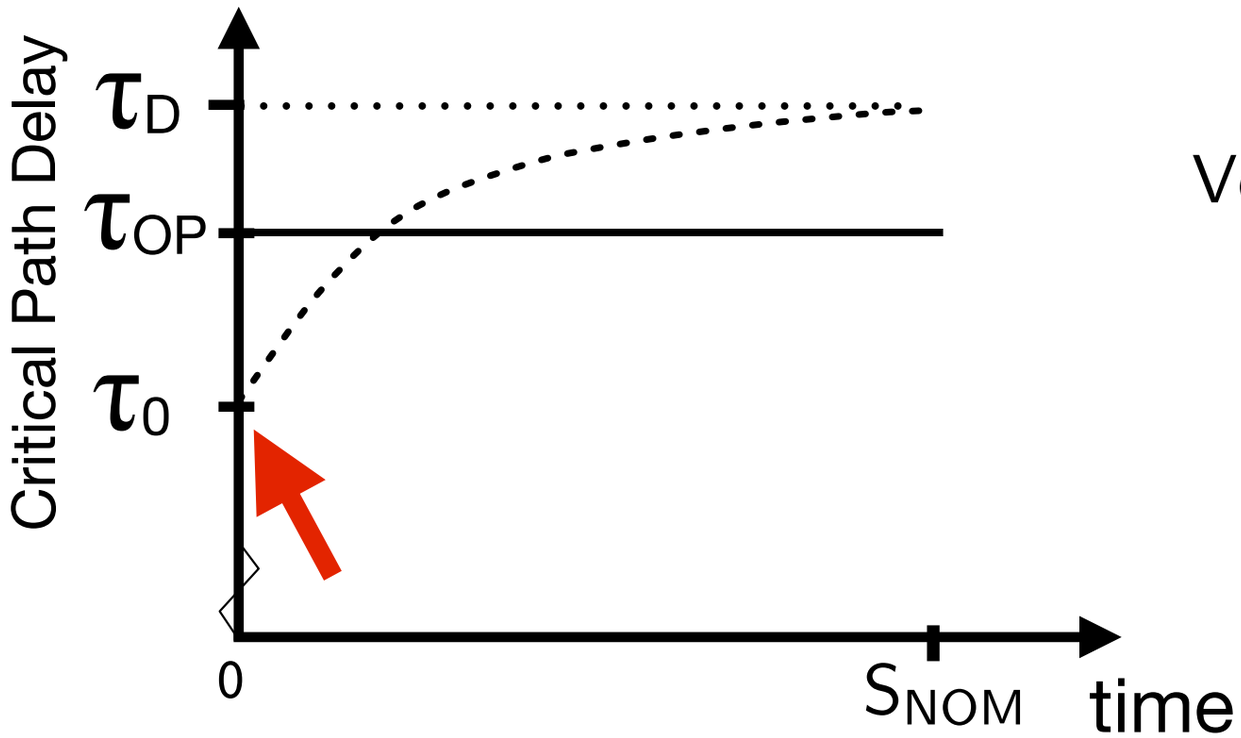


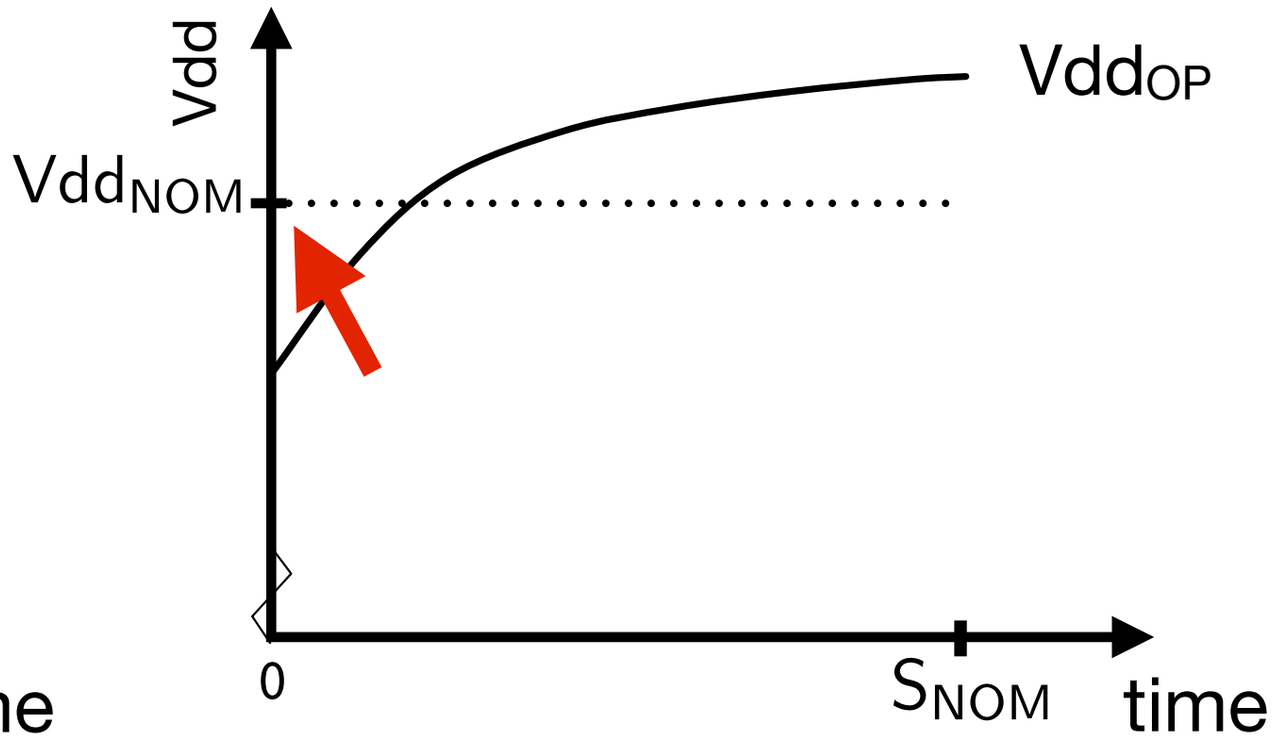


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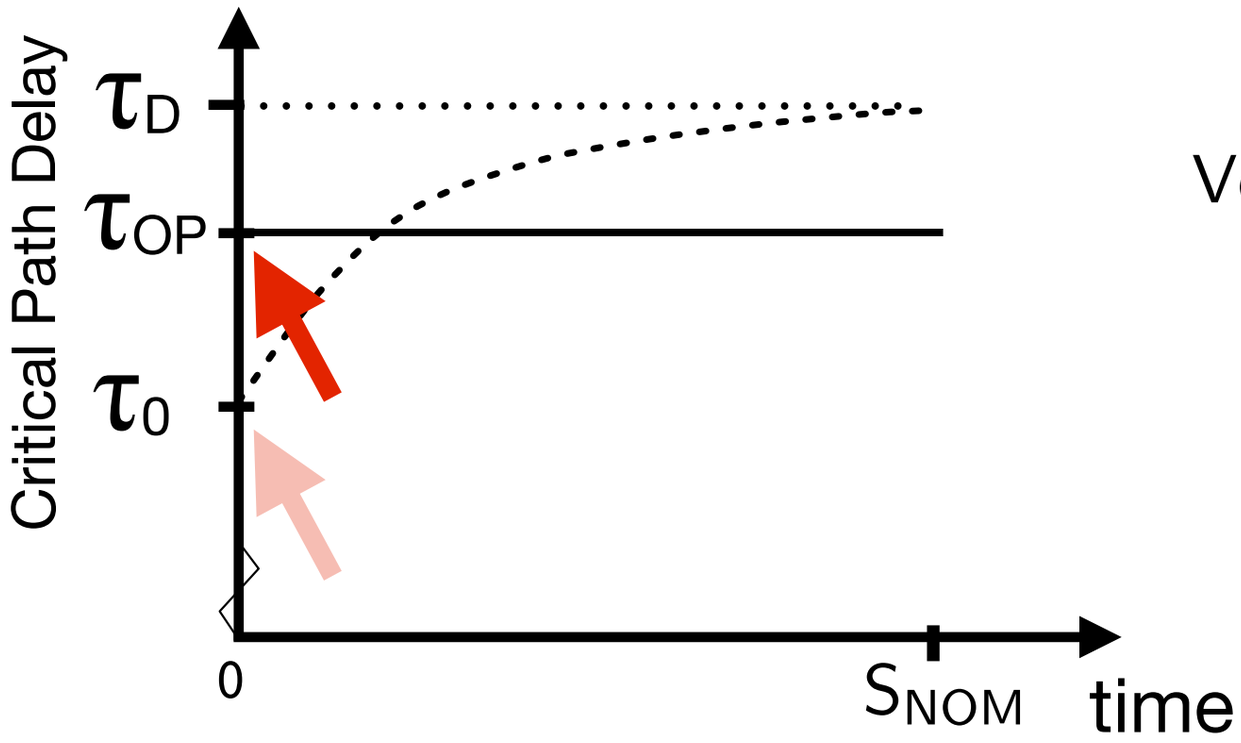


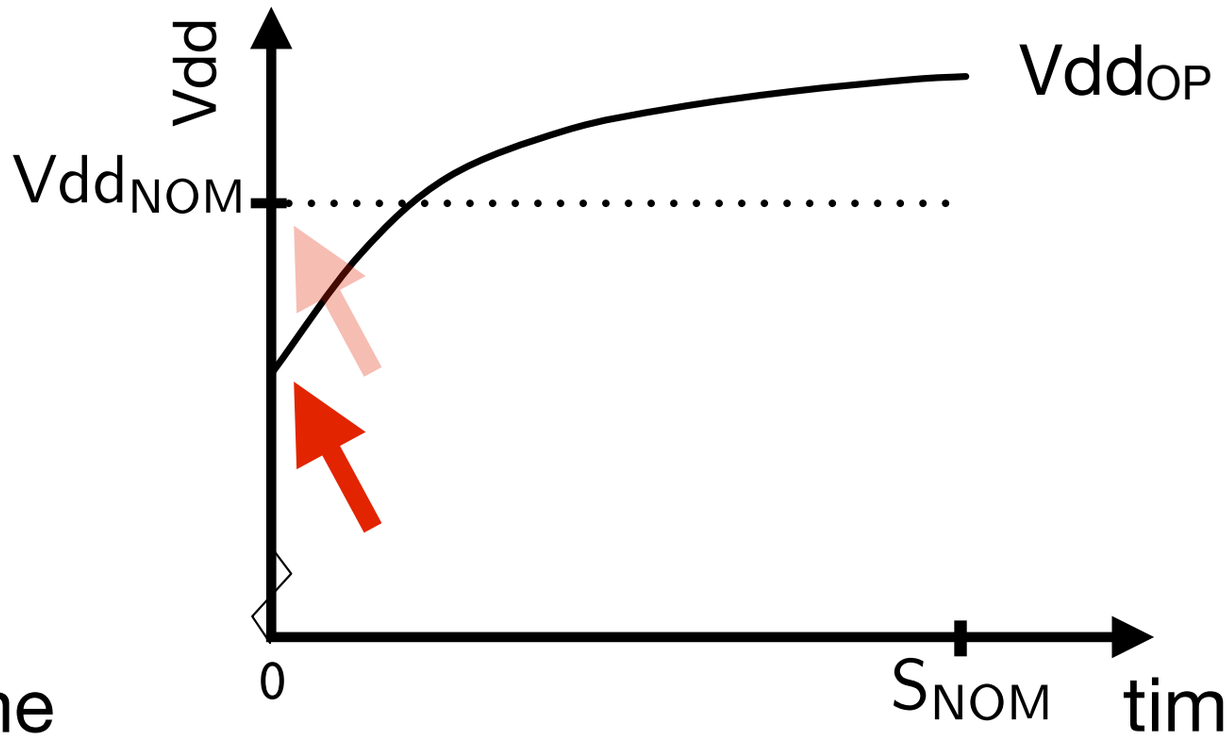


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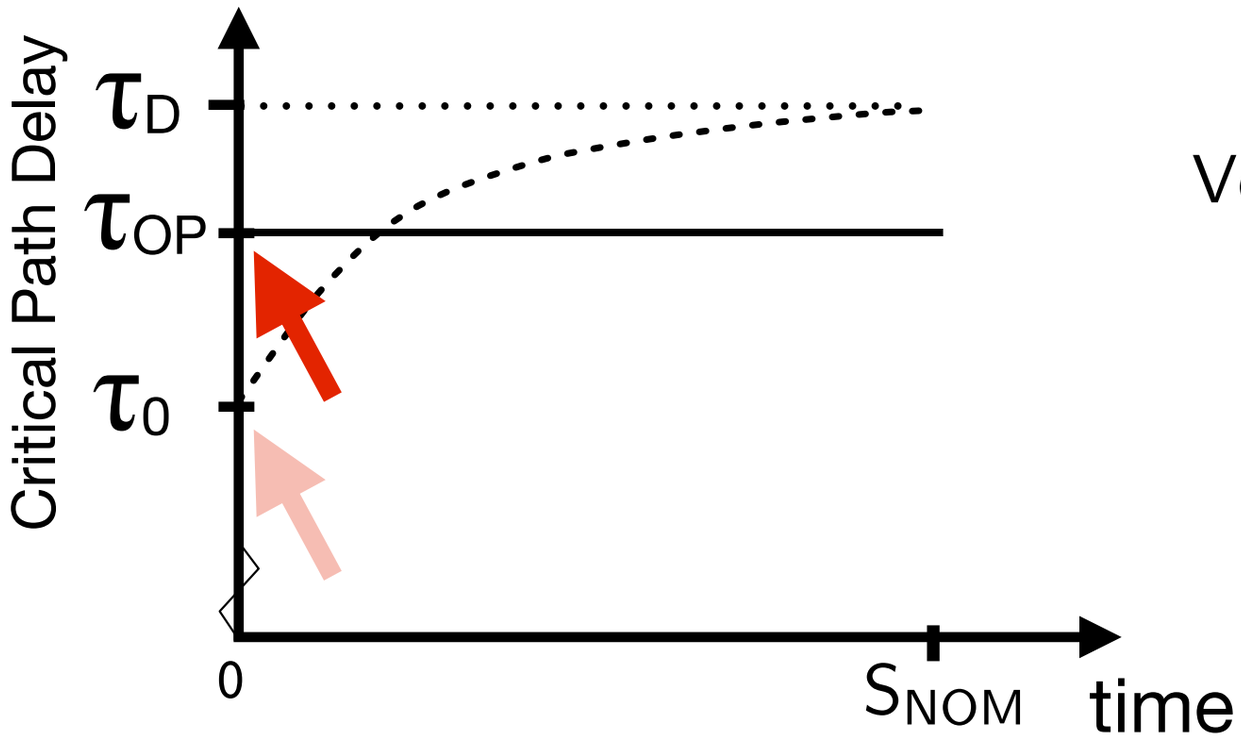


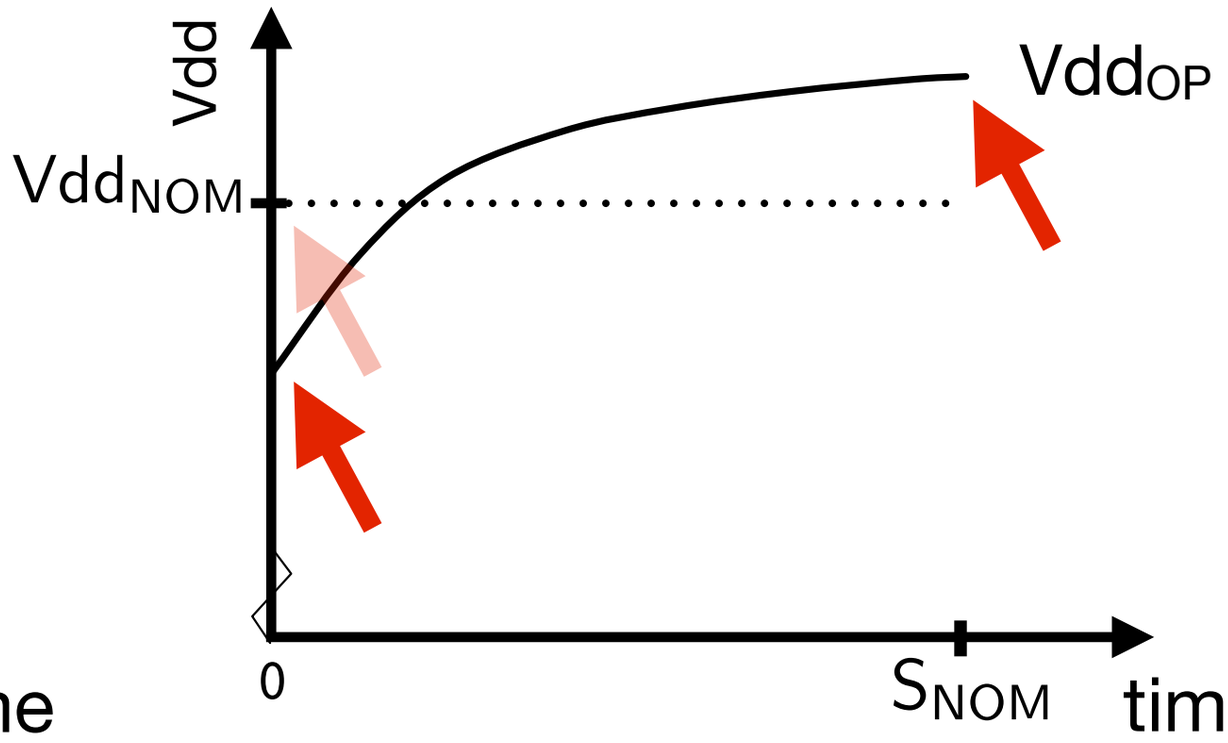


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# DVSAM-Perf for SSHORT

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Idea: Aggressive DVSAM-Perf for a short service life to get even higher performance

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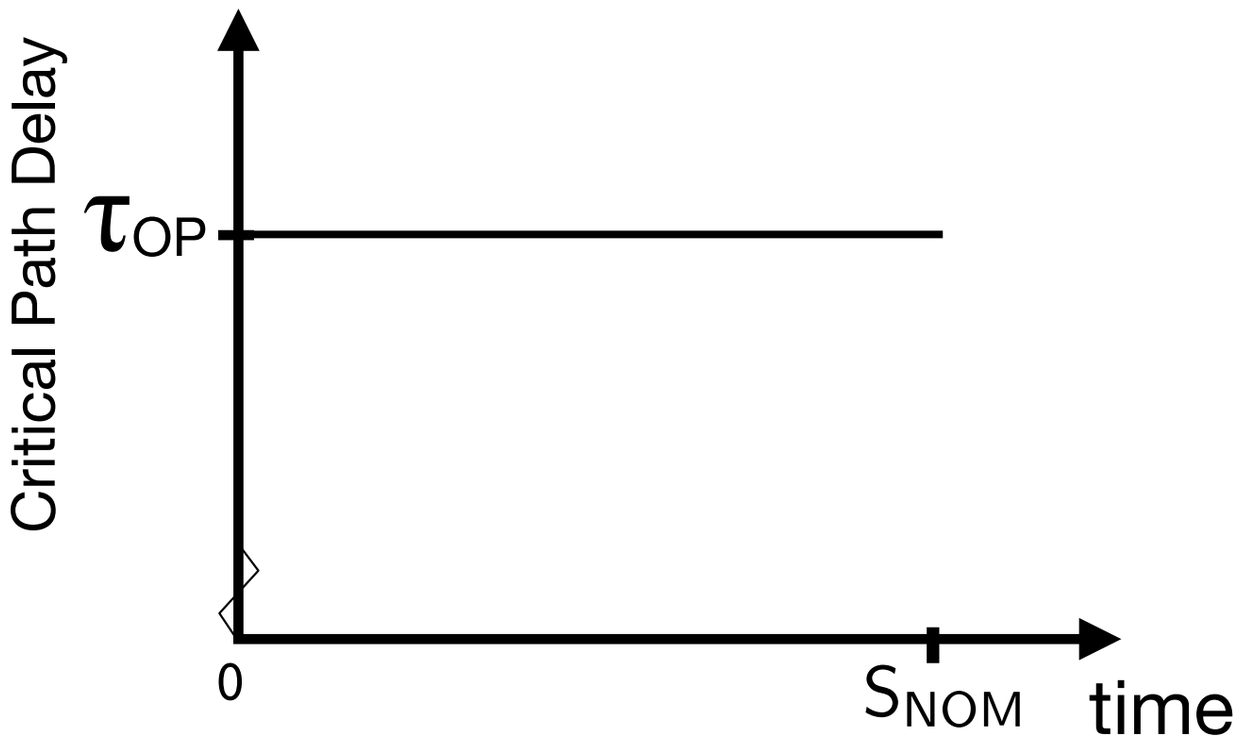


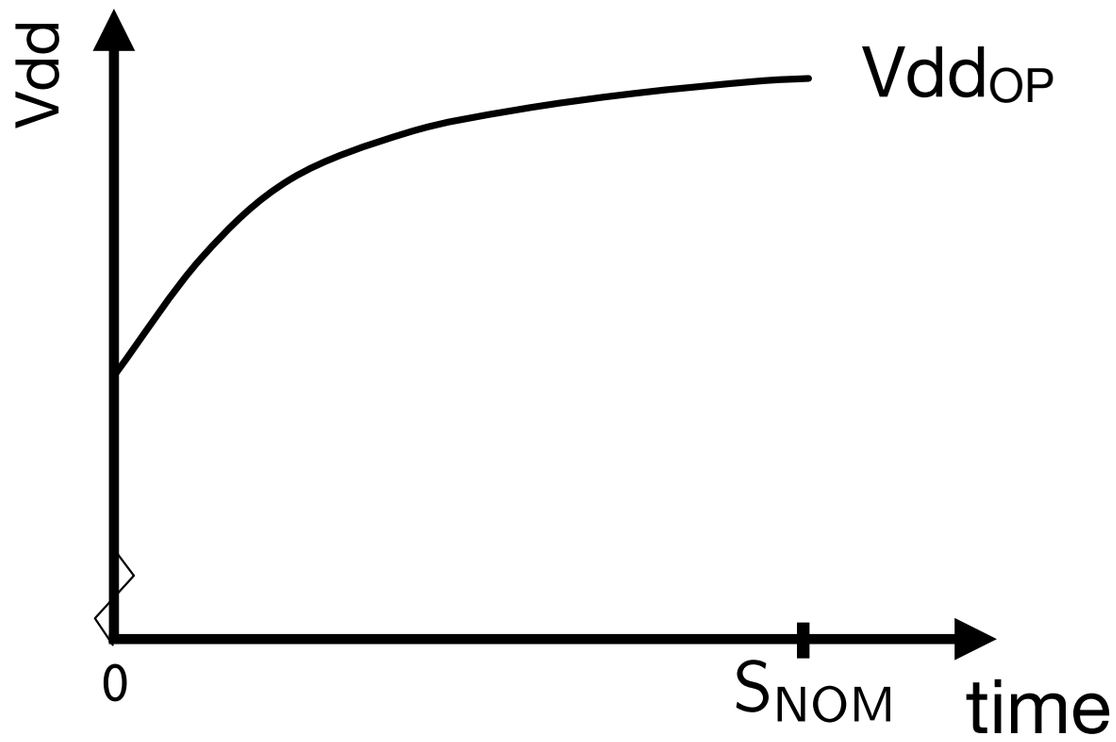

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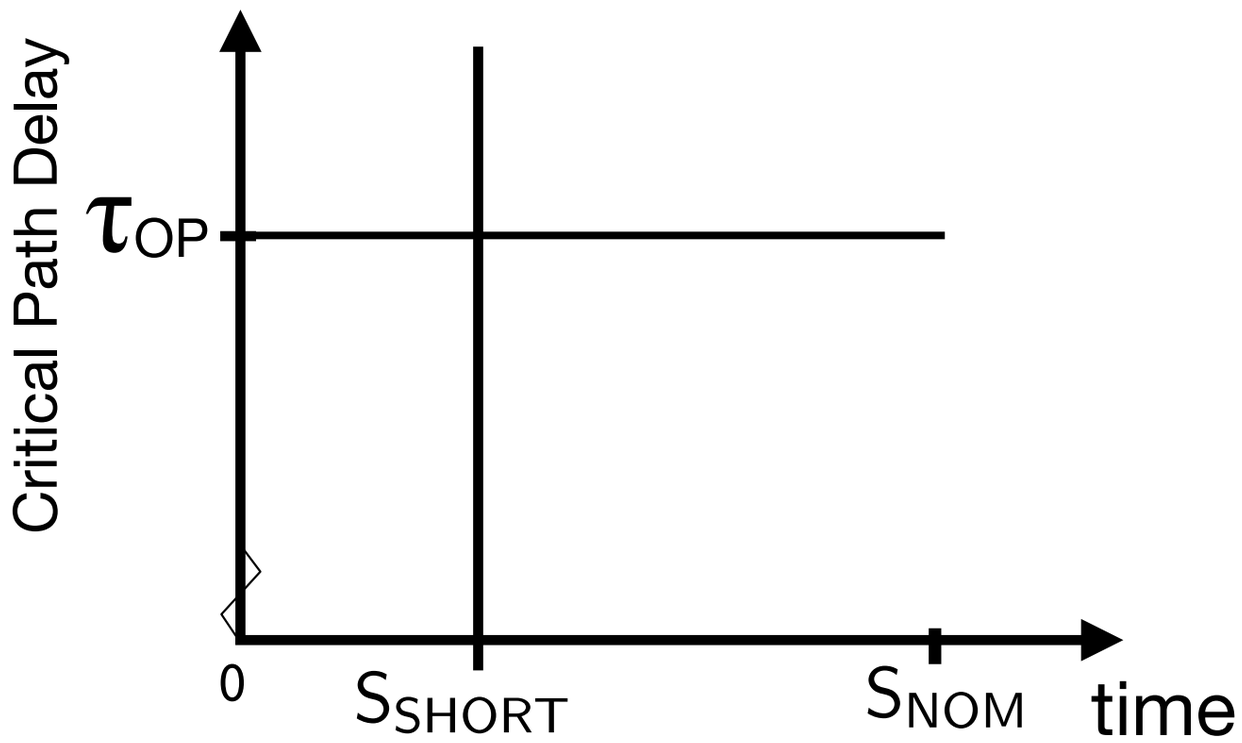


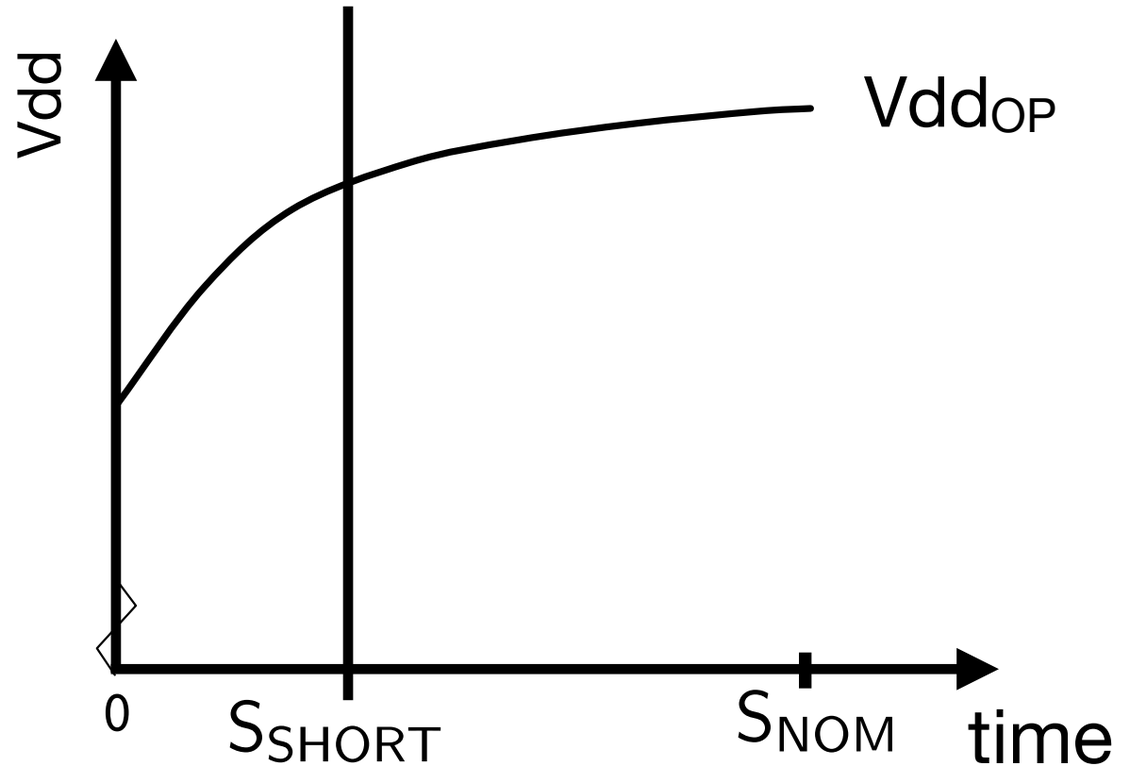

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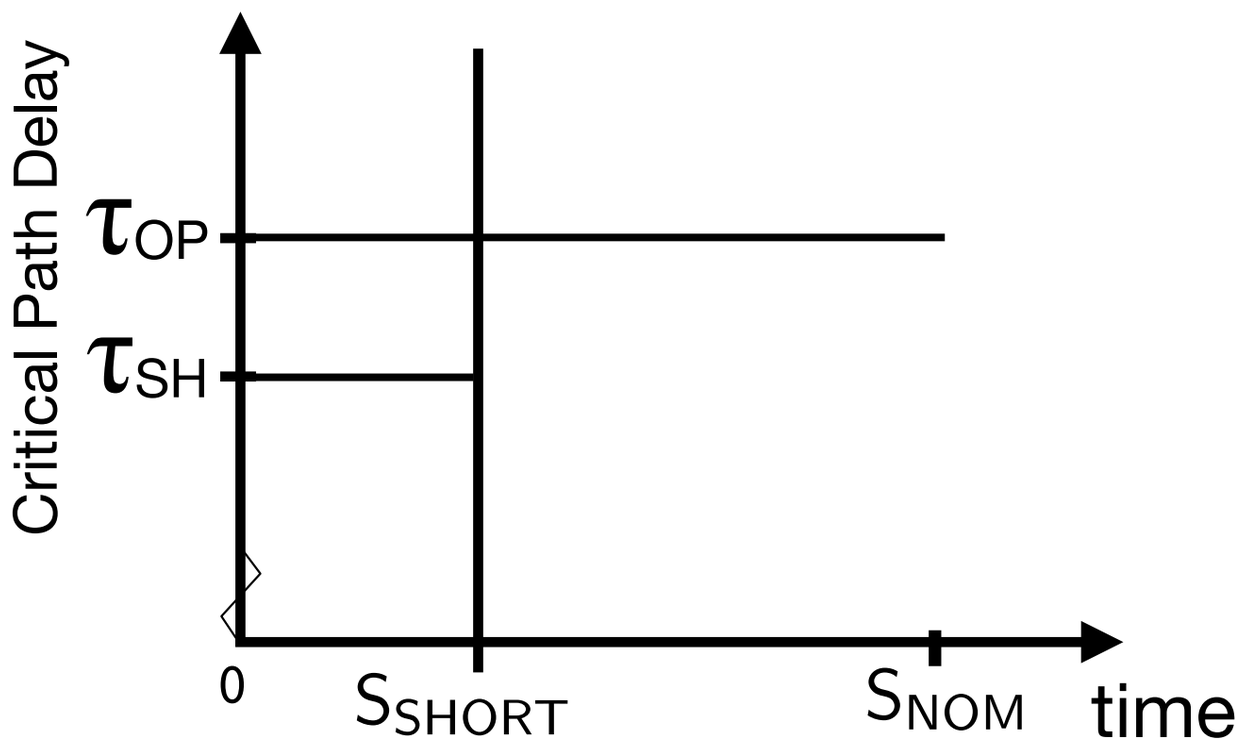


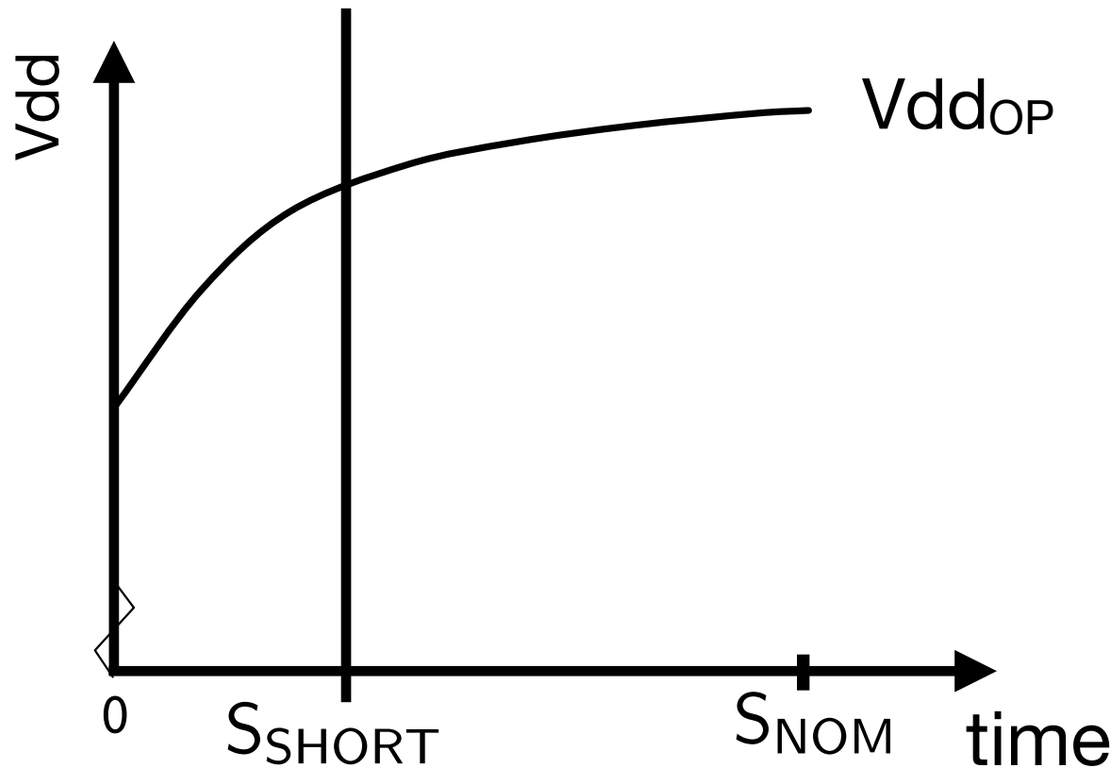

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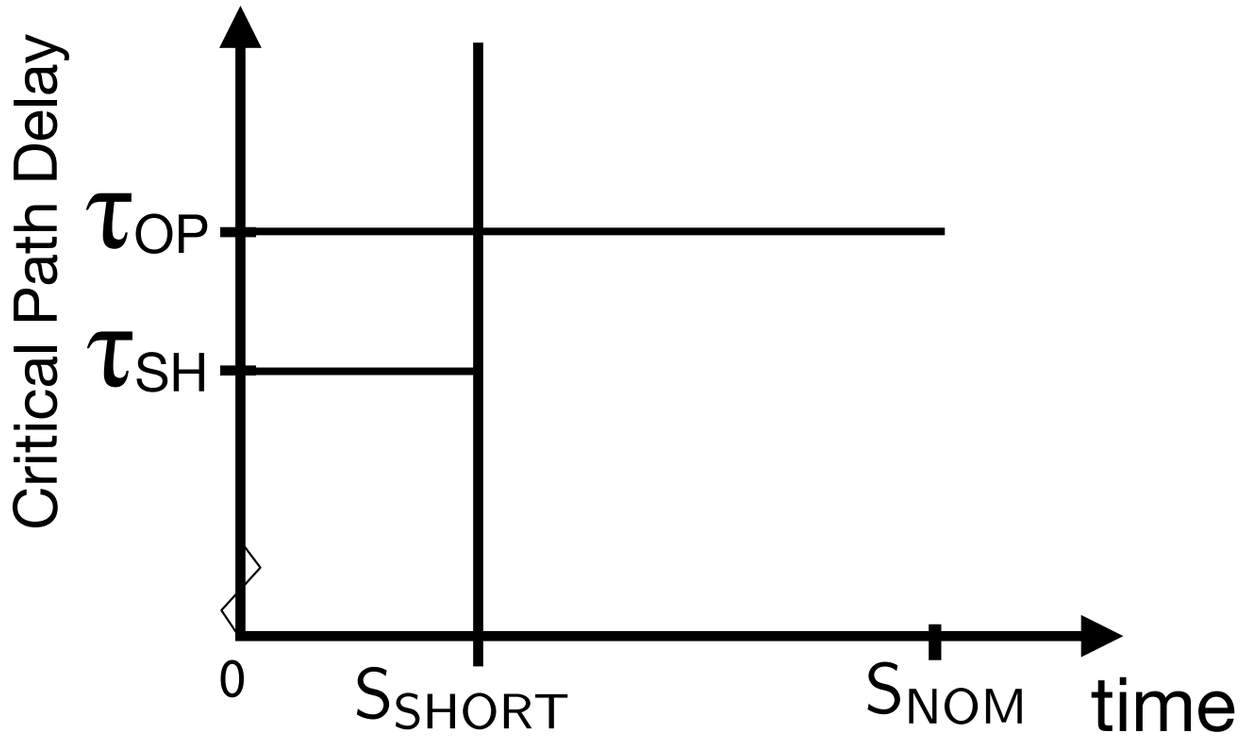


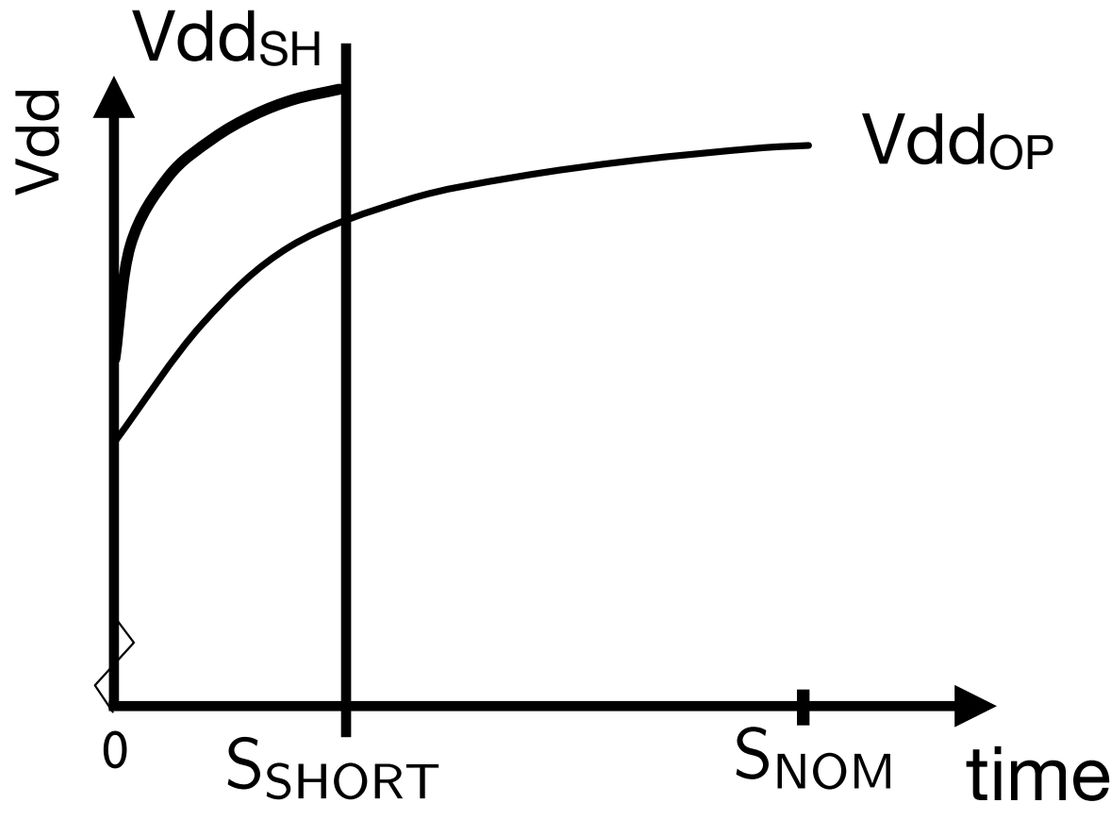

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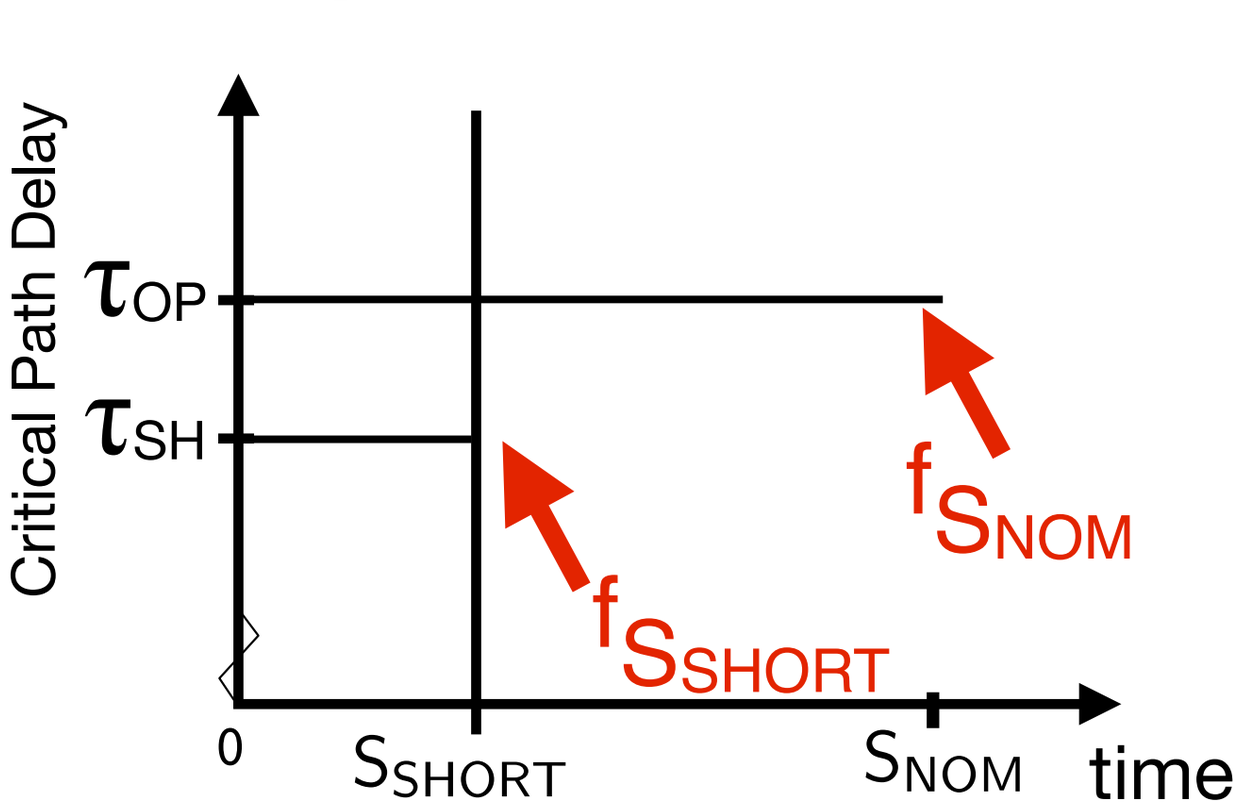
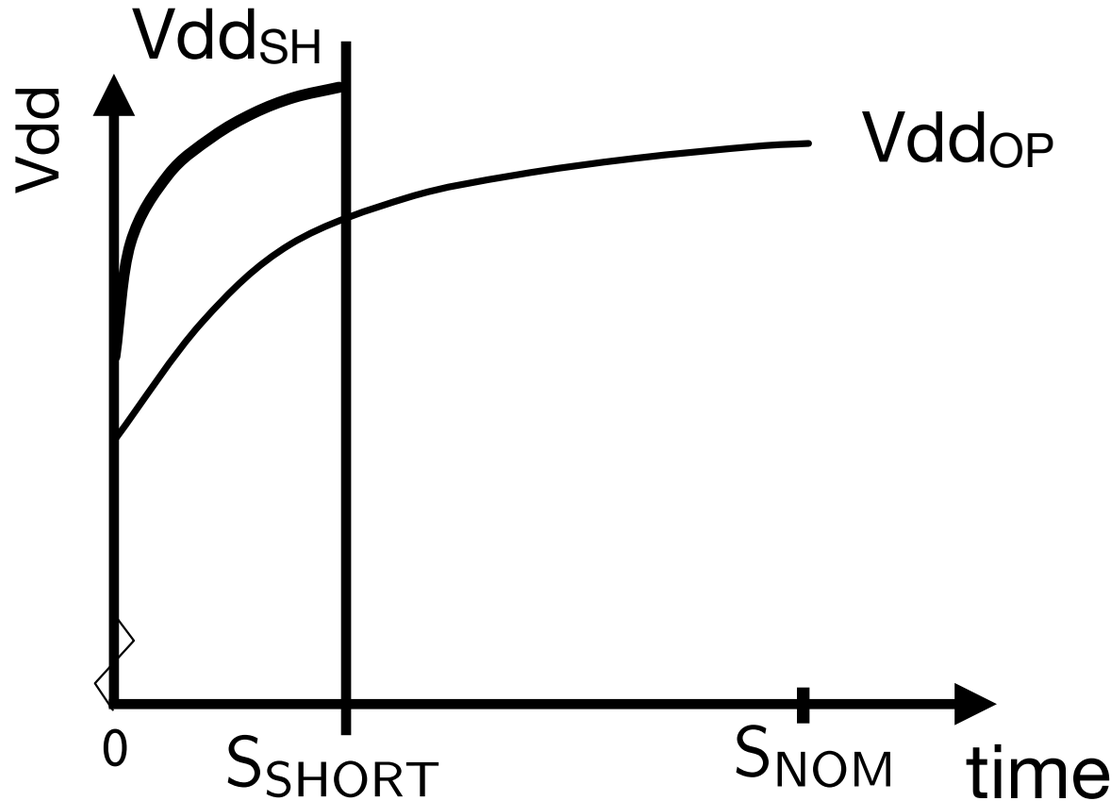
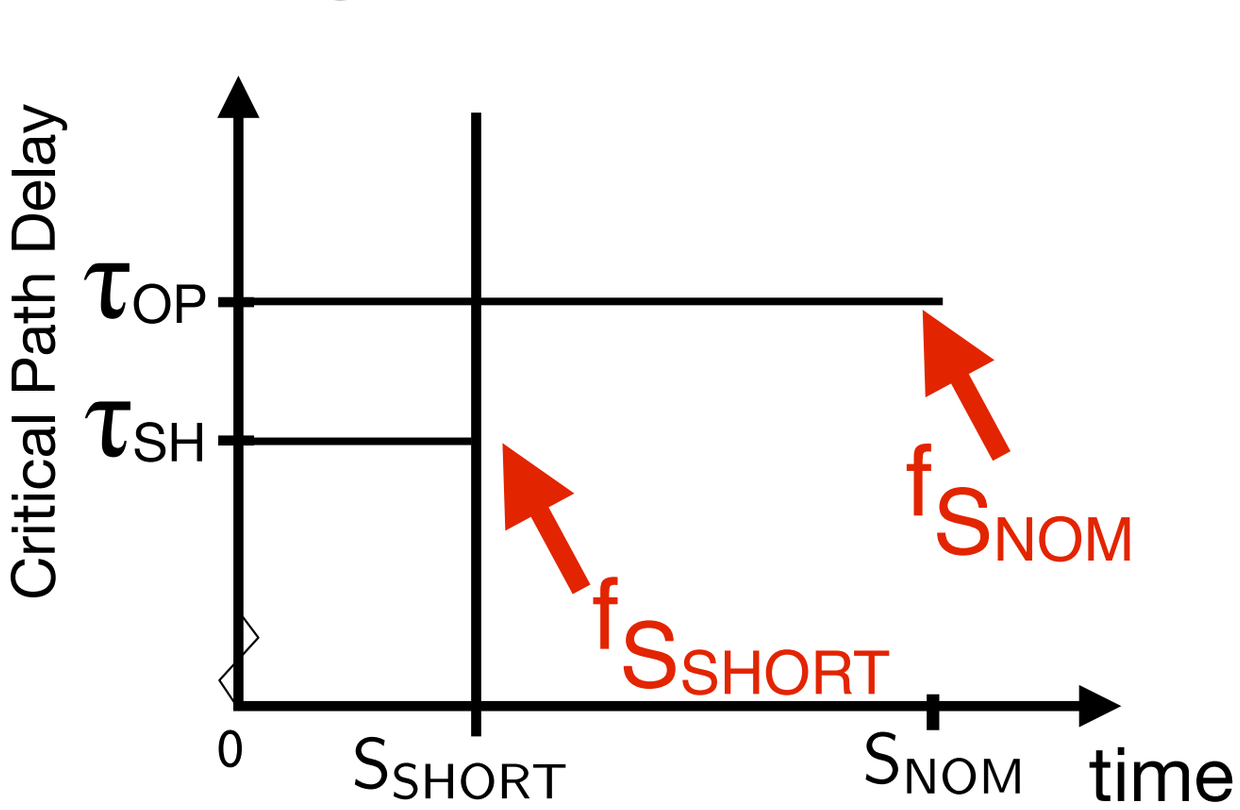


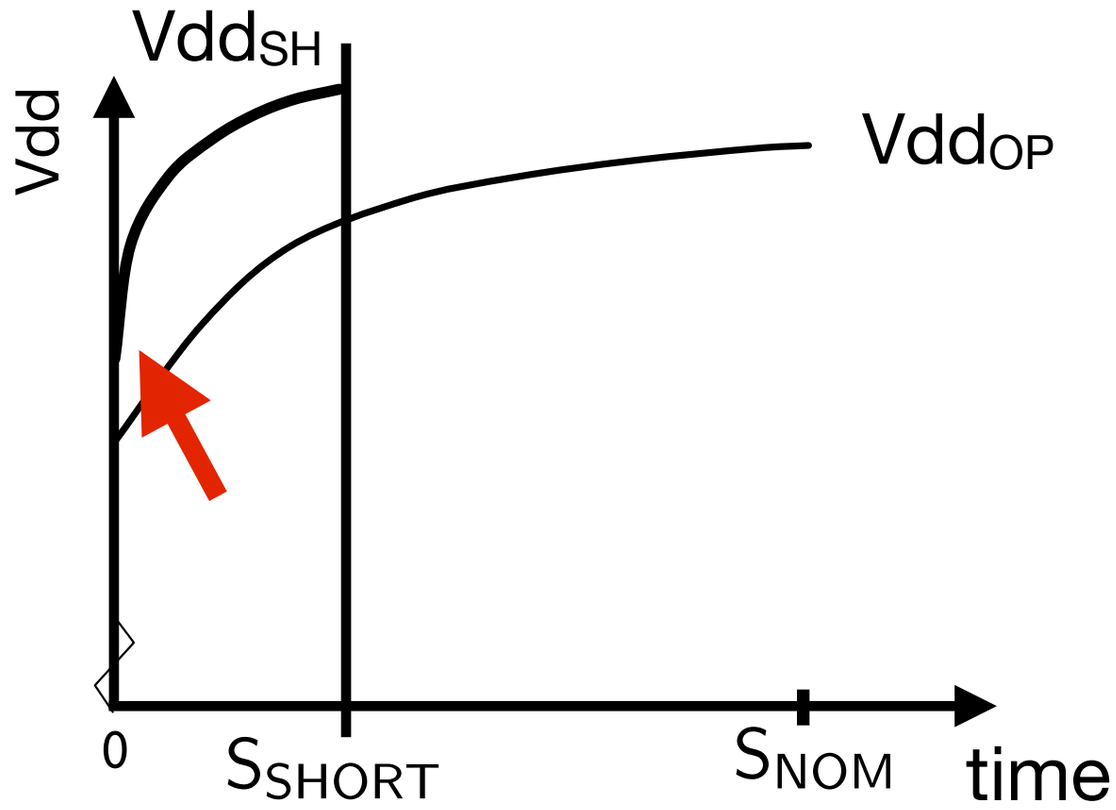




- Even higher frequency than DVSAM-Perf for short service life

# DVSAM-Perf for $S_{SHORT}$

Idea: Aggressive DVSAM-Perf for a short service life to get even higher performance

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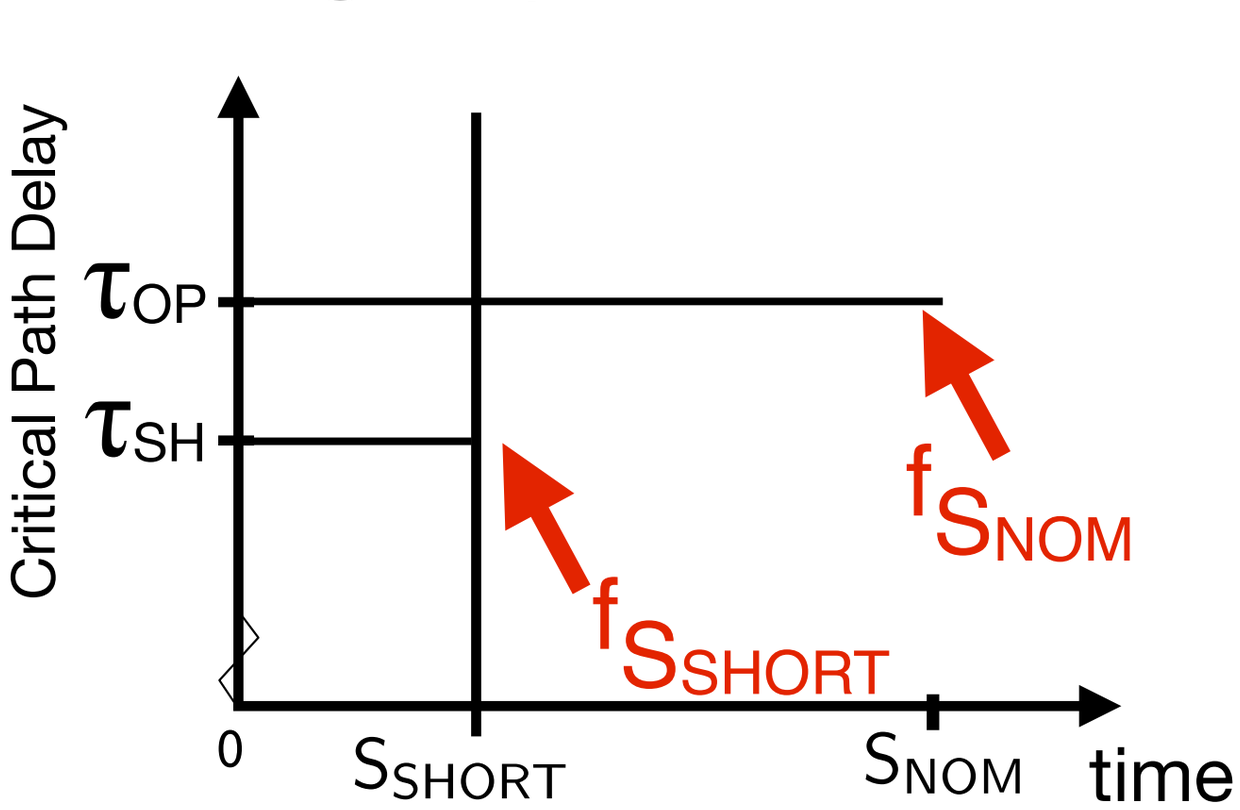


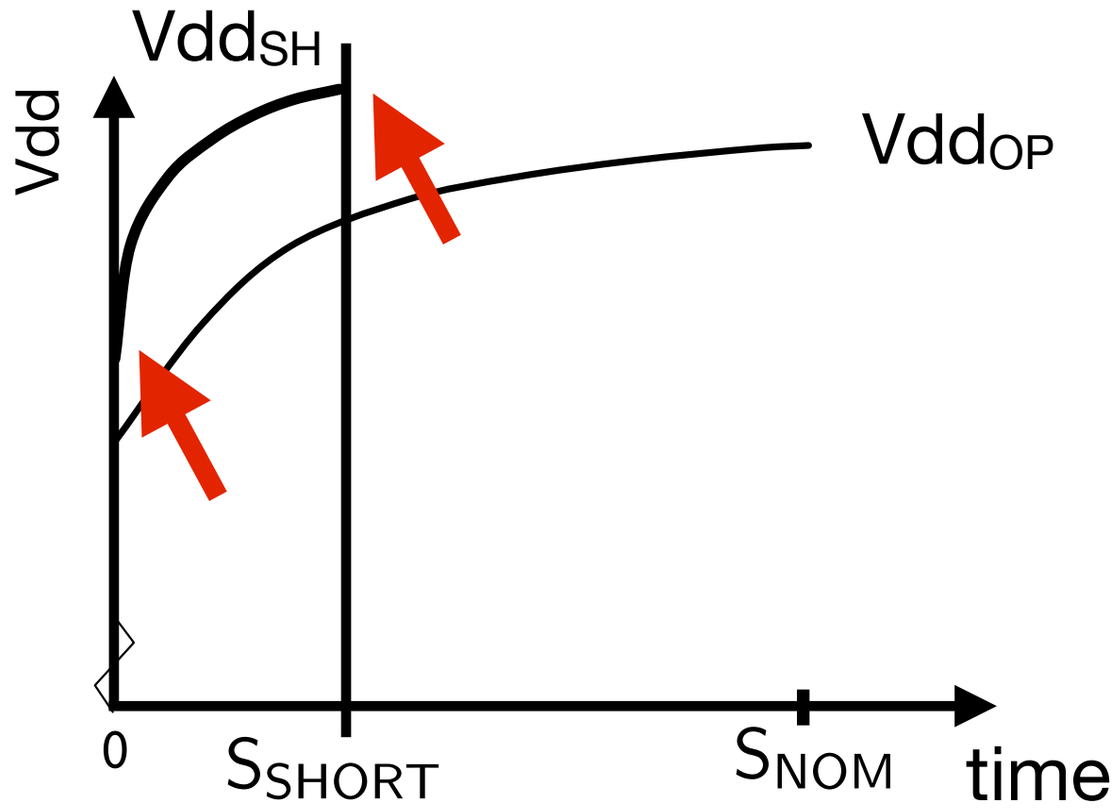


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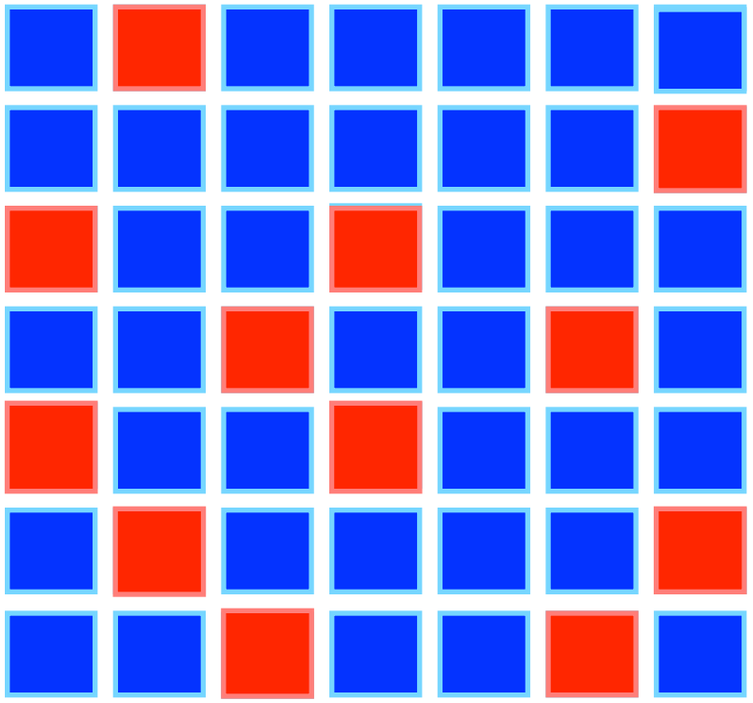
# BubbleWrap Environments

Throughput Cores



Expendable Cores

# BubbleWrap Environments

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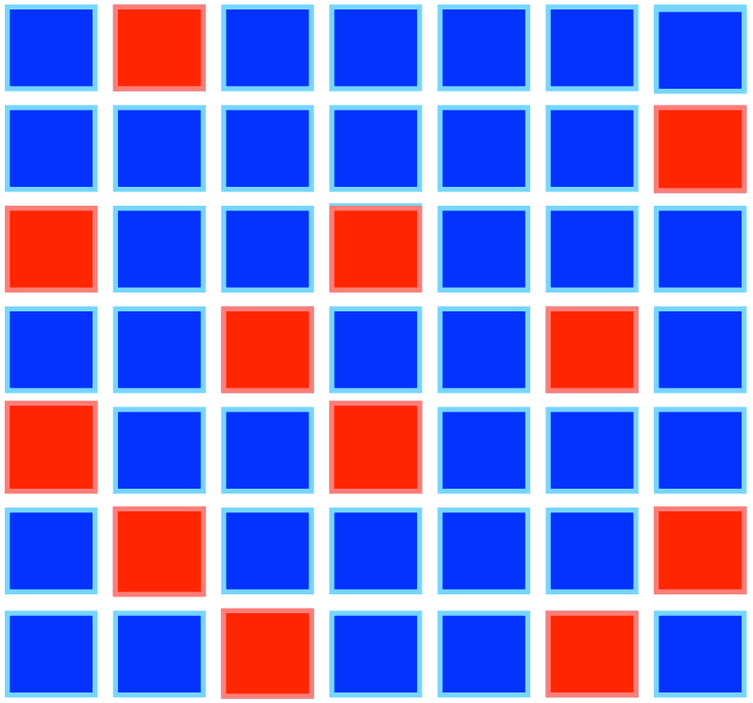

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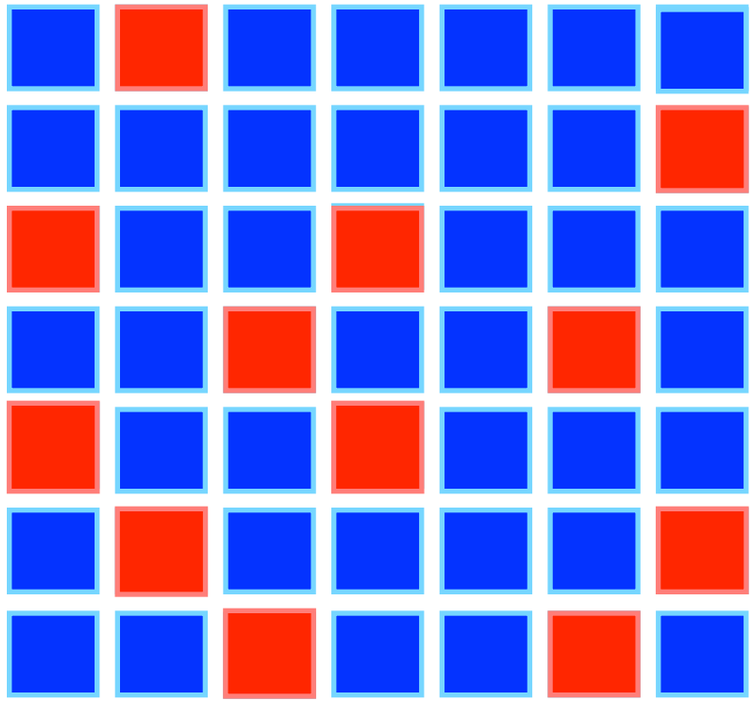

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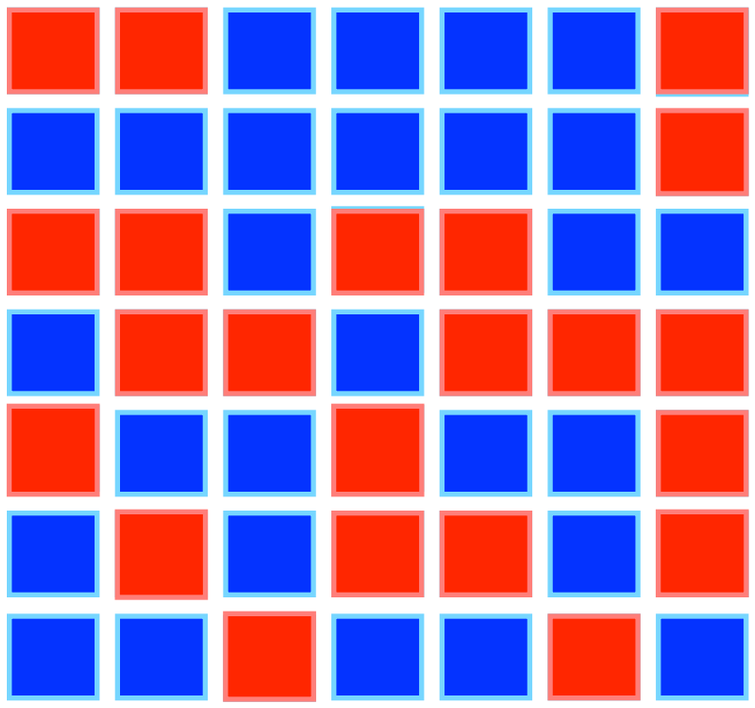

Expendable Cores

- Two choices for Throughput Cores
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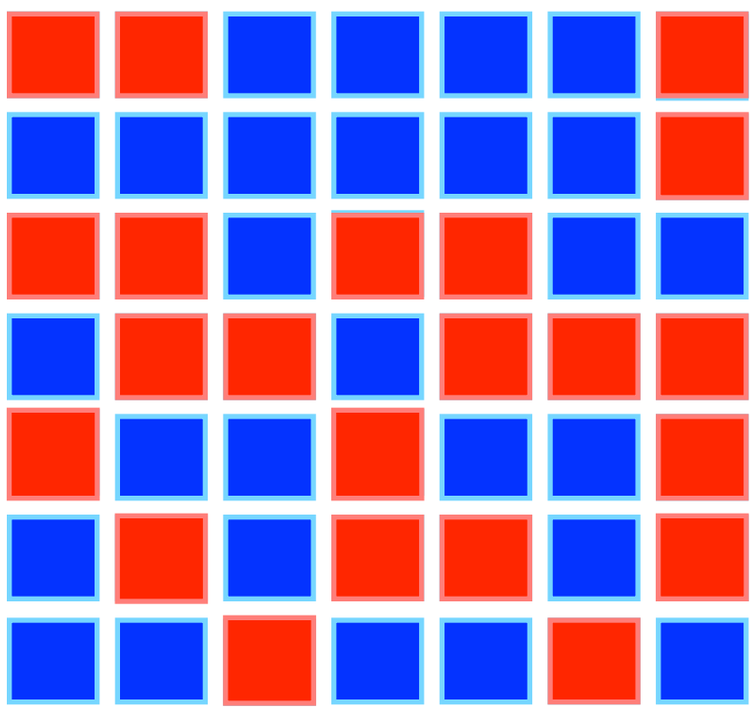


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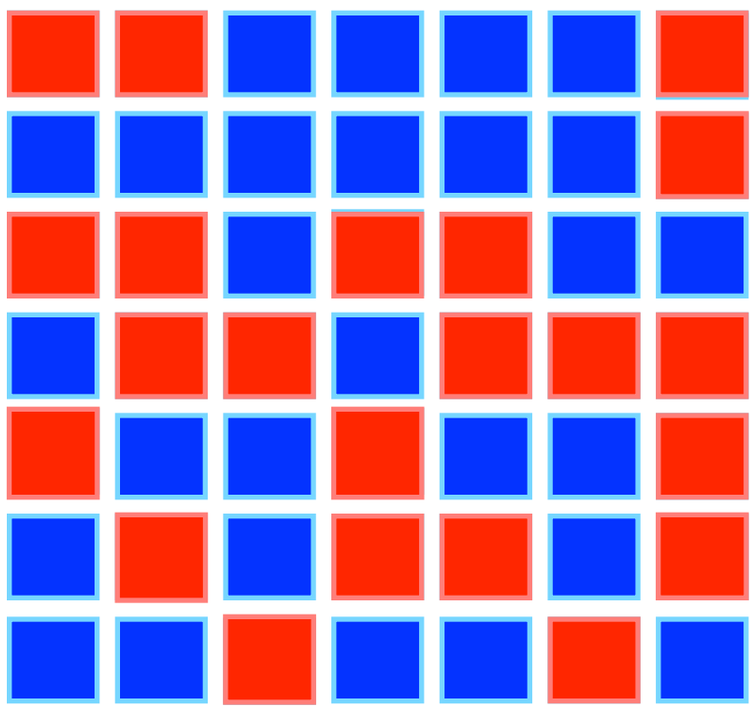


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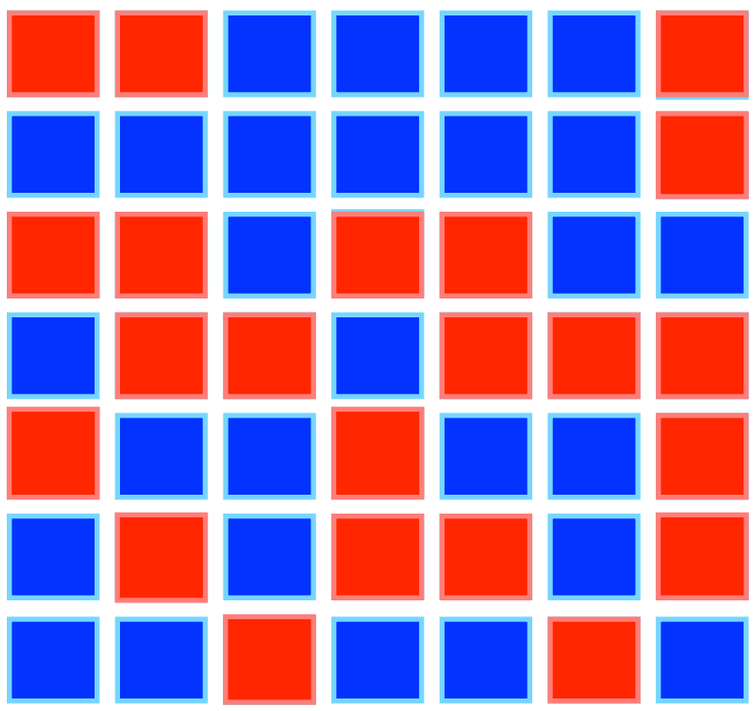


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- SESC enhanced by a power & thermal model

# Frequency Gains of Sequential Section

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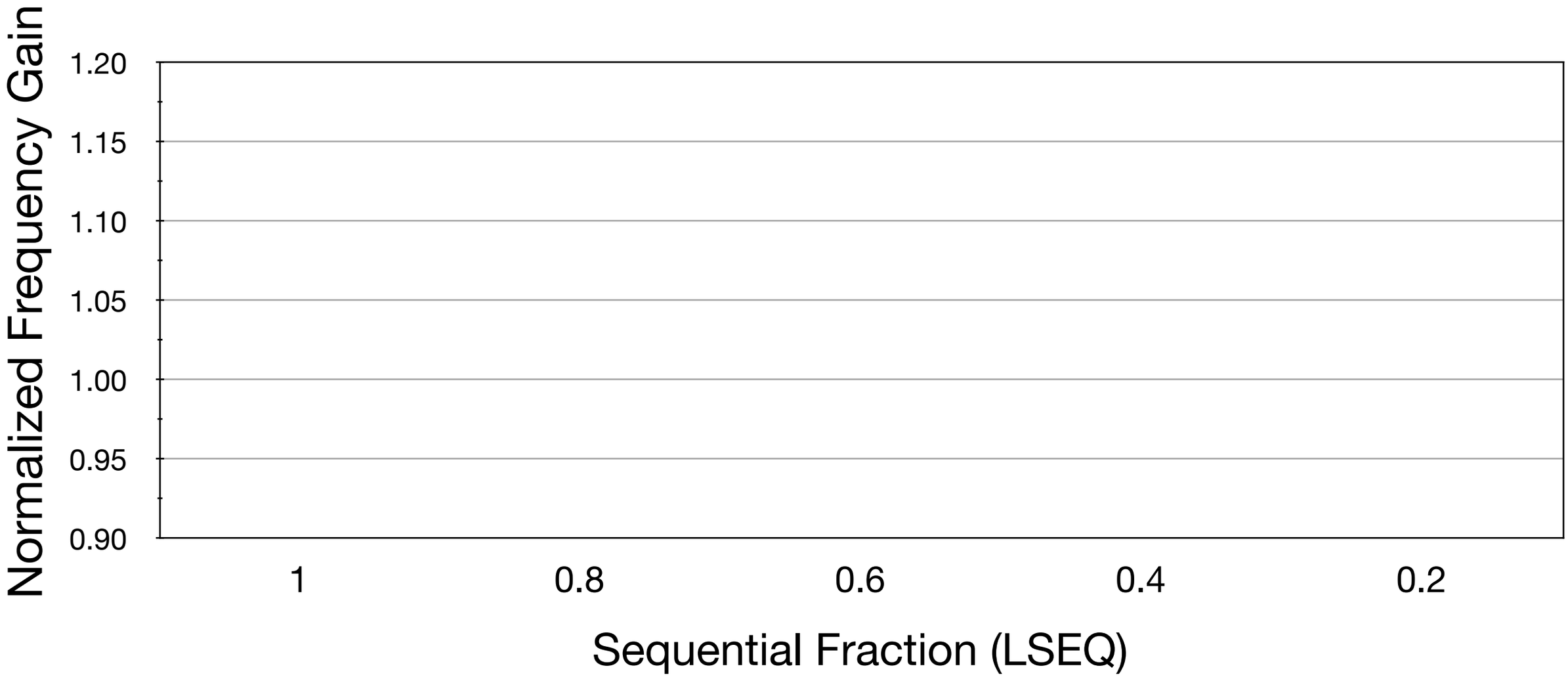

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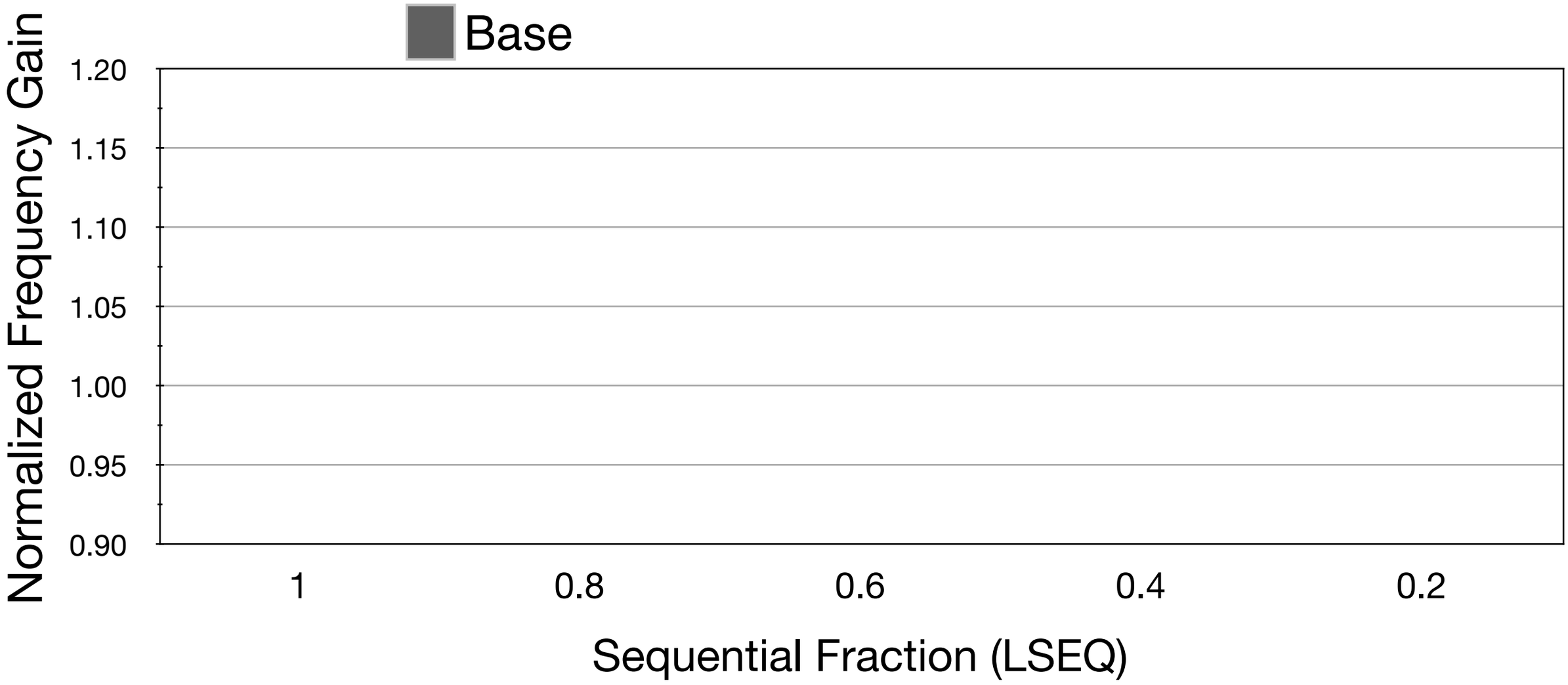

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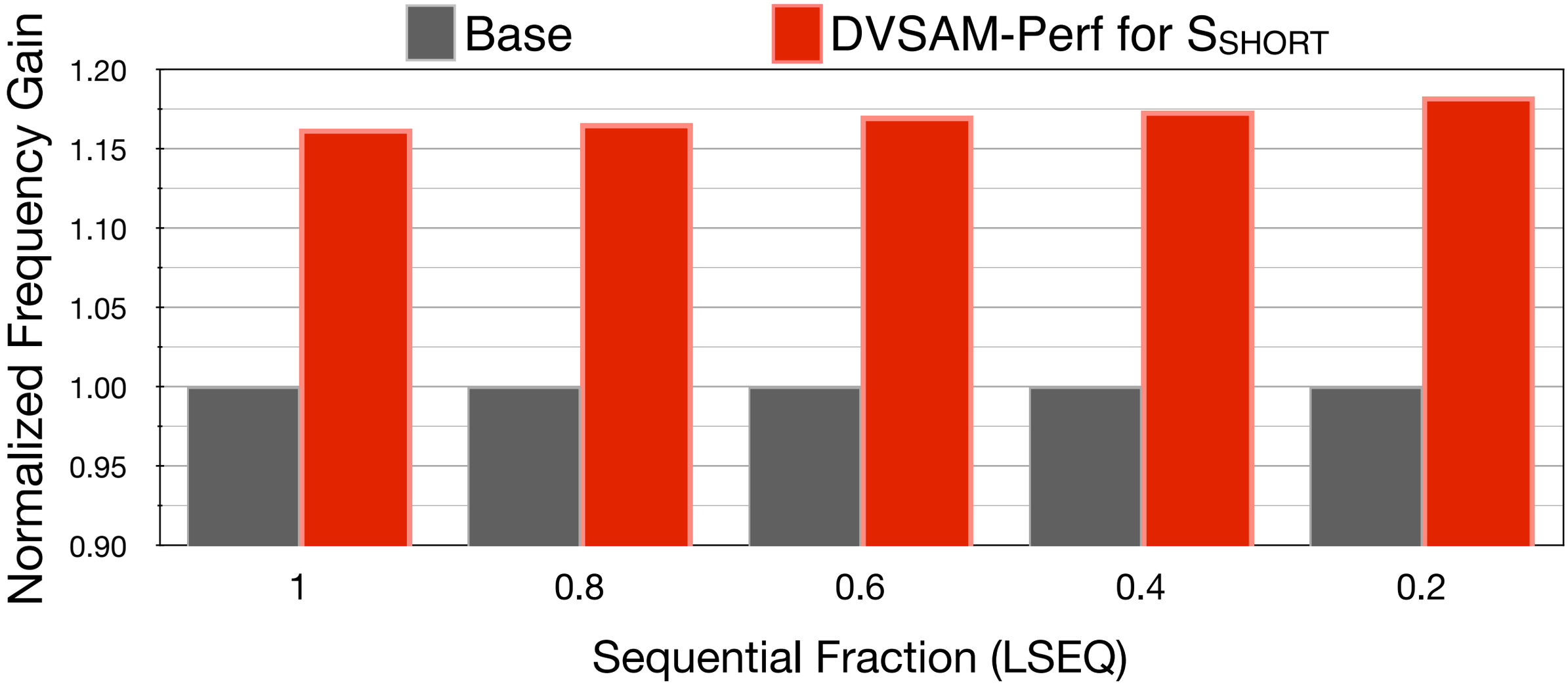

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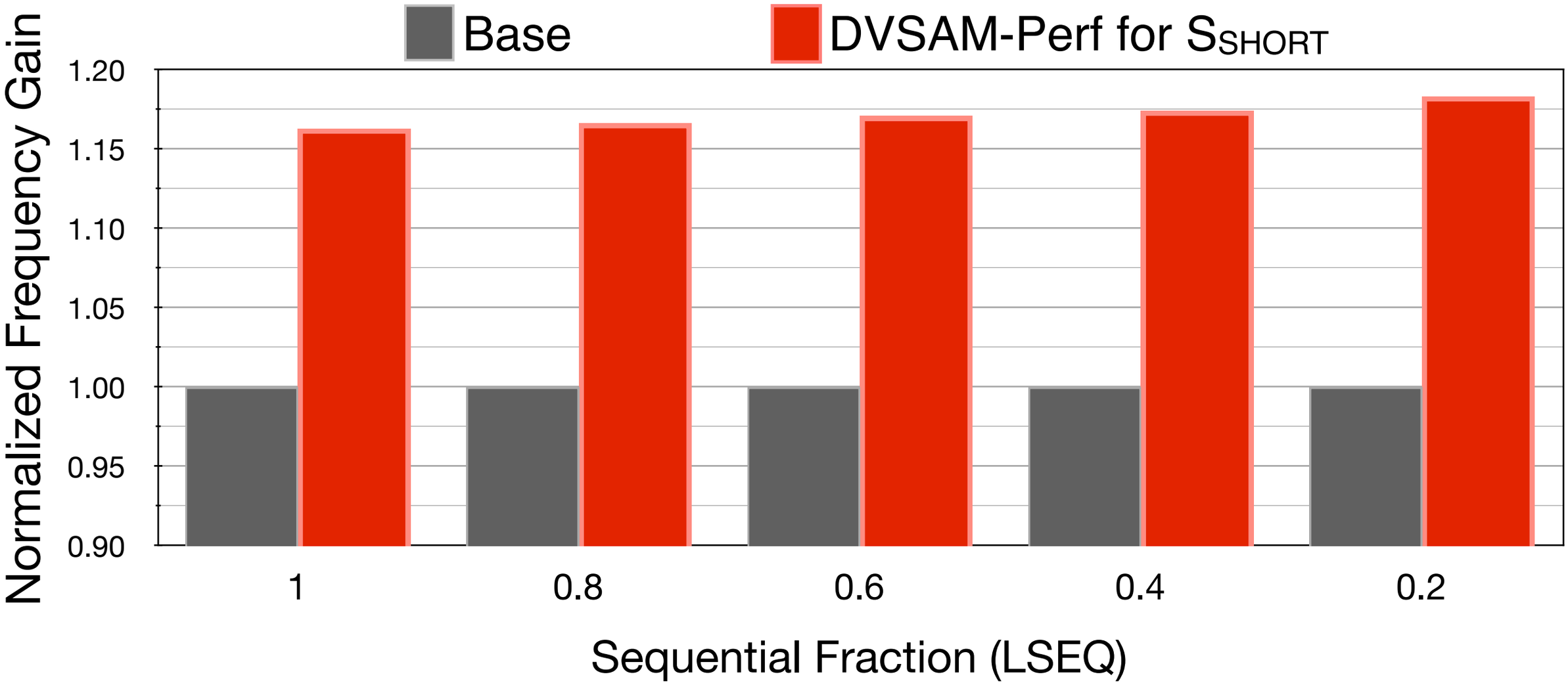


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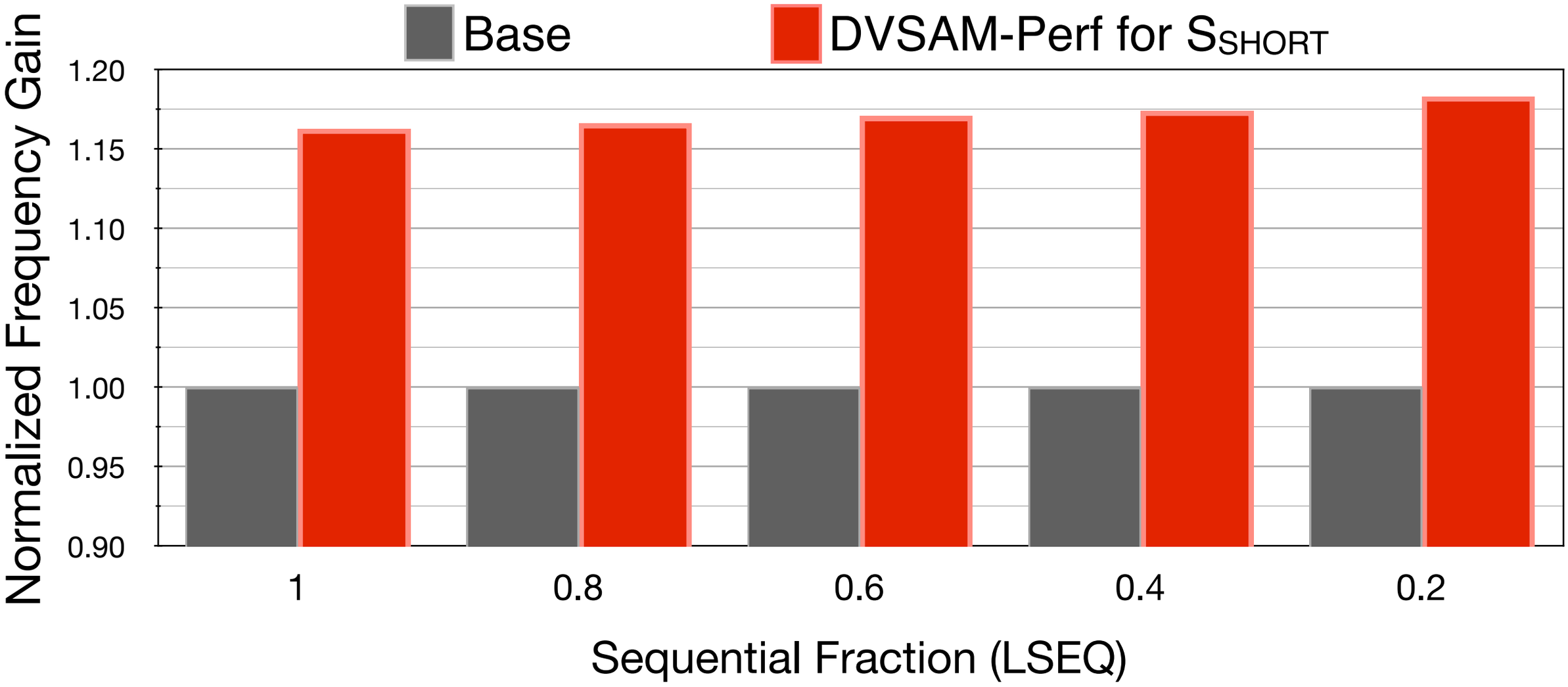


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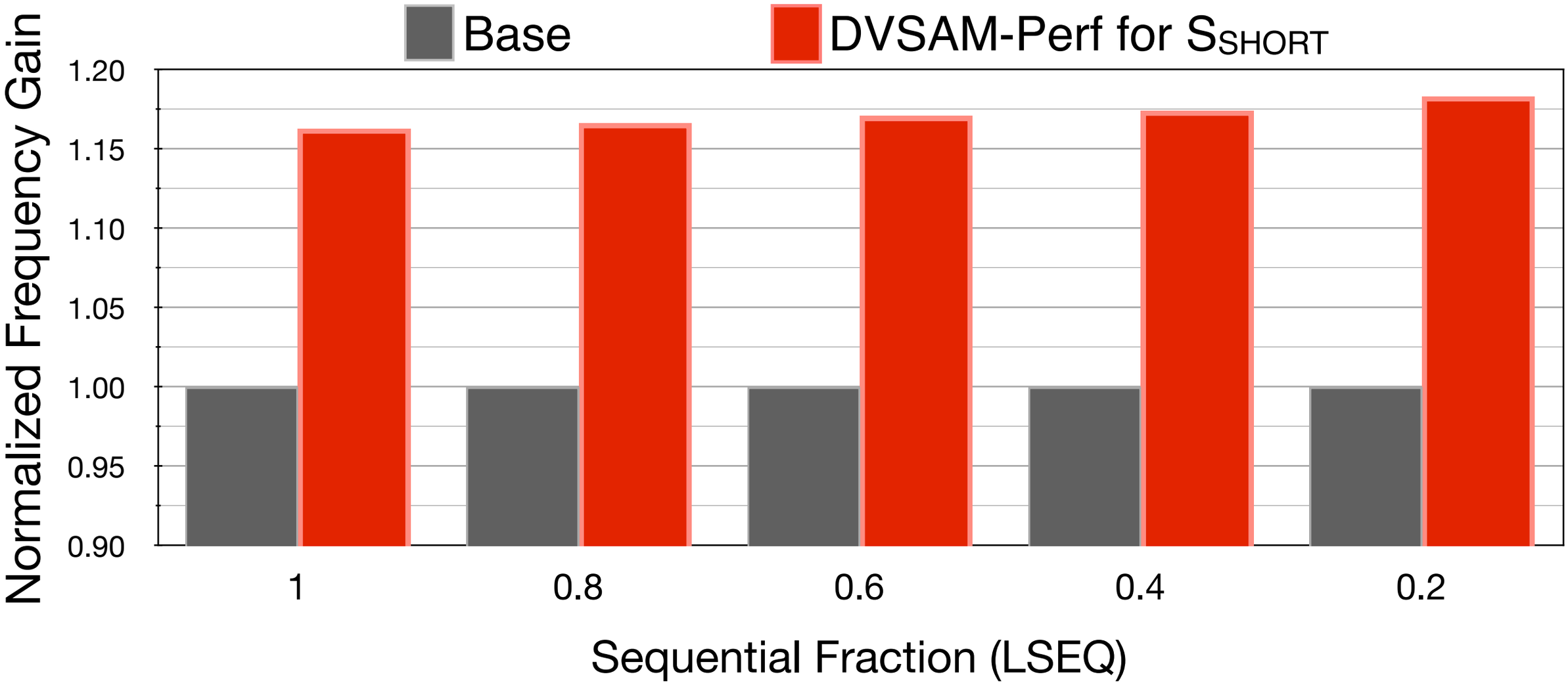


- Large f gains are feasible
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- For DVSAM-Perf, each expendable core runs for $L_{SEQ}/N_E$ x $S_{NOM}$

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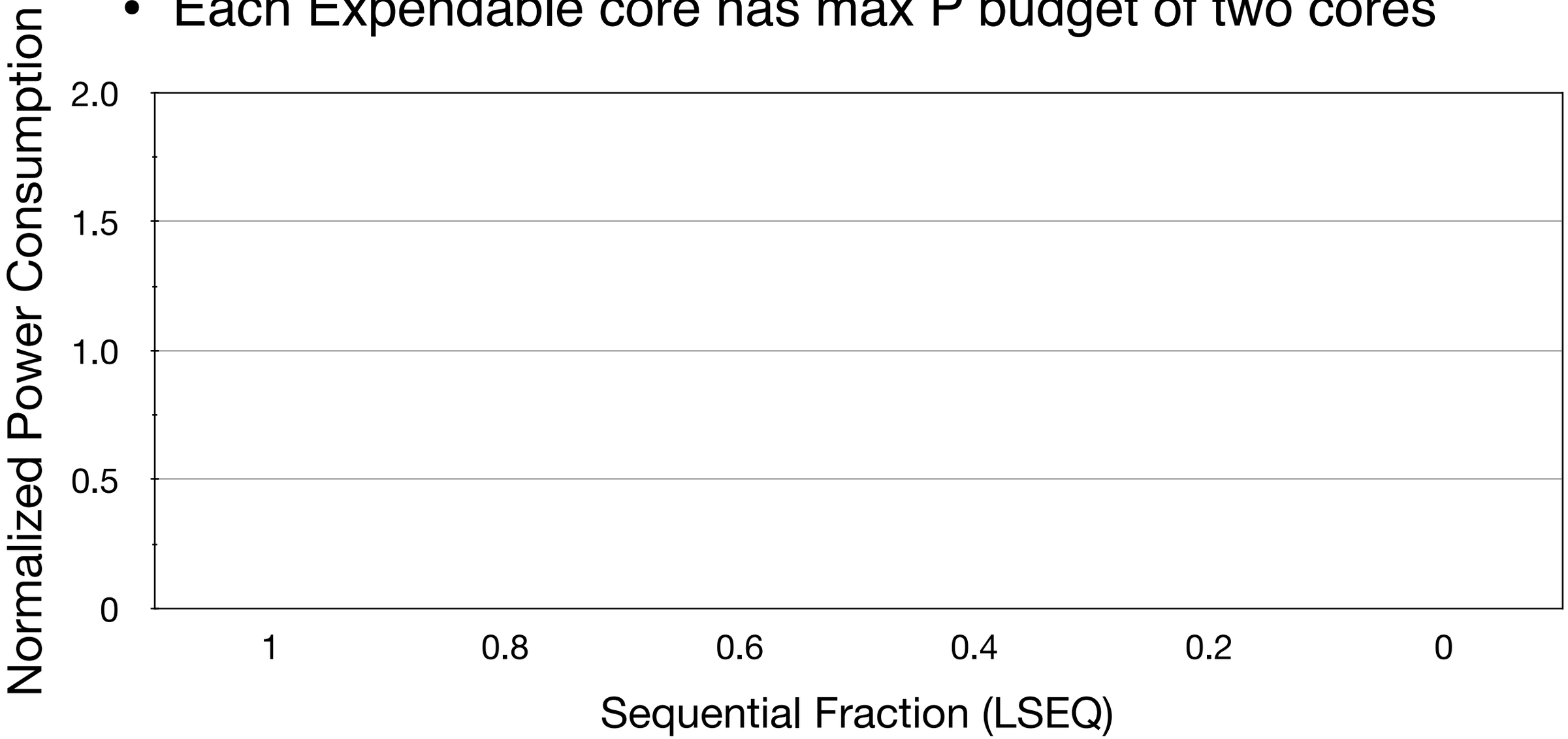

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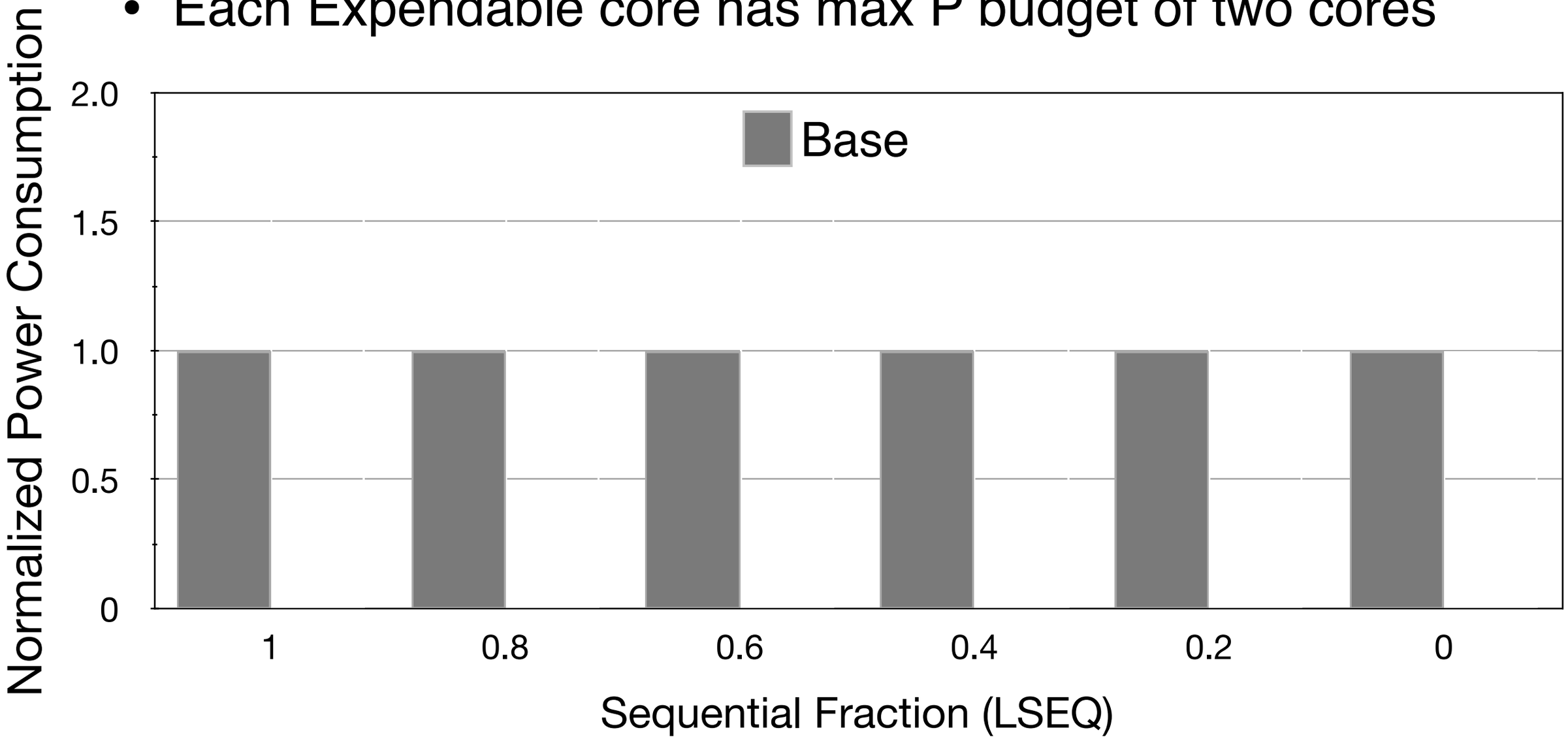

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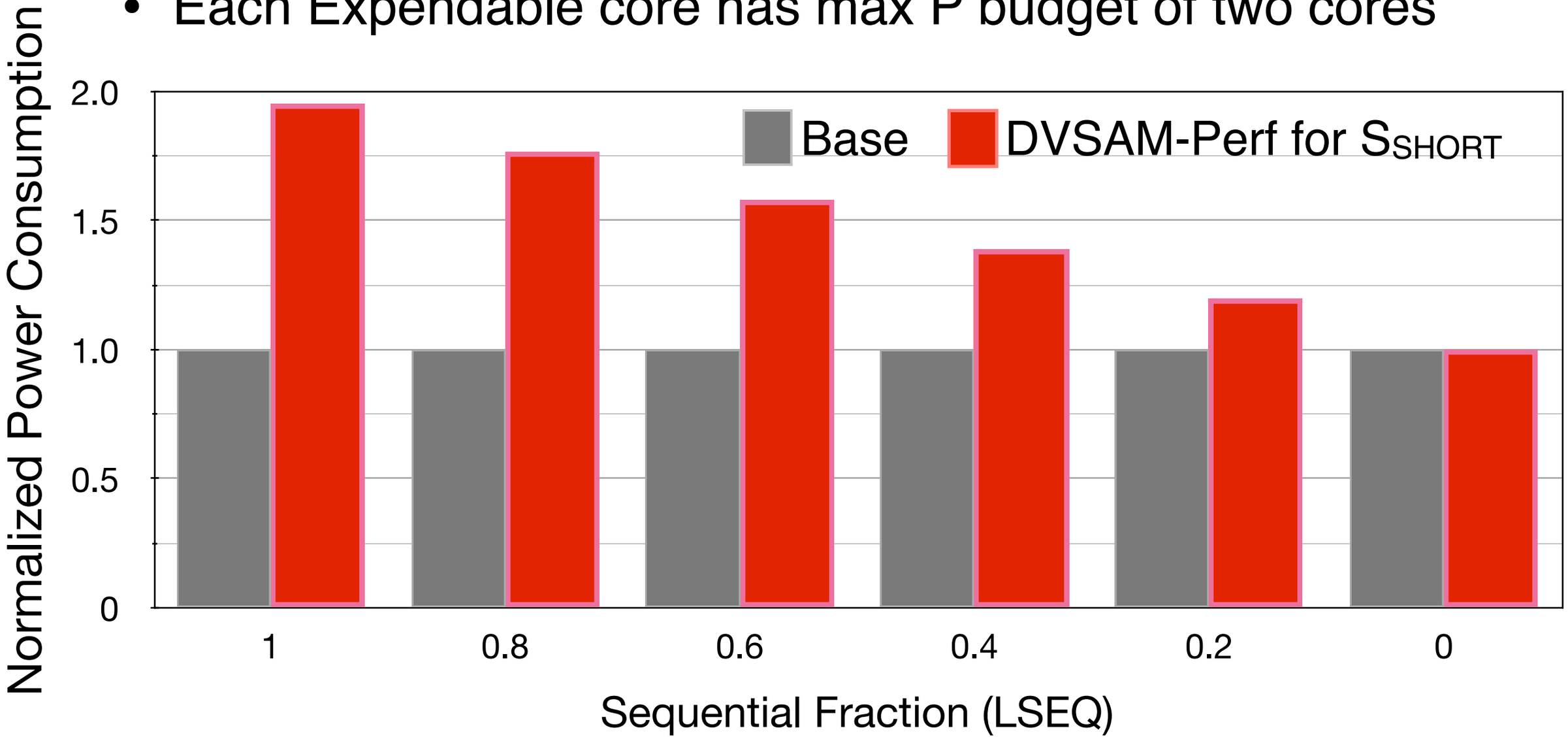

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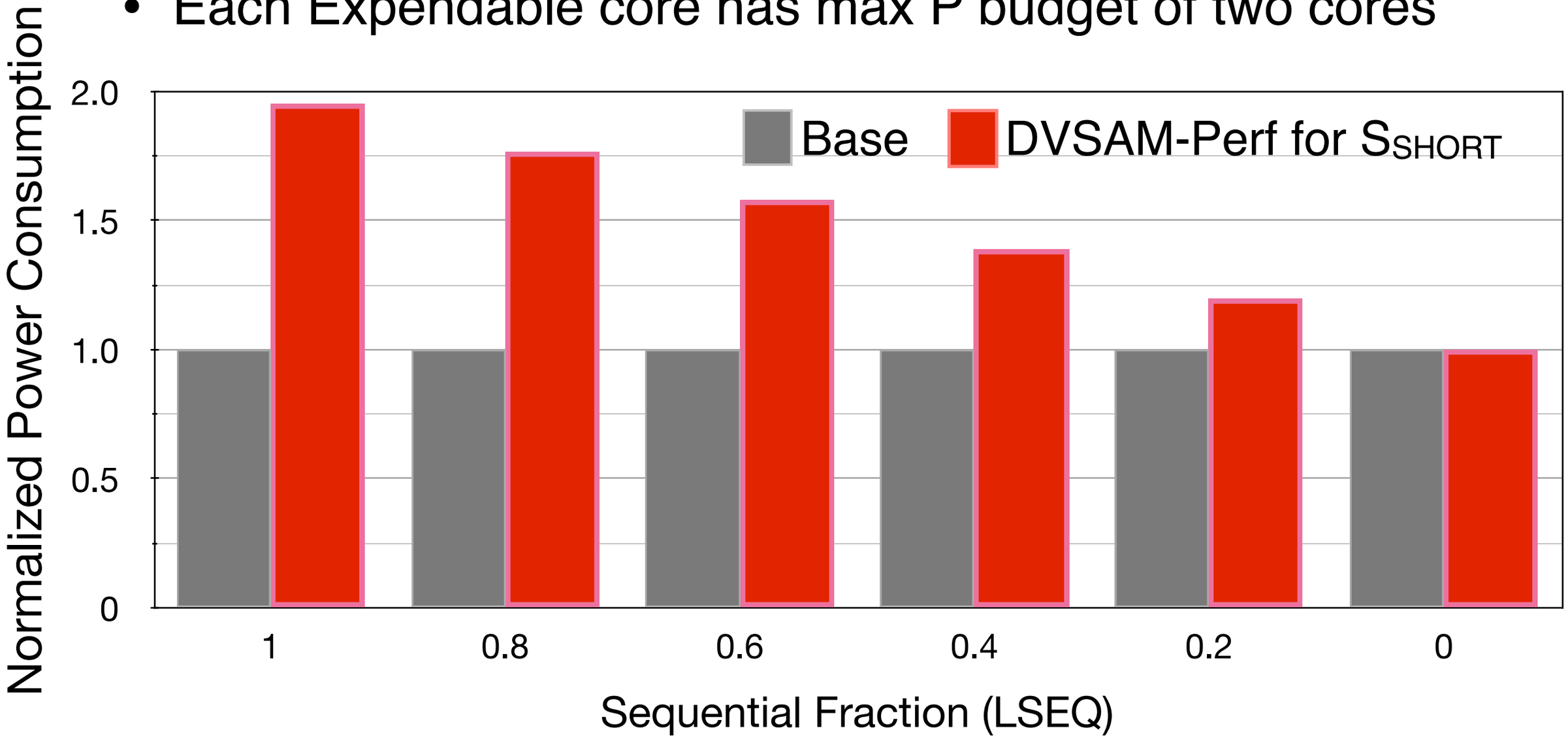
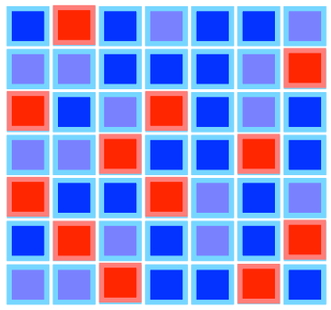



- Tolerable power cost for the frequency gains

# Conclusion

The BubbleWrap Many-Core:
Exploiting dormant cores for sequential acceleration



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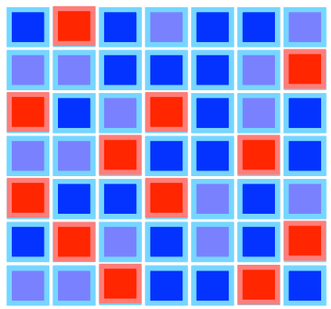

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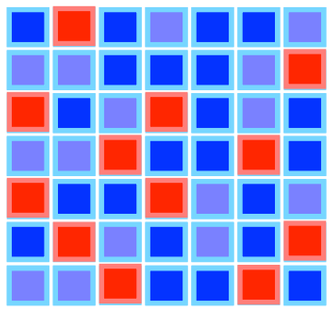

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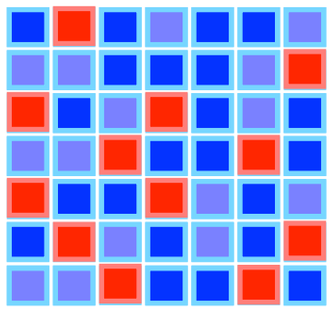

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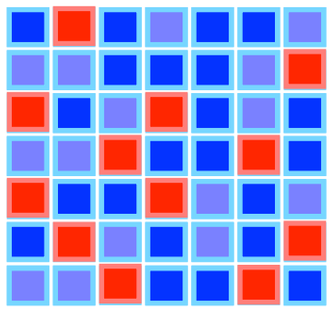

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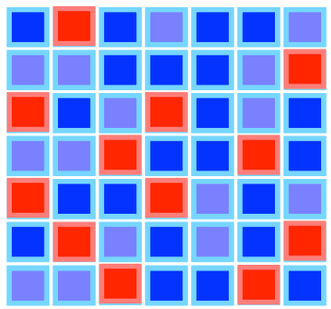

- Simple homogeneous design
- No architectural or software changes
- Improves sequential and parallel performance
  - Fully sequential applications at 16% higher f
  - Fully parallel applications at 30% higher throughput

# The BubbleWrap Many-Core:
## Popping Cores for Sequential Acceleration

**Ulya Karpuzcu**, Brian Greskamp, Josep Torrellas
University of Illinois

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