A holistic analysis of circuit performance variations in 3D-ICs with thermal and TSV-induced stress considerations

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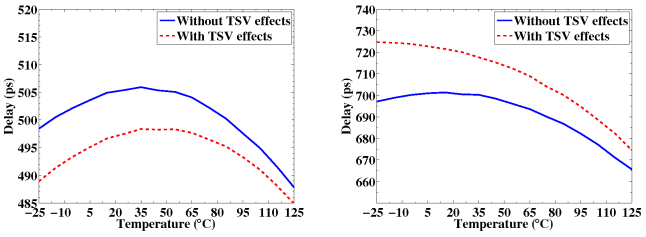
***Abstract*—In 3D-ICs, TSV-induced thermal residual stress impacts several transistor electrical parameters – low-field mobility, saturation velocity, and threshold voltage. These thermal-stress-related shifts are coupled with other temperature effects on transistor parameters that are seen even in the absence of TSVs. In this paper, analytical models are developed to holistically represent the effect of thermally-induced variations on circuit timing. A biaxial stress model is built, based on a superposition of 2D axisymmetric and Boussinesq-type elasticity models. The computed stresses and strains are then employed to evaluate transistor mobility, saturation velocity and threshold voltage. The electrical variations are translated into gate-level delay and leakage power calculations, which are then elevated to circuit-level analysis to thoroughly evaluate the variations in circuit performance induced by TSV stress.**

***Key Terms* : 3D-IC, Through Silicon Via, Static Timing Analysis, Finite Element Method**

I. Introduction

3D-IC technology, which allows vertical scaling by stacking chips together, provides significant benefits over conventional 2D-ICs, including reductions in critical wire lengths, higher transistor density per unit footprint, and heterogenous integration. However, a major issue with 3D-ICs is that on-chip temperature variations can be significant. On-chip temperatures can affect the behavior of a 3D-IC in several ways. *First*, thermal effects can change the threshold voltage and carrier mobilities in a transistor. The former serves to speed up the circuit while the latter slows it down: one or the other effect may dominate at a specific temperature. As a result, a circuit may show either positive temperature dependence (PTD) where the delay decreases monotonically with temperature, negative temperature dependence (NTD) where it increases monotonically, or mixed temperature dependence (MTD), where it changes nonmonotonically [1]. *Second*, through-silicon-vias (TSVs), which connect different wafers/dies in a 3D-IC, induce a thermal residual stress in silicon, and cause changes in device electrical parameters. The transistor mobilities are affected by stress due to piezoresistivity; threshold voltages are impacted by stress-induced shifts in electronic band potentials; carrier saturation velocities are altered due to stress-induced quantum mechanical effective mass of charge carriers in transistor channels (these are shown to be correlated with the changes in low-field mobility [2]). The magnitude of stress-induced electrical variations in 3D-IC transistors is dependent upon the distance of the devices from the TSVs and the transistor channel orientation with the crystallographic axis.



(a) (b)

Fig. 1. Delay dependence of benchmarks (a) ac97_ctrl and (b) usb_funct for the cases where TSV effects are ignored and taken into account.

To understand the delay variation with temperature in 3D circuits, a holistic analysis must be conducted, considering both the above effects. This variation of delay with temperature is shown for two sample benchmark circuits in Fig. 1. In each plot, the solid curve shows the trend without TSV effects, which shows MTD effects similar to those reported in [1] in both cases. Under TSV stress effects, the delays change and the temperature dependence is altered, as shown by the dotted curve. While the circuit ac97_ctrl shows MTD effects, PTD effects dominate for usb_funct. Moreover, in one case the delays decrease, while in another, they increase. However, the relative deviation between dotted and solid curves diminishes with temperature. Prior approaches [3]–[5] have considered TSV stress effects ignoring the inherent effects of temperature on mobility and threshold voltage, and have assumed that the worst-case delay occurs at the lowest temperature: as seen above, this is not always true.

The TSVs may be made of copper, tungsten, or polysilicon: copper is the primary choice owing to its low resistivity. During manufacturing, the TSV is embedded in silicon after several thermal cycles and a final annealing process. During annealing and subsequent cooling, the structure undergoes a thermal ramp from about $250°C$ down to room temperature. Because of the difference in the coefficient of thermal expansion (CTE) of the copper TSV and the silicon, a residual thermal stress is induced in the region surrounding the TSV.

Often a thin dielectric liner layer is grown between the sidewalls of the copper TSV and silicon. Two primary choices of the liner material are silicon dioxide (SiO_2) and benzo-

cyclobutene (BCB). The liner layer improves the mechanical reliability of the copper TSV and reduces the magnitude of stress in silicon. Thus the amount of stress in silicon also depends upon the mechanical properties of the liner layer.

Stress in 3D-IC structures has been studied using the finite element method (FEM) and through analytical methods [4], [6], although these works did not consider the impact on circuit delays. FEM simulations can capture the finite geometries of the TSV structure (TSV+liner+silicon), and the differences in the material properties. Thus, they yield accurate estimates of stress levels around a TSV, but the computational cost of evaluating this stress data at different temperature corners for a given layout becomes quite prohibitive. FEM-based precharacterization approaches [7] are faster, but need significant storage to store the results of simulation on a grid with large number of points, and the fact that PTD/NTD/MTD requires such stresses to be stored at multiple temperature points. In contrast, an analytical approach lends to faster computation with no additional storage requirement since the stress at any point in the layout can be computed on-line.

The analytical model in this work uses a 2D axisymmetric model to obtain the thermal stresses in silicon taking into account the material property differences. However, the 2D approach does not mimic the traction-free surface condition (zero normal and tangential stress components) over the TSV and the liner as observed in the FEM. Thus a compensating pressure is applied over the TSV and the liner regions to recover the traction-free condition at the surface. The resultant stress distributions in silicon can be obtained using classical Boussinesq problem technique in elasticity [8]. This approach was used in [9] to study the copper TSV interfacial reliability but relies upon a numerical approach. In this work, a compact analytical model for stresses in silicon is developed using a combination of 2D and Boussinesq-type solutions. Furthermore, we show that TSV-induced stress is biaxial in nature. Prior work in [5] uses a uniaxial model for TSV-stress which incurs significant errors in mobility computations [10].

Based on the stress models, we derive a complete analytical model for delay and leakage power variations under stress. Our contributions are as follows:

- We incorporate both sets of thermal effects into a single analysis, capturing TSV stress effects, and thermally-driven low-field mobility and threshold voltage variations. The variations in saturation velocity can be empirically expressed in terms of low-field mobility variations. In contrast, prior works [4]–[6], [11] perform this analysis only at the lowest temperature in the range, ignoring NTD/MTD effects.
- We model the biaxial nature of the TSV stress considering the differences in material properties of TSV, liner, and silicon along with the traction free condition on the respective surfaces. This leads to a better comparison with FEM, in the useful range from and beyond the Keep-Out Zone (KOZ).[1]
- On benchmark circuits, we demonstrate how the path delays in a circuit can change, depending on the relative locations of gates on the path and the TSVs. We show the magnitude of these changes and their impact on the critical path in a circuit. Furthermore, we show the circuit leakage power variations due to TSVs in the layout.

[1]The KOZ is the (often rectangular) region around the TSV within which no transistor is allowed to be placed, since the stresses are very high and can adversely affect transistor performance and reliability.

II. Stress modeling

A. Notation and definitions

The stress field is represented as a tensor that comprises six unique stress components: three normal stresses (σ_{11}, σ_{22}, σ_{33}) and three shearing stresses (τ_{12}, τ_{23}, τ_{31}), where the subscripts 1, 2, and 3 correspond to the three orthogonal axes in any spatial coordinate system. Similarly, the six strain [three displacement] fields are represented by ϵ_{ij} [u_i] where $i, j \in \{1, 2, 3\}$. In Cartesian coordinates, these correspond to the x, y, and z directions, while in cylindrical coordinates the axes are along radial (r), circumferential (θ), and axial (z) directions. In the rest of the paper, a superscript $M \in \{Cu, Si, Liner = SiO_2/BCB\}$ represents the corresponding elastic fields in the corresponding materials. The physical constants used in this work are given in Table I.

In cylindrical coordinates where the z-axis is perpendicular to the TSV and silicon surface, a *traction-free* condition corresponds to $\sigma_{zz} = \tau_{rz} = 0$.

TABLE I
Physical Constants for Stress Computation

	E (GPa)	**CTE (ppm/^{o}C)**	ν
Copper	111.5	17.7	0.343
Silicon	162.0	3.05	0.28
SiO_2	71.7	0.51	0.16
BCB	3	40	0.34

A stress tensor that is defined by only one normal stress component, the other components being zero, corresponds to *uniaxial stress*; one defined by two normal stresses, the other stresses being zero, is referred to as *biaxial stress*.

B. Overview of our TSV stress solution

The TSV structure is three-dimensional in nature, with the TSV, liner and silicon having different material properties as shown in Table I. Three-dimensional problems in elasticity can often be reduced to 2D problems to simplify solution procedures. These are known as *plane* problems, where displacement and stress components can be treated independent of one of the axis directions, based on the geometry. Here we shall treat the z-axis as the independent axis direction and use cylindrical coordinates to describe the approaches. These plane problems can be solved in two ways [12]:

- A *plane strain* approach is used when the dimensions of a body along the z-axis is much larger than the cross-section along the orthogonal axes directions. This makes the displacements and the stresses independent of the z-direction. Furthermore, $\epsilon_{iz} = 0$ with $i \in \{r, \theta, z\}$, in the plane strain approach. However, from Hooke's law, even when the z-dimensional strains are zero, it can be shown

that σ_{zz} can be nonzero in general due to the Poisson's effect of stresses in other directions.

- A *plane stress* condition exists when the thickness along the z-axis is smaller compared to the other dimensions. Here, the stresses and displacements almost remain the same through the thickness and hence are independent of the z-direction. Furthermore, in *plane stress* problems, $\sigma_{zz} = 0$ and $\tau_{iz} = 0$ with $i \in \{r, \theta\}$. Analogous to the plain strain approach, from Hooke's Law, ϵ_{zz} can be nonzero in general for a plane stress analysis.

Based on the TSV geometry and the resultant stress distributions, we choose to solve the problem using a superposition of two solutions. First, we apply 2D plane strain techniques to obtain the thermal residual stress distributions in the TSV structure, considering the material property differences. However, as pointed out above, the σ_{zz} stress component is nonzero on the surfaces of the TSV and the liner. Thus the surface of the TSV structure is not traction-free in the 2D solution.

To recover the traction-free condition on the TSV and the liner surfaces, a compensating pressure, equal in magnitude but opposite in direction as that of the 2D solution, is applied on the respective surfaces. This corresponds to a Boussinesq problem in elasticity and deals with stress distributions in a 3D half-space, when surface normal pressure is applied over a region [8], [13]. For simplicity, we assume the 3D half-space is entirely homogeneous and is made up of silicon. It will be shown later that the error due this assumption is minor in practice, and that the analytical stress closely matches with that of the FEA. The rationale behind this approach is that the compensatory pressure is a second-order effect, and a slight inaccuracy in its computation is tolerable.

The complete stress solution is then a linear superposition of the stresses from the 2D problem and the surface stress distributions of the Boussinesq type problems. Let $[\sigma^{Si}]_{axi}$ denote the stress tensor from the axisymmetric 2D solution and let $[\sigma^{Si}]_{Bou1}$ and $[\sigma^{Si}]_{Bou2}$ denote the Boussinesq type solutions due to normal pressure over TSV and the liner surfaces, respectively. The total stress response σ^{Si} can be obtained as:

$$\sigma^{\mathbf{Si}} = \left[\sigma^{\mathbf{Si}}\right]_{axi} + \left[\sigma^{\mathbf{Si}}\right]_{Bou1} + \left[\sigma^{\mathbf{Si}}\right]_{Bou2} \tag{1}$$

C. 2D-axisymmetric solution

The TSV is modeled as a long copper cylinder surrounded by a thin liner layer and encompassed by infinite silicon. This assumption is valid since the TSV diameter is typically smaller compared to its height, which is taken along the z-axis. Furthermore, TSV-induced stress vanishes after a short finite distance in silicon and thus the assumption of infinite silicon. We apply the 2D plane strain techniques to obtain the stress state of this mechanical system.

Fig. 2 shows the 2D view of an isolated TSV in silicon with a liner layer. The z-axis is normal to the plane of the paper. Let O denote the origin of the cylindrical coordinate axes. Let a and b denote the radii of the inner and outer circles, respectively. Thus, if R^{Cu} [t^{Liner}] represent the radius [thickness] of the TSV [Liner], then $a = R^{Cu}$ and $b =$

TABLE II
ANALYTICAL STRESS COMPONENTS

Stress components due to 2D axisymmetric thermal stress solution

Stress in Copper TSV:

$$\begin{aligned}
\sigma_{rr}^{Cu} &= \sigma_{\theta\theta}^{Cu} = C^{Cu}\left[A^{Cu} - (1+\nu^{Cu})\alpha^{Cu}\Delta T\right] \\
\sigma_{zz}^{Cu} &= \nu^{Cu}\left(\sigma_{rr}^{Cu} + \sigma_{\theta\theta}^{Cu}\right) \neq 0
\end{aligned}$$

Stress in liner (SiO_2/BCB):

$$\begin{aligned}
\sigma_{rr}^{Liner} &= C^{Liner}\Bigg[A^{Liner} - \frac{B^{Liner}}{r^2}\left(1-2\nu^{Liner}\right) \\
&\quad -(1+\nu^{Liner})\alpha^{Liner}\Delta T\Bigg] \\
\sigma_{\theta\theta}^{Liner} &= C^{Liner}\Bigg[A^{Liner} + \frac{B^{Liner}}{r^2}\left(1-2\nu^{Liner}\right) \\
&\quad -(1+\nu^{Liner})\alpha^{Liner}\Delta T\Bigg] \\
\sigma_{zz}^{Cu} &= \nu^{Liner}\left(\sigma_{rr}^{Liner} + \sigma_{\theta\theta}^{Liner}\right) \neq 0
\end{aligned}$$

Stress in silicon:

$$\begin{aligned}
\left[\sigma_{rr}^{Si}\right]_{axi} &= -\left[\sigma_{\theta\theta}^{Si}\right]_{axi} = (1-2\nu^{Si})C^{Si}B^{Si}\frac{1}{r^2} \\
\left[\sigma_{zz}^{Si}\right]_{axi} &= \nu^{Si}\left(\left[\sigma_{rr}^{Si}\right]_{axi} + \left[\sigma_{\theta\theta}^{Si}\right]_{axi}\right) = 0
\end{aligned}$$

Stress components due to Boussinesq type solution

$$\begin{aligned}
\left[\sigma_{rr}^{Si}\right]_{Bou1} &= -\left[\sigma_{\theta\theta}^{Si}\right]_{Bou1} = (1-2\nu^{Si})\left[\sigma_{zz}^{Cu}\frac{a^2}{2}\right]\frac{1}{r^2} \\
\left[\sigma_{rr}^{Si}\right]_{Bou2} &= -\left[\sigma_{\theta\theta}^{Si}\right]_{Bou2} = (1-2\nu^{Si})\left[\sigma_{zz}^{Liner}\frac{b^2-a^2}{2}\right]\frac{1}{r^2} \\
\left[\sigma_{zz}^{Si}\right]_{Bou1} &= \left[\sigma_{zz}^{Si}\right]_{Bou2} = 0
\end{aligned}$$

Constants

$$\begin{aligned}
C^{M} &= \frac{E^{M}}{(1+\nu^{M})(1-2\nu^{M})} \text{for} M \in \{Cu, Si, Liner\} \\
A^{Cu} &= A^{Liner} + \frac{B^{Liner}}{a^2} \\
B^{Cu} &= 0 \\
A^{Liner} &= \frac{mh-ng}{h(1+c_2)-g(1-c_4)}\Delta T \\
B^{Liner} &= \frac{n(1+c_2)-m(1-c_4)}{h(1+c_2)-g(1-c_4)}\Delta T \\
A^{Si} &= (1+\nu^{Si})\alpha^{Si}\Delta T \\
B^{Si} &= c_2 A^{Liner} b^2 - c_1 B^{Liner} - c_2 b^2 (1+\nu^{Liner})\alpha^{Liner}\Delta T \\
m &= (1+\nu^{Si})\alpha^{Si} + c_2(1+\nu^{Liner})\alpha^{Liner} \\
n &= (1+\nu^{Cu})\alpha^{Cu} - c_4\alpha^{Liner} \\
g &= \frac{1-c_1}{b^2};\ h = \frac{1+c_3}{a^2} \\
c_1 &= \frac{E^{Liner}(1+\nu^{Si})}{E^{Si}(1+\nu^{Liner})};\ c_2 = \frac{c_1}{1-2\nu^{Liner}} \\
c_3 &= \frac{E^{Liner}(1+\nu^{Cu})}{E^{Cu}(1+\nu^{Liner})};\ c_4 = \frac{c_3}{1-2\nu^{Liner}} \\
a &= R^{Cu};\ b = R^{Cu} + t^{Liner} \\
\Delta T &= T - T_{ref}
\end{aligned}$$

$R^{Cu} + t^{Liner}$. The stress tensor at the point $P(r, \theta)$ in silicon is computed using 2D plane strain techniques. Appendix A provides the governing equation and the general solution for this 2D axisymmetric problem.

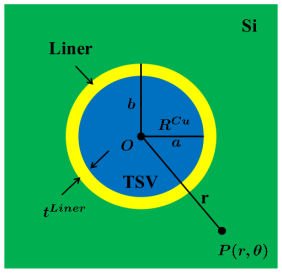
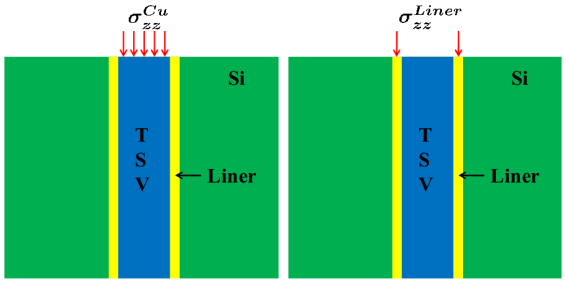


Fig. 2. Axisymmetric geometry of TSV (blue) surrounded by thin liner (yellow) and encompassed by infinite silicon (green). The z-axis is normal to the plane of the paper.

The complete solution, for the 2D thermal stress problem in copper, liner (SiO_2/BCB), and silicon is listed in Table II. The terms A^M and B^M for $M \in \{Cu, Si, Liner = SiO_2/BCB\}$ represent the coefficients of the general solution of equation (A.18) which are determined by the boundary conditions given in the Appendix A. In Table II, the terms E^M, ν^M, and α^M denote, respectively, the Young's modulus, Poisson's ratio, and the CTE of the material M. The temperature differential ΔT is the difference between operating temperature T and the initial copper annealing temperature, T_{ref} (250°C).

In Table II, the terms m and n contribute to the CTE mismatch between copper/liner, and liner/silicon materials, respectively. In addition, the terms c_1, c_2, c_3, c_4, g, and h factor in the other mechanical property differences. From Table II, it can observed that the non-zero coefficients of the general stress solution in equation (A.18): A^{Cu}, A^{Liner}, B^{Liner}, A^{Si}, and B^{Si}, are all proportional to the temperature differential ΔT. Consequently, the resultant stress components in copper TSV, liner, and silicon shown in Table II, are also proportional to ΔT; they vary linearly with the operating temperature T.



(a) (b)

Fig. 3. Boussinesq problem for surface uniform normal pressure acting on (a) circular region (TSV region) of area πa^2 (b) circular ring-shaped region (liner region) of area $\pi(b^2 - a^2)$.

D. Solving the Boussinesq problem

From Table II, it can be seen that σ_{zz}^{Cu} and σ_{zz}^{Liner} are nonzero and thus the surface is not traction-free under the 2D plane strain solution. Since σ_{zz}^{Cu} and σ_{zz}^{Liner} are independent of the distance r, they are uniform over the surfaces of the TSV and the liner regions, respectively. To recover to the traction-free condition, a compensating normal pressure equal in magnitude but opposite in direction are applied over the respective surfaces and the Boussinesq type problems are solved. As stated earlier, the 3D half-space is treated as entirely made up of silicon, by ignoring material property differences. Furthermore, in integrated circuits, since devices are located near the surface, we need to determine the 3D stress distributions only on a single plane at the surface of the silicon. For a general Boussinesq problem in cylindrical coordinates, the elastic fields at the surface depend purely upon the distance r and not upon z as shown in the Appendix B. The general solution of the resultant stress components in the silicon region for a pressure P applied over circular region is given in equation (A.19). Fig. 3 shows the application of the Boussinesq technique applied to the TSV structure. The following two subproblems are evaluated to recover the traction-free condition over the TSV and the liner:

- A uniform pressure equal to σ_{zz}^{Cu} is applied on a circular region of area πa^2 (TSV region) of a half-space (silicon) as shown in Fig. 3(a). The resultant normal stress components in silicon are denoted by $[\sigma_{ij}^{Si}]_{Bou1}$ in Table II.
- A uniform pressure equal to σ_{zz}^{Liner} applied on a ring-shaped circular region of area $\pi(b^2 - a^2)$ (liner region) of a half-space (silicon) as shown in Fig. 3(b). The resultant normal stress components in silicon are denoted by $[\sigma_{ij}^{Si}]_{Bou2}$ in Table II.

III. Application to Integrated Circuits

Since our goal is to predict stress distributions in silicon due to TSV-induced thermal stress, we shall focus on the stress components in silicon alone and ignore the superscript M in the rest of the paper. Using 2D plane strain and Boussinesq approaches together with equation (1), the stress in silicon in cylindrical coordinates is given by:

$$\begin{aligned} \sigma_{rr} &= -\sigma_{\theta\theta} = \frac{K}{r^2} \\ \sigma_{zz} &= \tau_{rz} = \tau_{\theta z} = 0 \end{aligned} \tag{2}$$

where,

$$K = (1 - 2\nu^{Si}) \left[C^{Si} B^{Si} + \sigma_{zz}^{Cu} \frac{a^2}{2} + \sigma_{zz}^{Liner} \frac{b^2 - a^2}{2} \right]$$

Here K is a constant that takes into account the difference in mechanical properties, the temperature differential and the effect of the surface normal pressure on top of TSV and the liner. From the terms in Table II it can be deduced that K is directly proportional to ΔT. Thus at a fixed distance r, the stress components vary linearly with operating temperature T. Furthermore, from equation (2), for a fixed temperature the stress decreases quadratically with distance r. Moreover, the presence of two non-zero stress components in equation (2), shows that the TSV-induced stress is biaxial in nature.

A. Stress in Cartesian coordinate systems

Although the stress equations (2) have been expressed in the cylindrical coordinate system, IC design uses Manhattan geometries and it is convenient to transform these to the Cartesian coordinate system. This will facilitate the piezoresistivity

calculations described in Section IV. Using the transformations $x = r\cos\theta$ and $y = r\sin\theta$, as in [6], and with cylindrical-to-Cartesian tensor transformations, the following expressions are obtained from equation (2):

$$\begin{aligned} \sigma_{xx} &= -\sigma_{yy} = K\frac{x^2-y^2}{(x^2+y^2)^2} = \sigma_{rr}\cos 2\theta \\ \tau_{xy} &= K\frac{2xy}{(x^2+y^2)^2} = \sigma_{rr}\sin 2\theta \\ \sigma_{zz} &= \tau_{yz} = \tau_{zx} = 0. \end{aligned} \quad (3)$$

As defined earlier, σ_{xx}, σ_{yy}, and σ_{zz} are the three normal stresses in Cartesian coordinate axis, and τ_{xy}, τ_{yz}, τ_{xz} are the shearing stress components. The angle θ corresponds to the angle made by the transistor with the TSV.

B. Impact of the crystal orientation

The crystal orientation refers to the Miller index of the silicon crystal. The principal crystallographic axes create a coordinate system that corresponds to the [100], [010], and [001] directions. Within this system, the orientation of a wafer is defined as the direction normal to the plane of the silicon wafer. The (100) orientation is the dominant paradigm (although other orientations such as (111) may also be used) and our exposition will focus on this case. Due to symmetry, the (100), (010), and (001) orientations are equivalent.

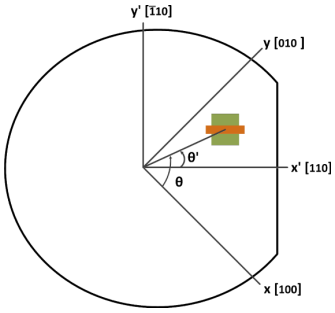


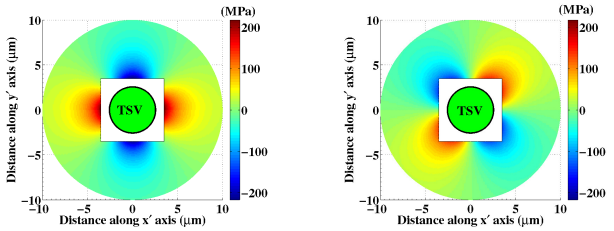
Fig. 4. Coordinate axes in (100) Si with a wafer flat orthogonal to the [110]. The transistor channel here is perpendicular to the [110] axis i.e., $\phi' = \pi/2$.

The orientation of transistors on a wafer is determined relative to the wafer flat, as shown in Fig. 4: transistors may be parallel or perpendicular to this feature. Therefore, a rotated coordinate space with a new x'-axis that is perpendicular to the wafer flat is a convenient frame of reference. This x'-axis is in the [110] direction, and therefore, the [100]–[010] axes must be rotated by $45°$ [14], [15].

By examination, a rotation by 45° causes the axial direction to move along the transverse direction. We can thus easily deduce the biaxial stress tensors in these coordinates from equations (3) to be:

$$\sigma_{x'x'} = -\sigma_{y'y'} = \tau_{xy}; \quad \tau_{x'y'} = -\sigma_{xx} \quad (4)$$

The Fig. 5 shows the stress contours of $\sigma_{x'x'}$ and $\tau_{x'y'}$. The stress patterns are seen to be tensile and compressive in mutually perpendicular directions. This results from the $\cos 2\theta$ [$\sin 2\theta$] term in σ_{xx} [τ_{xy}] in equation (3).



(a) (b)

Fig. 5. Stress contour fields in the [110]-[$\bar{1}$10] axes. (a) $\sigma_{x'x'}$ stress contour field. (b) $\tau_{x'y'}$ stress contour field.

C. Comparison with finite element simulation

To validate the effectiveness of the closed-form 2D analytical solution in equation (2), we perform 3D FEA simulations using the ABAQUS [16] tool with realistic TSV structures. As stated earlier, since we are interested in modeling the degradation of the devices, our region of interest lies outside the KOZ. In our experiments, we define the KOZ to be 1μm from the edge of the TSV or 3.5μm from the center of the TSV, and is chosen to ensure that there is no more than 33% mobility variation in any transistor around an isolated TSV. In practice, the KOZ constraint is driven by the mobility degradation of PMOS transistors, which exceeds that of NMOS devices. The effect of the copper landing pad is ignored in this analysis, since the landing pad size is always within the KOZ boundary and its main influence is felt only at the edge of the TSV.

All materials (TSV, liner, silicon) are assumed to be linear, elastic, and isotropic. The annealing process is modeled in FEA by applying a temperature load with an initial temperature of 250°C and final temperature of 25°C. For the 3D FEA simulations, the copper TSV diameter is 5μm, height is 30μm, and the liner thickness is 125nm [17]. The mechanical properties of the materials are listed in Table I.

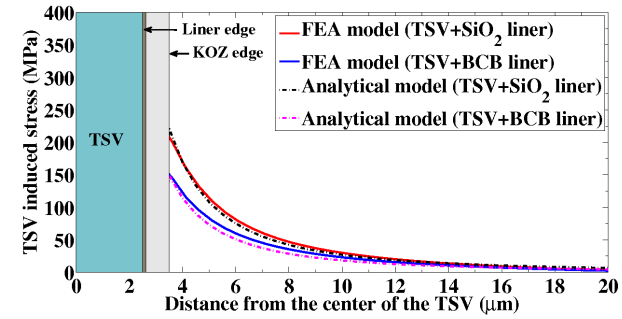
The analytical solution is compared against actual FEA stress with BCB and SiO_2 liners, respectively. Fig. 6 shows the comparison of the corresponding models against σ_{rr} and $\sigma_{\theta\theta}$ components. It can be observed that the analytical models closely follow their FEA counterparts outside the KOZ. The small errors between the analytical solution and FEA can be attributed to the assumption of a homogeneous TSV structure (silicon) in the Boussinesq subproblems.

It will be shown in Section VI that the worst case error in actual gate delay computations, using the analytical models as compared to the FEA models, is less than 1ps for a two input NAND gate in the library.

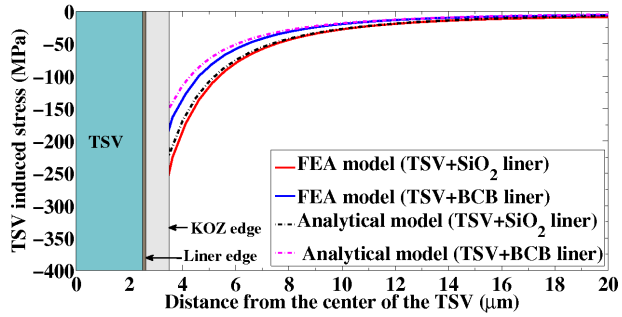
IV. Effects of Stress on Electrical Parameters

Applied mechanical strain alters the band structure of semiconductors [18] and causes changes in electrical parameters – low-field mobility, threshold voltage, and saturation velocity. This section deals with modeling the changes in electrical parameters under TSV-induced stress effects.

In an unstrained silicon, according to many valley theory, there are six degenerate conduction band valleys, with a pair along each of the three Cartesian coordinate axes. On the other hand, the valence band consists of two degenerate electronic



(a)



(b)

Fig. 6. Comparison of (a) σ_{rr} and (b) $\sigma_{\theta\theta}$ between the analytical and the FEA models. The TSV edge, liner edge, and KOZ edge are at 2.5μm, 2.625μm and 3.5μm respectively.

bands – heavy hole and light hole, and one split-off band lower in energy. Applied strain lifts the degeneracies of the conduction and valence band valleys and causes shifts and splits in the electronic band potentials. The changes in the mobility and saturation velocity can be attributed to the strain-induced carrier effective mass changes and reduction in inter-valley scattering [18]. The threshold voltage changes are due to the strain-induced shifts in conduction and valence band electronic band potentials [19], [20].

Strictly speaking, the complete electronic band structure needs to be evaluated to compute changes in electrical parameters. However, for the small strains such as those induced by the TSV, piezoresistivity [deformation potential theory] can be applied to evaluate changes in mobility [threshold voltage] as a function of stress [strain] components. The changes in saturation velocity can be expressed in terms of the changes in low-field mobility [2], [21].

The electronic band potentials in silicon are defined along the <100> directions in Miller notation [18]. The energy band gap is typically measured along this direction. Thus, we need the strain tensors in the Cartesian system for evaluating strain-induced threshold voltage variations. However, the transistor channel orientation with the crystallographic axes determines the carrier transport properties, hence the magnitude of mobility variation. Thus, in piezoresistivity calculations we use the stress components in the primed coordinate system which is parallel and perpendicular to the wafer flat direction.

A. Transistor low-field mobility variation with stress

In quantum mechanics, the transistor mobility is related to the effective mass of the carriers and scattering mechanisms by the Drude's approximate model as [18]:

$$\mu = e\tau/m^* \tag{5}$$

where e is the charge of the carrier, τ is the mean free time between scattering or momentum relaxation time, and m^* is the effective mass of the charge carrier. For the NMOS [PMOS] transistors, the active charge carriers are electrons [holes]. The reduction of scattering mechanisms due to band-splitting increases τ and has a positive effect on mobility. Similarly, the decrease [increase] in the effective mass m^* increases [decreases] low-field mobility.

The scattering mechanisms dominant in silicon processes are: quantum-mechanical acoustic (intra-valley) and optical (inter-valley) phonon scattering, and process-induced surface roughness scattering. The intra-valley scattering is dominant at low temperatures, while at room temperature and above the inter-valley scattering phenomenon dominates [18]. However, the changes in the electronic transport parameters can be accurately determined through full-band simulations alone [22], [23]. For small strains, we can make use of piezoresistivity theory where the changes in the low-field mobility are expressed as a linear combination of stress tensor components.

From the basic axiom of the theory of conduction of electrical charge, the current density vector is a function of electric field vector. Alternatively, the electric field vector is related to the current density vector by the resistivity tensor, which can be related to mobility. According to piezoresistivity theory, the resistivity tensor components vary with applied mechanical stress in piezoresistive materials such as silicon [24]. A complete mathematical model for piezoresistivity has been presented and demonstrated in silicon in [15].

In the rotated (x', y') coordinate system described earlier, the relative change in mobility is given by the expression:

$$\begin{aligned}\frac{\Delta\mu'}{\mu'} &= \left[\pi'_{11}\sigma_{x'x'} + \pi'_{12}\sigma_{y'y'}\right]\cos^2\phi' \\ &\quad + \left[\pi'_{11}\sigma_{y'y'} + \pi'_{12}\sigma_{x'x'}\right]\sin^2\phi' + \left[\pi'_{44}\tau_{x'y'}\right]\sin 2\phi' \end{aligned}\tag{6}$$

Here, π'_{11}, π'_{12} and π'_{44} are the three unique piezoresistivity coefficients defined along the primed coordinate axes, and ϕ' is the angle made by the transistor channel with the x'-axis, i.e., the [110] axis. This implies that $\phi' = 0$ for the transistor channels that are oriented along this direction, and $\phi' = \pi/2$ when they are orthogonal to this axis. As we will see, the piezoresistivity coefficients and the stress tensor components vary with the channel orientation, implying that the mobility variation depends on the transistor channel orientation.

In practice, the piezoresistivity coefficients for silicon are typically listed in databooks along the crystallographic axes. Using standard techniques for coordinate rotation, the corresponding coefficients in primed axes are obtained as [25]:

$$\begin{aligned}\pi'_{11} &= (\pi_{11} + \pi_{12} + \pi_{44})/2 \\ \pi'_{12} &= (\pi_{11} + \pi_{12} - \pi_{44})/2 \\ \pi'_{44} &= \pi_{11} - \pi_{12}\end{aligned}\tag{7}$$

Here, the terms π_{11}, π_{12}, and π_{44} are the primary piezoresistive coefficients along the crystallographic axes. Table III

shows the values for the primary piezoresistivity coefficients [3] in both coordinates. The relative magnitudes of the coefficients show the anisotropic nature of silicon where PMOS [NMOS] transistors oriented along primed [crystallographic] axes show greater sensitivity to stress. This will be reflected in the magnitude of mobility variations [18].

TABLE III
PIEZORESISTIVITY COEFFICIENTS (X10^{-12} Pa^{-1}) IN (100) SI [3]

	π_{11}	π_{12}	π_{44}	π'_{11}	π'_{12}	π'_{44}
NMOS	1022.0	-537.0	136.0	310.5	174.5	1559.0
PMOS	-66.0	11.0	-1381.0	-717.5	662.5	-77.0

For a transistor oriented along the [110] axis, $\phi' = 0$. From equations (4), (6), and (7),

$$\frac{\Delta\mu'}{\mu'} = \pi'_{11}\sigma_{x'x'} + \pi'_{12}\sigma_{y'y'} = \pi_{44}\sigma_{x'x'} = \pi_{44}\sigma_{rr}\sin 2\theta. \quad (8)$$

Recall that θ is the angle made by the vector from the origin to the center of the transistor with the unprimed x-axis. Similarly, for a transistor in the orthogonal direction, $\phi' = \pi/2$, and

$$\begin{aligned}\frac{\Delta\mu'}{\mu'} &= \pi'_{11}\sigma_{y'y'} + \pi'_{12}\sigma_{x'x'} \\ &= -\pi_{44}\sigma_{x'x'} = -\pi_{44}\sigma_{rr}\sin 2\theta. \end{aligned} \quad (9)$$

Fig.7 shows the mobility variations in NMOS/PMOS transistors at room temperature (25°C) based on equation (8). Based on the above analysis, we can observe that:

- For the same stress and orientation, PMOS and NMOS devices experience opposite mobility variation effects: both depend on π_{44}, which has a different sign for PMOS and NMOS (Table III). In Fig. 7 along the x'-axis direction, where the stress is tensile, PMOS mobility degrades while NMOS mobility improves; the opposite is true along y'-axis direction where the stress is compressive.
- For the same stress, PMOS devices experience greater mobility variation as compared to NMOS devices, since the π_{44} value of PMOS is an order of magnitude greater than that of the NMOS as seen in [26].
- The relative mobility variation depends on the operating temperature since stress varies linearly with temperature as pointed out in Section II.

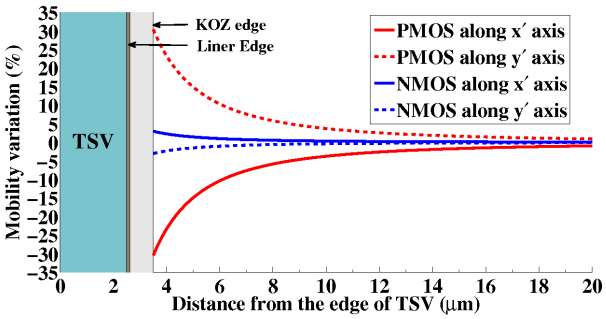


Fig. 7. Mobility variation of PMOS/NMOS transistors with distance from the TSV along x' and y' axis directions. Here edge of the TSV = 2.5μm.

B. Saturation velocity variation with mechanical stress

In short channel CMOS transistors, the high lateral electric field in the channel causes velocity saturation, where charge carriers acquire a nearly constant velocity known as saturation velocity. The parameter critical length, denoted by l, is a short distance from the source side which determines the onset of velocity saturation [27]. Beyond this critical length, saturation region drain current is entirely determined by saturation velocity, while low-field mobility dominates within the critical length and determines linear region current. However, the variations in saturation velocity can be expressed in terms of variations in the low-field mobility as shown in [2], [21].

The maximum velocity charge carriers can physically acquire in the velocity saturation region is known as the ballistic velocity denoted by v_B, and it varies inversely with the square root of the effective mass m^* [27]. Thus, the ballistic velocity can be related to the low-field mobility by an empirical power law as $v_B \propto \mu^{\alpha}$. If scattering is ignored, $\alpha \approx 0.5$. In reality, under different scattering mechanisms $\alpha < 0.5$ [2], and thus limits the maximum achievable velocity. The resultant net saturation velocity at the source is also known as source injection velocity v_{inj} [28], which determines the saturation drain current. The ratio of v_{inj} to v_B is known as ballistic efficiency and is denote by B; B is typically less than 1. Furthermore, the critical length parameter l decreases with increased low-field mobility and can be empirically expressed as $l \propto \mu^{-\beta}$, where $\beta \approx 0.45$ [2]. The relative changes in injection velocity, which determines the drain saturation current, can be expressed in terms of the relative changes in the low-field mobility as [2]:

$$\frac{\Delta v_{inj}}{v_{inj}} = [\alpha + (1-B)(1-\alpha+\beta)]\frac{\Delta\mu}{\mu} \quad (10)$$

Experimental studies in [2] show that the correlation between changes in saturation velocity and changes in mobility is about 0.85. From equation (10) it can be deduced that even when ballistic efficiency approaches 1 in highly scaled devices, the saturation velocity may still be related to low-field mobility by the factor α [21], [29]. Furthermore, advantageous strain improves the carrier effective mass and thus ballistic velocity limit itself increases with such strain [2].

C. Threshold voltage variation due to mechanical stress

According to the deformation potential theory [18]–[20], mechanical strain in the channel causes shifts and splits (by lifting the degeneracy) in conduction and valence band potentials. This results in corresponding shifts in the threshold voltage of the transistors and can be attributed to changes in silicon electron affinity, band gap, and valence band density-of-states. As pointed out earlier, the strains in the Cartesian coordinate system are employed to evaluate the changes in conduction and valence band potentials as [18], [20]:

$$\begin{aligned}&\Delta E_C^{(i)}(\epsilon) = \Xi_d(\epsilon_{xx}+\epsilon_{yy}+\epsilon_{zz}) + \Xi_u\epsilon_{ii}, i \in \{x,y,z\} \\ &\Delta E_V^{(hh,lh)}(\epsilon) = a(\epsilon_{xx}+\epsilon_{yy}+\epsilon_{zz}) \\ &\pm\sqrt{\frac{b^2}{4}(\epsilon_{xx}+\epsilon_{yy}-2\epsilon_{zz})^2 + \frac{3b^2}{4}(\epsilon_{xx}-\epsilon_{yy})^2 + d^2\epsilon_{xy}^2}\end{aligned} \quad (11)$$

Here, $\Delta E_C^{(i)}$ is the change in the conduction band potential energy of the carrier band number i. The term E_V^{hh} (E_V^{lh}) denotes the heavy-hole (light-hole) valence band potential. The positive (negative) sign is used for E_V^{hh} (E_V^{lh}). The terms Ξ_d and a are the hydrostatic deformation potential constants, and have the effect of shifting the conduction and valence bands. On the other hand, the terms Ξ_u, b, and d are the shear deformation potentials which have the effect of lifting the degeneracy or splitting the conduction and valence bands. The corresponding values of Ξ_d, Ξ_u, a, b, and d in eV are: 1.13, 9.16, 2.46, -2.35, and -5.08. The terms ϵ_{xx}, ϵ_{yy}, ϵ_{zz}, and ϵ_{xy} denote the TSV-induced strains in Cartesian coordinate system. The strains can be obtained from the stresses in equation (3) as:

$$\begin{aligned} \epsilon_{xx} &= \frac{1}{E^{Si}}\left(\sigma_{xx} - \nu^{Si}\left(\sigma_{yy}+\sigma_{zz}\right)\right) \\ \epsilon_{yy} &= \frac{1}{E^{Si}}\left(\sigma_{yy} - \nu^{Si}\left(\sigma_{zz}+\sigma_{xx}\right)\right) \\ \epsilon_{xy} &= \frac{1+\nu^{Si}}{E^{Si}}\tau_{xy} \\ \epsilon_{zz} &= \epsilon_{yz} = \epsilon_{zx} = 0 \end{aligned} \tag{12}$$

From equations (3) and (12), it can be deduced that $\epsilon_{xx} = -\epsilon_{yy}$, and $\epsilon_{zz} = 0$. Thus, the hydrostatic contribution in equation (11), $\epsilon_{xx} + \epsilon_{yy} + \epsilon_{zz} = 0$. Hence, under TSV-induced stress, there is only splitting of conduction and valence bands without any hydrostatic shifts. This is unlike the process induced strains in [30] where both hydrostatic shifts and shear splits take place in electronic bands. The net effect is a smaller variation in electronic band gap potential due to TSV-induced stress. Regardless of the strain type, the energy band gap has been shown to decrease [22], [31]. Thus threshold voltage is also expected to decrease under TSV-induced stress.

The threshold voltage is a function of band-gap potential and thus can be expressed as a function of the changes in conduction band and valence band potentials. Ignoring the changes in the densities of states whose contributions are negligible [32], we have:

$$\begin{aligned} q\Delta V_{tp} &= m\Delta E_C - (m-1)\Delta E_V \\ q\Delta V_{tn} &= m\Delta E_V - (m-1)\Delta E_C \end{aligned} \tag{13}$$

where ΔV_{tp} and ΔV_{tn} are the changes in PMOS and NMOS threshold voltages, respectively, $q = 1.6 \times 10^{-19}$C is the electron charge, and m is the body-effect coefficient and takes values 1.1−1.4. ΔE_C is the minimum of the changes in conduction band potentials, ΔE_C^i. Since conduction band is lowered under TSV-induced stress, ΔE_C is negative valued. The term ΔE_V denotes the maximum of the changes in valence band potentials, ΔE_V^{hh} and ΔE_V^{lh}, and is positive valued. This leads to decrease in bandgap potential consistent with [22], [31]. The work in [33] uses similar models to predict TSV-induced threshold voltage variation of upto 8mV, but uses the generalized process strain equations in [30] which is not valid for TSV-induced strains. Furthermore, in the same work, there is a sign error in the usage of ΔE_C and band gap potential. This leads to errors in threshold voltage computations, although the actual changes in threshold voltage are still within 15mV under TSV effects.

Based on the above analysis, the threshold voltage variations of PMOS and NMOS transistors are plotted in Fig. 8 at the room temperature (25^{o}C). We can observe that threshold voltage for the PMOS and NMOS have decreased; positive [negative] shifts for PMOS [NMOS]. Furthermore, beyond a short distance from the KOZ edge, the threshold voltage variations are practically zero. The patterns can be explained by the relations in equations 11 and 13. The threshold voltage improvements suggest leakage power degradations.

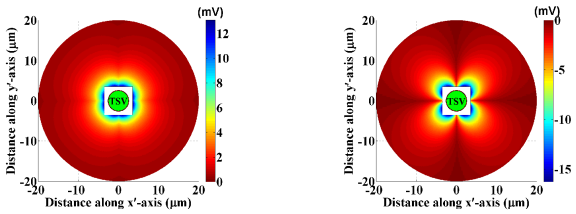


Fig. 8. TSV-induced threshold voltage variation in (a) PMOS transistor (b) NMOS transistor. Here edge of the TSV = 2.5μm. KOZ edge = 3.5μm

V. Timing Analysis under Electrical Variations

Our circuit-level input is a characterized cell library and a placed netlist, based on which the stresses may be computed using the techniques in Section II; this stress can be converted to determine the transistor mobility, saturation velocity, and threshold voltage variations, using the methods in Section IV.

A. Delay dependence on temperature

We first consider the effects of temperature on delay without TSV stress and then add the TSV stress effects.

The traditional assumption that has guided timing analysis is that the delays of library cells increase monotonically with temperature, corresponding to the NTD case. However, with technology scaling and the increased use of lower V_{dd} and V_t values, PTD and MTD are also often seen. Gate delays change with T in two ways:

(1) The *mobility change* for charge carriers, $\Delta\mu_T$, is given by:

$$\Delta\mu_T = \mu\left(T_0\right)\left(T/T_0\right)^{-m} \tag{14}$$

Here T_0 is the room temperature, and $m > 0$ is the mobility temperature exponent, with a typical value of 1.7 in highly doped silicon, and 1.4 in nanometer silicon layers, where boundary scattering becomes important [34]. This reduction in μ increases the delay.

(2) The *threshold voltage change*, ΔV_t, for a transistor is given by:

$$\Delta V_t = -\kappa\left(T - T_0\right) \tag{15}$$

where $\kappa > 0$ has a typical value of 2.5mV/K [35]. Thus, the delay decreases with T due to this effect.

The two phenomena above have opposite effects on gate delays, and depending on which of the two is more dominant, results in PTD, NTD, or MTD effects.

B. Gate characterization

The variation in the low-field mobility, saturation velocity and threshold voltage translates into variations in the gate delay metric. Since changes in saturation velocity are correlated to the changes in low-field mobility as seen from equation (10), it suffices to express changes in gate delays in terms of changes in low-field mobility and threshold voltage. The delay, D_{str}, of a gate under stress is given by:

$$D_{str} = D_{nom} + \left(\frac{\partial D}{\partial \mu}\right)(\Delta\mu_{TSV} + \Delta\mu_T) + \left(\frac{\partial D}{\partial V_t}\right)\left(\Delta V_t^{TSV} + \Delta V_t\right) \quad (16)$$

where D_{nom} is the delay without temperature or TSV effects, $\partial D/\partial \mu$ [$\partial D/\partial V_t$] is the sensitivity of the delay to mobility [V_t] variation at the nominal point, and $\Delta\mu_{TSV}$ [ΔV_t^{TSV}] is the mobility [threshold voltage] change due to TSV stress. Note that the sensitivity $\partial D/\partial \mu$ accounts for both low-field mobility and saturation velocity. For the 45nm technology used in our work, the changes in velocity saturation account for less than 1% change in gate delays. In this work, the delay variations are primarily due to the changes low-field mobility and the threshold voltage.

The mobility sensitivity is a nonlinear function of the nominal point, and is stored as a look-up table (LUT) rather than a constant sensitivity value. On the other hand, the threshold voltage sensitivity is a linear function of the nominal point. During delay calculation, linear interpolation is used between the stored points. This results in improved accuracy, e.g., for a NAND2 gate in the library, the delay error using our approach is less than 3%.

LUT characterization is a one-time exercise for a library. The range of the LUT reflects the observed range of variations. For example, for mobility sensitivity, using HSPICE, we characterize a 45nm gate library for five delay values with corresponding PMOS mobility variations ranging from $\pm 50\%$. For the NMOS mobility variations, we use a linear approximation considering a range of $\pm 5\%$. For threshold voltage sensitivity, we characterize the gate library at the nominal threshold voltage and with a shift of -20 mV [20 mV] in NMOS [PMOS] transistors. The library characterization is performed from $-25°$C to $125°$C, along with different supply voltages, load capacitances, and input slopes.

The leakage power of a transistor exponentially increases (decreases) with its decreasing (increasing) threshold voltage. However, for small changes in threshold voltage of a transistor, the gate-level leakage power varies almost linearly. As seen in Fig. 8, the TSV-induced threshold voltage variations in transistors are typically few tens of millivolts not exceeding 15 mV. For the TSV-induced stress, all the transistors of the same type (NMOS or PMOS) experience equal magnitude of threshold voltage shifts. This is because TSV-stress spans an area that is considerably larger than the individual layouts of the logic gates. Thus, if there are n transistors in a gate, the total leakage power of the gate is given by:

$$L_{gate}^{str} = L_{gate}^{nom} + \sum_{i=1}^{n} \left.\frac{\partial L_{gate}}{\partial V_{ti}}\right|_0 \Delta V_{ti}^{TSV} \quad (17)$$

where L_{gate}^{str} is the leakage power of a gate under TSV-induced stress and L_{gate}^{nom} is the nominal leakage power of the gate under no stress. The partial derivative of L_{gate} with V_{ti} represents the sensitivity of the leakage current of the gate to changes in the threshold voltage of transistor i, evaluated at the nominal point. ΔV_{ti}^{TSV} denotes the threshold voltage shift in the transistor i. Note that all the NMOS or PMOS transistors in a gate correspondingly have the same ΔV_{ti}. In our work, the relative error in estimating the gate leakage power of the standard cells with this approach is under 1%.

C. Timing analysis framework

For the placed netlist that is provided as an input to the procedure, the left bottom coordinates and width and height of each cell in the layout can be determined. The computation then proceeds as follows: *First*, from the above placement information, the centers of the TSV and the standard cells are computed. *Second*, the equations in (4) and (12) are used to calculate the stress and strain tensors, respectively, from every TSV present in the circuit, capturing the transistor channel orientation with respect to the wafer flat. The stress tensor from different TSVs are added up. *Third*, the mobility variations are calculated according to equations (8) for transistor channels oriented along the [110] axis. The TSV strain-induced threshold voltages are computed using equation (13). *Fourth*, the computed electrical variations are employed to obtain accurate cell delays using LUT and linear interpolation with the characterized delay values in conjunction with equation (16) during static timing analysis. *Finally*, the delay of the circuit is computed at different temperature points ranging from -25°C to 125°C in steps of 20°C.

VI. Results

A. Gate delay comparison: Analytical solution vs. FEA

In this section, we compare the errors in the gate delays based on the analytical stress models as compared to the results from true FEA stress simulations presented in Section III-C. For this analysis, we employ the analytical stress [strain] components $\sigma_{x'x'}$ and $\sigma_{y'y'}$ [ϵ_{xx}, ϵ_{yy}, and ϵ_{xy}] in the primed [Cartesian] coordinate system and its corresponding FEA counterparts to evaluate the mobility [threshold voltage] variations. Finally, gate delays are computed using equations (16).

Fig. 9(a) and Fig. 9(b) shows the errors in the gate delay of a NAND2 gate in the library around a TSV with BCB and SiO_2 liner, respectively. From the legend it can be observed that the error in using analytical models for computing the gate delays is less than 1ps. This demonstrates the accuracy of the analytical model for practical circuit performance evaluation, and thus removes the need for storage overhead of store FEA models, or the computational overhead of on-the-fly FEA.

B. Effect of TSV-induced stress on circuit path delays.

We apply our techniques on a set of IWLS 2005 benchmarks [36] whose attributes are as shown in Table IV, where #PO denotes the number of primary outputs in the design. The parameters chosen in our experiments are listed below:

- The analytical stress and strain models for TSV with BCB and SiO_2 liners, respectively.

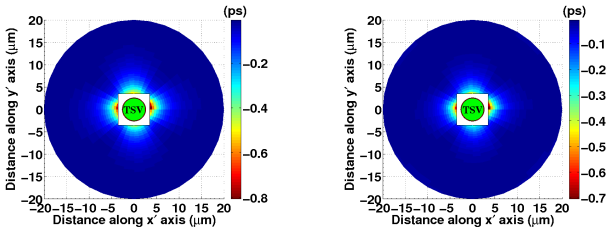


Fig. 9. Contours of rise time difference of NAND2 gate around a TSV with (a) BCB liner and (b) SiO_2 liner.

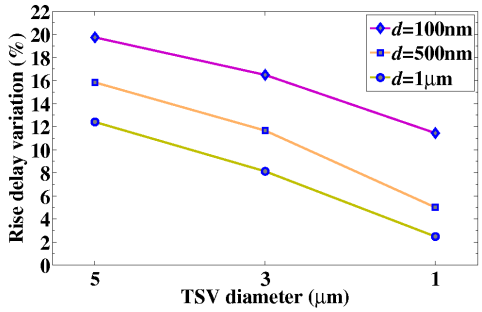


Fig. 10. FO4 rise delay variation of a NAND2 gate with different TSV diameters. The NAND2 gate is at a distance d from the KOZ edge.

- A cell library characterized under the 45nm PTM [37].
- All transistor orientations parallel to the [110] axis.
- A TSV diameter of 5μm. The TSV is surrounded by either BCB or SiO_2 liner with a liner thickness of 125nm.
- Our KOZ is defined as the point where the mobility variations are below 33%; this corresponds to a KOZ size of 1μm from the TSV edge.
- For scaled technologies, a TSV diameter of 3μm [1μm] with SiO_2 liner and a KOZ size of 0.6μm [0.2μm].

The Fig. 10 shows the FO4 rise delay variation of a NAND2 gate in the library at 25°C with TSV diameters of 5μm, 3μm, and 1μm. In all the cases, the NAND2 gate is at a fixed distance of 100nm/500nm/1μm from the KOZ edge of the corresponding TSVs. Furthermore, the centers of the standard cell and the respective TSVs are aligned along x'-axis. From the figure, it can be seen that for a fixed distance from the TSV the delay variation decreases as TSV diameter scales down, consistent with observations in previous sections. Furthermore, even for smaller TSV diameters such as 1μm, at shorter distance from the TSV, the delay variation is significant. However at the circuit level, the delay variations may get toned down due to inherent cancellations in path delay computations.

We place TSVs in the layout with equal horizontal and vertical spacing. The number of TSVs in a circuit depends upon the size of the benchmark and the TSV spacing used. The following layouts are generated using the Capo placer [38]:

- TSVless contains no TSVs.
- TSV_5_i, $i \in \{3, 7, 10\}$ correspond to regularly-spaced horizontal and vertical TSVs of diameter 5μm with a spacing of 3, 7, and 10 μm, respectively, between the edges of the KOZs for the TSVs.
- Layout TSV_3_3 [TSV_1_3] consists of identical number of TSV's as that of TSV_5_3 layout but with TSV diameter of 3μm [1μm] spaced 3μm apart.

TABLE IV
IWLS 2005 [36] CIRCUITS

Circuit	# Gates	Dimension H×W (μm×μm)	# POs	#V1	#V2	#V3
ac97_ctrl	11308	130×80	4204	70	54	35
aes_core	12223	87×85	12313	49	36	25
des	4647	68×85	332	35	24	15
ethernet	29739	104×170	32149	170	84	60
i2c	1221	16×74	204	6	5	4
mem_ctrl	10094	94×84	2522	49	36	25
pci_bridge32	11148	127×85	9025	70	48	35
spi	3632	48×87	564	21	18	10
systemcdes	2694	50×71	549	18	15	8
usb_funct	12987	76×113	3930	54	40	28

In Table IV, the corresponding number of TSVs in TSV_5_3, TSV_5_7, and TSV_5_10 layouts are: #V1, #V2, and #V3.

Tables V and Table VI show how the critical path changes, when TSV with corresponding BCB and SiO_2 liners are taken into account. In Table V, D0 represents the critical path delay for the TSVless case, and the temperature at which this delay is seen. The columns designated by D1, D2, and D3 represent the critical path delays of TSV_5_3, TSV_5_7, and TSV_5_10 layouts with the TSV+BCB liner effects. The temperatures at which the maximum occurs is shown alongside each delay. Each circuit is seen to exhibit MTD as its worst case delay occurs in the interior of the temperature range of [−25°C, 125°C]. We found that, the interconnect lengths were short in the critical paths of the circuits considered here. Hence the gate delay component dominates the interconnect delay component, and addition of interconnect delays will not significantly alter the timing results presented here.

TABLE V
COMPARISON OF CRITICAL PATH DELAY OF CIRCUITS WITHOUT AND WITH {TSV + BCB LINER} EFFECTS

Circuit	TSVless		TSV_5_3			TSV_5_7			TSV_5_10		
	D0 (ps)	T (°C)	D1 (ps)	T (°C)	$\Delta D1$ (%)	D2 (ps)	T (°C)	$\Delta D2$ (%)	D3 (ps)	T (°C)	$\Delta D3$ (%)
ac97_ctrl	505	55	501	35	-0.8%	500	35	-1.0%	504	35	-0.2%
aes_core	516	35	519	35	0.6%	538	15	4.3%	511	15	-1.0%
des	1024	35	1023	15	-0.1%	1024	15	0.0%	1022	35	-0.2%
ethernet	914	15	919	-5	0.5%	902	15	-1.3%	903	15	-1.2%
i2c	444	35	443	15	-0.2%	445	35	0.2%	445	15	0.2%
mem_ctrl	979	35	983	15	0.4%	988	15	0.9%	983	15	0.4%
pci_bridge32	738	35	737	35	-0.1%	739	35	0.1%	733	15	-0.7%
spi	954	15	957	15	0.3%	960	15	0.6%	951	15	-0.3%
systemcdes	855	15	859	-5	0.5%	865	-5	1.2%	855	15	0.0%
usb_funct	702	15	712	15	1.4%	704	15	0.3%	697	15	-0.7%

TSVs act as blockages for cell placement. When the TSV pitch changes, the locations of these blockages change, and therefore the circuit placement changes. Since the four layouts in Table V are different, these delays should not be directly compared. However, the portion of the delays, ΔDi, i ∈ {1, 2, 3}, can explicitly be attributed to the TSV+liner effects (clearly, ΔD0 is zero in the TSVless layout). To compute each ΔDi, we first find the critical path delay for the corresponding layout while ignoring TSV stress effects, then the critical path delay when TSV stresses are added in, and we show the percentage change. The liner effects are always considered when the TSV is present. In Table VI, the columns ΔD4, ΔD5, and ΔD6 represent the changes in delay of circuits TSV_5_3, TSV_5_7, and TSV_5_10, respectively, with TSV+SiO_2 liner. The corresponding changes in circuits TSV_3_3 and TSV_1_3 are shown in columns denoted by ΔD7 and ΔD8. Note that the critical path can (and often does) change with TSV stress.

TABLE VI
CRITICAL PATH DELAY OF CIRCUITS WITH {TSV + SiO_2 LINER} EFFECTS

Circuit	TSV_5_3		TSV_5_7		TSV_5_10		TSV_3_3		TSV_1_3	
	T (°C)	$\Delta D4$ (%)	T (°C)	$\Delta D5$ (%)	T (°C)	$\Delta D6$ (%)	T (°C)	$\Delta D7$ (%)	T (°C)	$\Delta D8$ (%)
ac97_ctrl	35	-0.8%	35	-1.4%	35	0.2%	35	0.2%	15	-0.2%
aes_core	35	1.0%	15	6.4%	35	-1.4%	15	1.4%	35	0.0%
des	15	0.9%	35	0.6%	35	-0.3%	15	0.6%	35	0.1%
ethernet	15	1.4%	-5	-1.2%	15	-1.4%	15	-0.8%	15	-0.1%
i2c	-125	0.5%	15	0.5%	15	0.5%	15	-0.2%	35	-0.2%
mem_ctrl	35	0.8%	15	1.3%	15	0.5%	15	0.6%	15	0.4%
pci_bridge32	35	-0.1%	35	0.1%	35	-0.8%	35	-0.4%	35	0.0%
spi	15	0.5%	15	1.2%	15	-0.4%	15	1.5%	15	0.1%
systemcdes	-5	3.0%	-5	1.8%	15	-0.1%	-5	1.3%	15	0.0%
usb_funct	-125	3.1%	15	1.6%	15	-0.9%	15	-0.4%	15	-0.1%

The improvements (negative changes) in critical path delays indicate that even with the smaller, more aggressive KOZ used here, we can mitigate the TSV effects on the critical path delays to some extent by careful design choices during initial circuit placement. Additionally, temperature dependence of the circuits is also altered when TSV effects are taken into account. In Table VI, although circuits TSV_5_3, TSV_3_3, and TSV_1_3 contain identical number of TSVs, the differences in the changes in critical path delay of individual circuits can be attributed to the difference in relative placement of the gates with respect to the TSVs. The TSV_5_3 circuit shows a delay variation of -0.8 to 3.1% while TSV_3_3 [TSV_1_3] circuit shows a variation of -0.8 to 1.5% [-0.2 to 0.4%]. Thus, it can be concluded that even with smaller dimensions of TSVs, the stress effects on circuit timing cannot be ignored.

From Tables V and VI, it can be observed that there is a wider range of delay variation in the TSV inserted layouts with SiO_2 liner as compared to the corresponding layouts with BCB liner. For instance, in the TSV_5_7 layouts, the critical path variations with SiO_2 liner ranges from -1.4% to 6.4%. The corresponding variation within the same layout with the BCB liner taken into account ranges from -1.3 to 4.3%. Similar trends can be observed in the TSV_5_3 and TSV_5_10 layouts. The smaller magnitude of variations in using a BCB liner indicates that the BCB liner is preferable over SiO_2 liner from a circuit timing perspective. The improvement in mechanical reliability in using BCB liner over SiO_2 is already shown in [7]. For these reasons, we shall focus on the layouts with TSV+BCB liner for the rest of the discussion.

TABLE VII
DELAY CHANGES IN THE TSV_5_7 CIRCUITS WITH {TSV + BCB LINER}

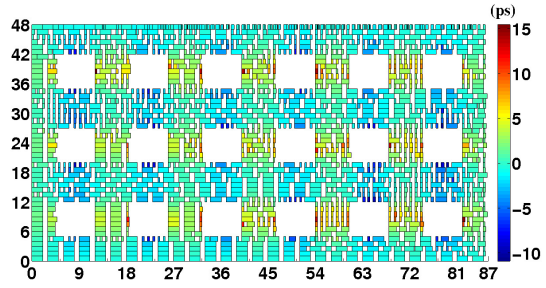
Circuit	D_{P1} (ps)	ΔD_{P1} (%)	D_{P2} (ps)	ΔD_{P2} (%)	D_{P3} (ps)	ΔD_{P3} (%)	ΔTPS (ps)	ΔTNS (ps)
ac97_ctrl	505	-1.0%	361	5.8%	347	-5.5%	-1135	0
aes_core	513	4.9%	536	4.3%	423	-4.7%	13543	-269
des	1012	1.2%	783	4.0%	833	-3.1%	261	-10
ethernet	908	-0.7%	624	4.5%	596	-5.4%	23566	0
i2c	443	0.5%	344	4.4%	295	-5.1%	29	-2
mem_ctrl	979	0.9%	597	4.9%	573	-4.5%	-327	-85
pci_bridge32	715	3.4%	566	4.8%	645	-4.2%	-217	-1
spi	951	0.9%	800	3.5%	675	-4.0%	-53	-26
systemcdes	837	3.3%	742	3.6%	485	-5.4%	1313	-13
usb_funct	684	2.9%	619	3.9%	360	-5.8%	4850	-22

In order to gain more insights into the circuit timing behavior we further examine the TSV_5_7 circuits in detail. Let P1 denote the critical path in the circuit with TSV effects. Let P2 and P3 represent the paths that show maximum delay degradation, and delay improvement, respectively, when TSV effects are considered. For each circuit, Table VII describes the extent of delay changes in these paths due TSV-induced mobility variations. Here D_{P1}, D_{P2} and D_{P3} denote the nominal path delays of paths P1, P2, and P3, respectively, and ΔD_{P1}, ΔD_{P2}, and ΔD_{P3}, respectively, are the changes in the delay of each of these paths due to TSV-stress-induced variations. Note that D_{P1} and ΔD_{P1} together evaluate to the actual critical path delay of the circuit show in column D2 of Table V. This table also shows the amount of change in the circuit total positive slack (TPS) and the total negative slack (TNS) when TSV effects are considered, are denoted by ΔTPS and ΔTNS, respectively. While computing slacks, we consider the worst case path delay of the circuit without TSV effects as the required time specification to be met. From the table we can observe that:

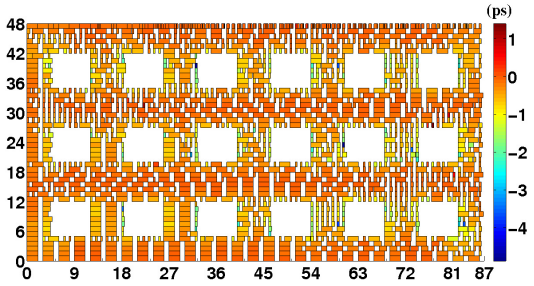
- The actual change on the critical path denoted by ΔD_{P1} can be more than the change in the worst case path delay observed at the circuit level shown in $\Delta D2$ in Table V.
- A noncritical path can become timing-critical when TSV effects are considered. This is observed by comparing the delays in D_{P1} and its percentage change, ΔD_{P1} in Table VII with the circuit critical path delay D2 and the circuit level change, $\Delta D2$ in Table V.
- The maximum delay degradation or improvement, given by ΔD_{P2} and ΔD_{P3}, respectively, among all paths is significantly greater than the worst case path delay changes observed at the circuit level.
- The negative [positive] changes in ΔTPS of the circuits reveal that a majority of paths experience delay degradation [improvement] and there is lower [more] positive slack available in the circuit under TSV effects.
- The wide distribution in the ΔTNS indicates that many non-critical paths in the circuit can violate timing constraints when TSV effects are taken into account.

Fig. 11 shows the color maps of the delay changes in PMOS and NMOS transistors in the gates for the spi circuit. The square white portions represent the TSV locations. Consistent with Figure 5, we see that maximum delay changes are observed in the horizontal and vertical regions between the TSVs. Furthermore, it can be observed that minimum delay variations occur in the regions diagonal to the TSVs. From the scales, it can be noticed that PMOS transistors tend to experience greater magnitude of delay variations than NMOS transistors. The effect of threshold voltage improvements seen in Fig. 8 suggests that for regions closer to the KOZ, mobility degradations are attenuated to an extent while mobility improvements are fortified. Since threshold voltage changes vanish after a short distance beyond KOZ, mobility variations are predominant at further distance from the KOZ. From the Fig. 11, it can be concluded that path delay degradations [improvements] are due to the gates placed in the horizontal [vertical] regions of the TSV. The effects are opposite when all the transistor channels are perpendicular to the [110] axis.

Short path variations: We examine the effects of TSV stress on short paths and hold time constraints, since it is possible for path delays to decrease under TSV effects, depending on



(a)



(b)

Fig. 11. spi (a) PMOS ΔDelay map (b) NMOS ΔDelay map.

TABLE VIII
MINIMUM PATH DELAY OF TSV_5_7 CIRCUITS WITH {TSV + BCB LINER} EFFECTS

Circuit	w/o TSV effects		with TSV effects	
	$D_{min}(ps)$	# Violations	$D_{min}(ps)$	# Violations
ac97_ctrl	22	998	22	984
aes_core	22	3802	22	3485
des	29	28	29	28
ethernet	22	2480	22	2448
i2c	22	80	22	73
mem_ctrl	22	500	22	449
pci_bridge32	22	4140	22	4045
spi	22	48	22	43
systemcdes	29	238	29	237
usb_funct	22	908	22	881

their placement relative to the TSVs. Table VIII shows the minimum path delays and the number of violations observed in the circuits without and with TSV effects. The minimum path delay in each case is denoted by D_{min} and we consider a minimum path delay requirement of 50 ps to report the number of path violations with and without TSV effects. We can see that, although the minimum path delay D_{min} remains same in the two cases, the number of path violations under TSV effects are reduced by different margins. Thus, during sequential circuit design in the presence of TSVs, the impact on minimum path delays should also be accounted for.

Layout guidelines: Based on this analysis, it has been demonstrated that the delay changes within the circuit are very significant, but their effects are attenuated at the outputs due to the effect of the max operation in timing analysis, which changes the critical path. This suggests that this freedom can be exploited by layout tools to "hide" the delay increases. Based on our analysis of stress patterns, we can draw the following general layout strategies that optimize delay:

- In general, to minimize the variations in gate-delays, the regions diagonal to the TSVs should be preferred.
- For paths that are timing-critical or near-critical, the gates should be placed in the vertical [horizontal] regions between TSVs when transistors are parallel [perpendicular] to the wafer flat.
- On paths with low minimum delay margins, the gates should be placed in the horizontal [vertical] regions between TSVs when transistors are parallel [perpendicular] to the wafer flat direction.

C. TSV-induced stress effects on leakage power

TSV-induced stress causes threshold voltage reductions in NMOS/PMOS transistors as seen in Section IV-C. Thus, the leakage power of the circuits are expected to degrade under TSV effects. To evaluate TSV effects on leakage power, we compare the leakage power of the TSV_7 layouts at room temperature (25°C), under TSV with SiO_2/BCB liner effects, with the TSVless layouts where the TSV-stress effects are not present. In Table IX, $L0$ denotes the leakage power in the TSVless layouts. Furthermore, the columns $L1$ and $L2$ [$\Delta L1$ and $\Delta L2$] represent the actual leakage power [changes in the leakage power] under TSV effects with SiO_2 and BCB liners, respectively. Obviously, here $\Delta L0$ is zero.

In Table IX, the positive changes in $\Delta L1$ and $\Delta L2$ indicate that leakage power is higher or degrades under TSV-induced stress effects. This shows that if TSV-induced threshold voltage is not taken into account, leakage power of the circuit is underestimated. The increase in leakage power when SiO_2 [BCB] liner is taken into account varies from 3.7% to 5.7% [2.5% to 3.8%]. Thus for the same TSV geometry and KOZ, a TSV with SiO_2 liner causes greater leakage degradations as compared to the BCB liner case. Since the TSV-induced stress with SiO_2 liner has a greater magnitude than the BCB liner case, the former liner case causes wider range of circuit timing and leakage power variations than the latter case.

TABLE IX
LEAKAGE POWER OF TSV_5_7 CIRCUITS

Circuit	w/o TSV	{TSV + SiO_2 liner}		{TSV + BCB liner}	
	$L0$ (mW)	$L1$ (mW)	$\Delta L1$ (%)	$L2$ (mW)	$\Delta L2$ (%)
ac97_ctrl	14.04	14.75	5.1%	14.52	3.4%
aes_core	14.72	15.32	4.1%	15.13	2.8%
des	6.3	6.61	4.9%	6.51	3.3%
ethernet	31.8	32.97	3.7%	32.59	2.5%
i2c	1.58	1.67	5.7%	1.64	3.8%
mem_ctrl	12.44	12.95	4.1%	12.79	2.8%
pci_bridge32	15.82	16.503	4.3%	16.28	2.9%
spi	4.44	4.63	4.3%	4.57	2.9%
systemcdes	3.96	4.15	4.8%	4.09	3.3%
usb_funct	14.73	15.29	3.8%	15.11	2.6%

VII. CONCLUSION

Through silicon vias cause layout-dependent electrical variations in 3D-IC circuits. We have developed a holistic framework that considers TSV-stress and other thermal effects on transistor electrical parameters. The analytical stress model presented in this work is shown to accurately capture the biaxial nature of the TSV-stress, with good agreement with FEA models. The stresses and strains thus obtained are employed to evaluate variations in gate and circuit level performance metrics. A thorough analysis of path delays is presented and the effects of TSV-stress on circuit leakage power is evaluated. Finally layout guidelines are suggested for improving timing performance in 3D-ICs.

APPENDIX

The fundamental equations from which the stress distributions in Table II are derived are presented here.

A. Basic equations of 2D-axisymmetric formulation

The TSV is modeled as a long copper cylinder surrounded by a thin liner and embedded in silicon at an annealing temperature of 250^{o}C. Under this scenario and due to the underlying assumptions, only the radial displacement u_r is constrained ($u_\theta = u_z = 0$) which under equilibrium satisfies the following governing equation:

$$\frac{d^2u_r}{dr^2} + \frac{1}{r}\frac{du_r}{dr} - \frac{u_r}{r^2} = 0$$

where, r is the distance from the center of the TSV. Subsequently, a general solution for the displacement can be obtained and the strains [stresses] are obtain from strain-displacement [Hooke's Law] relationships. Thus, for a material $M \in [Cu, Si, Liner = SiO_2/BCB]$ the axisymmetric stress state in cylindrical coordinates in terms of a general solution is given as:

- displacement:

$$\begin{aligned} u_r^M &= A^M r + \frac{B^M}{r} \\ u_\theta^M &= u_z^M = const. \end{aligned}$$

- strains:

$$\begin{aligned} \epsilon_{rr}^M &= \frac{\partial u_r^M}{\partial r} = A^M - \frac{B^M}{r^2}; \\ \epsilon_{\theta\theta}^M &= \frac{1}{r}\frac{\partial u_\theta^M}{\partial \theta} + \frac{u_r}{r} = A^M + \frac{B^M}{r^2}; \\ \epsilon_{zz}^M &= \frac{\partial u_z^M}{\partial z} = 0 \end{aligned}$$

- stresses:

$$\begin{aligned} \sigma_{rr}^M = \;& C^M[A^M - \frac{B^M(1-2\nu^M)}{r^2} - (1+\nu^M)\alpha^M\Delta T]; \\ \sigma_{\theta\theta}^M = \;& C^M[A^M + \frac{B^M(1-2\nu^M)}{r^2} - (1+\nu^M)\alpha^M\Delta T]; \\ \sigma_{zz}^M = \;& \nu^M(\sigma_{rr}^M + \sigma_{\theta\theta}^M); C^M = \frac{E^M}{(1+\nu^M)(1-2\nu^M)}. \end{aligned} \quad \text{(A.18)}$$

Here, the terms A^M, B^M represent the constants that need to be determined from the prescribed boundary conditions. The term C^M is a constant function of the mechanical parameters. The terms E^M, ν^M, and α^M denote the Young's modulus, Poisson's ratio, and the coefficient of thermal expansion (CTE) of the material M, respectively. The term $\Delta T = T - T_{ref}$ represents the temperature differential at an operating temperature of T with respect to the copper annealing temperature T_{ref} (250^{o}C). The values of physical constants used in this work are given in Table I. The constants A^M and B^M are obtained by satisfying the following boundary conditions:

I) at $r = 0$, $u_r^{Cu} = 0$.
II) at $r = \infty$, $\sigma_{rr}^{Si} = 0$ and $\sigma_{\theta\theta}^{Si} = 0$.
III) at $r = a$, $u_r^{Cu} = u_r^{Liner}$.
IV) at $r = a$, $\sigma_{rr}^{Cu} = \sigma_{rr}^{Liner}$.
V) at $r = b$, $u_r^{Liner} = u_r^{Si}$.
VI) at $r = b$, $\sigma_{rr}^{Liner} = \sigma_{rr}^{Si}$.

B. Boussinesq problem

Consider a uniform normal pressure P applied on the surface of a homogeneous half-space on a circular area of radius a. We are interested in the stress distributions outside this pressed area (silicon). For a material M the basic displacement distributions are given by [8]:

$$\begin{aligned} u_r &= -\frac{(1-2\nu^M)(1+\nu^M)}{2E^M}P\frac{a^2}{r} \\ u_z &= \frac{4\left(1-\left(\nu^M\right)^2\right)}{\pi E^M}Pr\left[K1\left(\frac{a}{r}\right) - \left(1-\frac{a^2}{r^2}\right)K2\left(\frac{a}{r}\right)\right] \end{aligned}$$

Here r is the distance on the surface from the center of the pressed area. The terms ν^M and E^M represent the Poisson's ratio and the Young's modulus of the material M respectively. The terms $K1(a/r)$ and $K2(a/r)$ denote the complete elliptical integrals of the first kind and the second kind, respectively. They can expanded by an infinite series in powers of the factor a/r. For $a/r < 1$, the elliptical integrals and their derivatives tend to zero. The corresponding strain components are given by:

$$\begin{aligned} \epsilon_{rr} &= \frac{\partial u_r}{\partial r} = \frac{(1-2\nu^M)(1+\nu^M)}{2E^M}P\frac{a^2}{r^2} \\ \epsilon_{\theta\theta} &= \frac{u_r}{r} = -\frac{(1-2\nu^M)(1+\nu^M)}{2E^M}P\frac{a^2}{r^2} \\ \epsilon_{zz} &= \frac{\partial u_z}{\partial z} = 0 \\ \epsilon_{rz} &= \frac{\partial u_z}{\partial r} + \frac{\partial u_r}{\partial z} \to 0 \text{ for } r > a \\ \epsilon_{r\theta} &= \epsilon_{\theta z} = 0 \end{aligned}$$

From Hooke's Law, we obtain the stress components:

$$\begin{aligned} \sigma_{rr} &= \frac{1-2\nu^M}{2}P(\frac{a^2}{r^2}) \\ \sigma_{\theta\theta} &= -\frac{1-2\nu^M}{2}P(\frac{a^2}{r^2}) \\ \sigma_{zz} &= \tau_{rz} = \tau_{r\theta} = \tau_{\theta z} = 0 \end{aligned} \quad \text{(A.19)}$$

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