# Probabilistic Wire Resistance Degradation due to Electromigration in Power Grids

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Abstract-Electromigration (EM) is a growing concern in on-chip interconnects, particularly in the computing and automotive domains. EM can cause wire resistances in a circuit to increase, which may result in circuit performance failure within the lifetime of a product. Classical circuit-level EM models have two drawbacks: first, they do not accurately capture the physics of degradation in modern copper dual-damascene (Cu DD) metallization, and second, they fail to model the inherent resilience in a circuit that may allow it to continue to function even after some wires fail. This work overcomes both limitations, and develops a method to analyze the effect of EM on the resistance of wires in a circuit. For a single wire, our probabilistic analysis encapsulates known realities about Cu DD wires, e.g., that some regions of these wires are more susceptible to EM than others, and that void evolution shows statistical behavior. We develop a new criterion for identifying mortal wires based on this analysis. One part of the criterion incorporates the achievement of steady state and provides a result that is slightly tighter than the traditional Blech criterion, while another part is tied to the lifetime of the system. We apply these ideas to the analysis of on-chip power grids and demonstrate the inherent robustness of these grids that maintains supply integrity under some EM failures.

*Index Terms*—Electromigration, copper, voids, power grid, probabilistic, lognormal, redundancy, resiliency.

#### I. INTRODUCTION

**E** LECTROMIGRATION (EM) in interconnects occurs due to the movement of metal atoms, activated by momentum transfer from collisions with free electrons [2]. When bounded by a blocking boundary, such as an encapsulating barrier layer that prevents metal diffusion in copper dual-damascene (Cu DD) wires, this movement causes a depletion of atoms at the cathode, which eventually leads to void nucleation and subsequent growth [3], [4]. Cu DD structures are particularly susceptible to EM since the critical stress for void nucleation in such wires is observed to be very small [5], and voids may form early in the lifetime of a design.

While there has been intensive research on understanding the physics and modeling of EM at the level of a single

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interconnect, there is a large gap between what is known at this physical level and the knowledge that is used at the circuit level. Traditional EM analysis is based on failure criteria measured under accelerated aging conditions through the application of temperature and current stress in a set of interconnect test structures. Under such conditions, failure is deemed to occur when the interconnect resistance crosses a predetermined threshold, and the time at which this occurs is defined as its time-to-failure. The time-to-failure parameters from accelerated aging conditions (of the order of hours) are extrapolated to normal operating conditions (of the order of years) using Black's equation [6].

For a specific circuit, EM failure criteria may be derived by a circuit designer. In the traditional design flow, some wires in a circuit may be considered immortal, i.e., immune to EM. The root cause of immortality is related to a back-stress that is created after the movement of atoms due to EM, which induces a back-flow of atoms to counteract the forward EM-induced atomic flow: when these two balance, the wire is immortal. The Blech criterion [7] states that for a wire with current density j and length L, if the product (jL) is below a threshold, then it is immortal. For mortal wires that do not satisfy the Blech criterion, Black's equation is applied to derive maximum current density limit rules, declaring a wire as having failed if it does not adhere to the limit.

There are several problems with such an approach. First, in a real circuit, the impact of such failures is context-dependent. In some cases, small changes in resistance may cause performance failures in the circuit even before the resistance crosses a large threshold, e.g., on critical paths in a clock and data networks in circuits [8]. In other cases, a large failure may be tolerated due to the inherent resilience in the circuit, e.g., due to redundancy in a power grid, where the failure of one wire may be compensated by current flow through other paths, which results in a more resilient performance of the circuit [1], [9]. Therefore, the use of a single threshold for the resistance change may either be excessively conservative, or not conservative enough, depending on how the threshold is chosen and on the sensitivity of circuit failure to a resistance change in a specific interconnect. Second, for Cu DD interconnects, complexities in the manufacturing process imply that a straightforward extension of prior EM approaches is untenable. A previous study has indicated that the Blech criterion based approach, which was originally derived for aluminum interconnects, is not valid for copper interconnects, and that some lines fail probabilistically even if they satisfy the Blech criterion on the value of their jL product [5], [10].

These peculiarities for Cu DD wires indicate the need to

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develop EM models that incorporate the physics specific to such interconnects, and to enable probabilistic circuit analysis in a context-sensitive manner. The probabilistic viewpoint reflects both the fact that EM mechanisms are stochastic, and that the number of interconnects on a chip is large enough that these effects may be manifested over the chip.

There have been few prior publications that have explored these directions. The work in [11] built up on [12] to consider some EM issues beyond the conventional Black's equation, but it was partly based on the traditional Blech criterion. The resilience of power grids to EM due to structural redundancies has been utilized in the industry, and has been pointed out in the precursor to this paper [1], which is based on a physics-based statistical method. The idea of accounting for redundancy in power grids while analyzing EM was subsequently also used in [13], [14], but these methods were primarily based on Black's equation. The work in [9] uses a physics-based model that incorporates the role of mechanical stress. The authors indicate that the variation in EM lifetimes is caused due to the variation in the structure of the metal interconnect at the microscopic level, i.e., its microstructure. Their consideration of the statistical nature of EM focuses on evaluating the mean of the EM-induced circuit performance shift, and the variation in the circuit performance shift due to probabilistic EM-induced degradation is not captured.

We propose a probabilistic EM analysis framework that incorporates the impact of variation in the material properties of the interconnect on EM performance of a circuit. Starting from the known distributions of parameters related to the microstructure, such as activation energy and grain size, our framework uses an analytical model to predict the distribution of EM-induced void growth and consequently, the EM-induced resistance change in the wire. A new mortality criterion is developed, based on the underlying statistics that drive EM. Based on the distribution of the change in the wire resistance, we calculate the circuit performance degradation by observing the IR drop variation in standard power grid benchmarks.

Next, we overview the physics of EM in Section II, wherein we discuss the material, circuit, and environmental parameters that influence the EM-induced void dynamics. Our EM model, described in Section III, incorporates the variation in interconnect microstructure parameters that influence void dynamics, and thereby predicts the probabilistic evolution of EM-induced voids and the consequent probabilistic change in resistance. Our new mortality criterion is presented here. The impact of EM-induced wire resistance change on circuit performance parameters is observed by performing Monte Carlo (MC) circuit simulation, as discussed in Section IV. In Section V, we numerically evaluate our approach, and then conclude the paper in Section VI.

#### II. EM MODELS

The fundamental phenomenon responsible for EM in metal interconnects consists of the electron wind force that drives atoms from the cathode end of the wire to the anode. This force is caused by transfer of momentum from moving electrons to the atoms as current flows [6]. The electron wind force,  $F_e$ , is

a function of the electric field and material properties of the interconnect and has the form

$$F_e = eZ_{eff}^{\star} E = eZ_{eff}^{\star} \rho j \tag{1}$$

where e is the elementary electron charge,  $Z_{eff}^*$  is a constant that represents the apparent effective charge number, and  $E = \rho j$  is the electric field, where  $\rho$  is the resistivity of Cu and, as before, j is the current density through the wire. The electron wind force makes it possible for thermally-activated metal atoms to be displaced from their lattice sites and to move in the direction of electron flow through one or more diffusion pathways, producing regions of uneven atomic concentration, i.e., depletion and accumulation. The drift velocity,  $v_d$ , of atoms moving due to the electron wind is

$$v_d = \mu_e F_e \tag{2}$$

where  $\mu_e$  is the mobility of metal atoms. The atomic flux due to the electron wind force from the cathode to the anode is given by [2]

$$Nv_d = N\mu_e F_e \tag{3}$$

where N is the atomic density. Further, using the Nernst-Einstein relation as discussed in [15], we have

$$\mu_e = \frac{D_{eff}}{k_B T} \tag{4}$$

where  $D_{eff}$  is the effective diffusivity for EM,  $k_B$  is Boltzmann's constant, and T is the temperature. Using (1), (2), and (4), the drift velocity can be rewritten as

$$\nu_d = \frac{D_{eff}}{k_B T} \left( e Z_{eff}^{\star} \rho \, j \right) \tag{5}$$

and the atomic flux due to electron wind in (3) becomes

$$N\left(\frac{D_{eff}}{k_BT}\right)\left(eZ_{eff}^{\star}\rho j\right) \tag{6}$$

The diffusion of atoms causes metal depletion at the cathode, resulting in tensile stress, and accumulation at the anode, resulting in compressive stress. This stress gradient results in a stress-induced backflow of atoms, from the anode (site of compressive stress) to the cathode (site of tensile stress), i.e., in a direction that opposes the flux due to the electron wind [7]. The magnitude of this reverse atomic flux is given as

$$N\left(\frac{D_{eff}}{k_BT}\right)\left(\Omega\left|\frac{\partial\sigma_H}{\partial x}\right|\right) \tag{7}$$

where  $\Omega$  is the atomic volume,  $\sigma_H$  is the hydrostatic stress, and  $\left|\frac{\partial \sigma_H}{\partial x}\right|$  represents the stress gradient along the line as a result of mass transfer from cathode to anode. Therefore, combining (6) and (7), the net atomic flux due to the combined effect of electron wind and back-stress is formulated as

$$J_{\rm flux}^{\rm EM} = N \frac{D_{eff}}{k_B T} \left( e Z_{eff}^{\star} \rho \ j - \Omega \left| \frac{\partial \sigma_H}{\partial x} \right| \right) \tag{8}$$

#### A. EM diffusion in Cu DD

We begin by outlining a typical Cu DD process. At the position where the wire is to be located, a trench is first etched into the interlayer dielectric (ILD). Next, a Ta-based barrier is deposited therein, and the Cu used to construct the interconnect is then deposited within the trench. The role of the barrier is to prevent Cu from diffusing into the ILD. Finally, the lines are capped above by a silicon nitride  $(Si_XN_Y)$  layer.



Figure 1: Cu DD interconnect cross-section showing possible atomic diffusion paths.

The structure of a Cu DD interconnect is key to understanding the effective diffusivity,  $D_{eff}$ , an important parameter in (8) that affects EM-induced performance degradation. This parameter can be considered as the sum of the contributions of atomic transport along various diffusion paths. These diffusion paths are a function of the microstructure of the interconnect, which is the arrangement of grains, i.e., regions of similar physical properties that are visible at microscopic levels of magnification. Figure 1 is a schematic that illustrates the cross-section of a Cu DD interconnect, showing grains within the metal wire and the regions of intersection of the grains, known as the grain boundaries. The diffusion pathways available for the migration of metal atoms are as follows

- along the grain boundaries (GB),
- through the bulk volume (BV),
- through the nonideal Ta barrier interface (I), and
- through the capping surface (S).

For a line of height h and width w,  $D_{eff}$  can be considered as a sum of contributions of atomic transport along these four pathways, and can be modeled as [16]

$$D_{eff} = D_I \delta_I \left(\frac{2}{w} + \frac{1}{h}\right) + D_S \delta_S \left(\frac{1}{h}\right) + D_{GB} \delta_{GB} \left(\frac{1}{d}\right) + n_{BV} D_{BV}$$
(9)

where the subscripts correspond to the diffusion pathway,  $D_I$ ,  $D_S$ ,  $D_{GB}$ , and  $D_B$  are diffusion constants,  $\delta_I$ ,  $\delta_S$ , and  $\delta_{GB}$  denote the effective thicknesses, d is the grain size along the longitudinal direction (Figure 1 shows  $d_i$  which is the grain size of the  $i^{\text{th}}$  grain), and  $n_{BV}$  is the fraction of atoms diffusing through the bulk volume.

Typically, it has been observed that the bulk and interface diffusion contribution can be neglected compared to diffusion along the capping surface and grain boundaries [15]. Furthermore, depending on the properties of the interconnect microstructure, additional terms can be omitted. For instance, the grain boundary component can be neglected in interconnects that have a bamboo-like grain structure wherein the grain boundaries are perpendicular to the width of the wire [15] and there is no continuous path for EM-induced atomic diffusion.

For previous technology nodes, the Cu microstructure was composed of bamboo-like grains, rendering surface diffusivity as the dominant EM diffusion mechanism. However, recently it is observed that the Cu microstructure has become increasingly polygranular, with a mixture of bamboo-like and polycrystalline microstructure. At present technology nodes, the Cu microstructure is dominated by fine grains, resulting in a largely polycrystalline structure [17]. This polycrystalline structure introduces a large number of grain boundaries, adding more potential paths for grain boundary diffusion. Additionally, process enhancements such as the introduction of CoWP as an alternative material to  $Si_XN_Y$ , have retarded the electromigration diffusion along the capping surface [18]–[20]. Therefore, for advanced technologies, the primary diffusion path for EM is along the grain boundaries.

The correct expression to be used for EM modeling depends on the context with respect to the microstructure of the wire. In this work, we compare our results against the 3-D EM model based simulation work in [4] in Section V-A that performs statistical EM analysis for single Cu DD interconnects, using Finite Element Analysis (FEA) for simulating void nucleation, supplemented with a compact modeling approach for void growth. For comparison with the FEA results in [4], we assume surface diffusion is the dominant component since those simulations are performed on wires with a bamboo-like grain structure. In contrast, for our power grid simulations in Section V-B, we assume the grain boundary diffusion as the dominant component in order to be consistent with the process conditions in state-of-the-art technologies, where as noted above, the microstructure is observed to be polygranular.

# B. EM-induced void evolution

There are multiple approaches that can be used for modeling the physics of EM in circuits. The most popular approach is based on the work from Korhonen [3]. Recent works in power grid analysis have proposed EM modeling approaches based on evolution of vacancy and plated atom concentrations, e.g., the model used in [9]. In this work, we will use the model from [3], commonly referred to as the Korhonen model.

The Korhonen model uses the atomic flux relation in (8) in conjunction with the continuity equation to represent the dynamics of EM atomic flow in interconnects. The dynamic interplay between electron wind and back-stress forces is described by a differential equation, given as

$$\frac{\partial \sigma_H}{\partial t} = \frac{\partial}{\partial x} \left[ \kappa \left( \frac{\partial \sigma_H}{\partial x} + G \right) \right] \tag{10}$$

where  $\kappa = \frac{D_{eff} B \Omega}{k_B T}$ ,  $G = \frac{eZ_{eff} \rho j}{\Omega}$ , and *B* is the effective bulk modulus for the Cu and interlayer dielectric system; other terms have been defined previously in Section II.

The work in [3] also proposes solutions to this differential equations under appropriate boundary conditions, the first one corresponding to a semi-infinite approximation of a wire, and the other corresponding to a finite length wire. The resulting analytical formulae can help to predict the conditions for formation and growth of EM-induced voids in a wire, and constitute the foundation for EM physical models in older Al and current-day Cu interconnect metallization technologies [4], [12]. For both Al and Cu, experiments indicate that EM failure in Cu interconnects occurs in two phases, in agreement with the Korhonen model [4], [21]. According to this, voids evolve in two phases:

- *Void nucleation*: Under EM, the depletion of atoms at the cathode creates a tensile stress. Once this exceeds a critical stress threshold value, the void nucleates.
- *Void growth*: After nucleation, further movement of metal atoms from the void results in void growth, resulting in increased wire resistance since the void effectively reduces the cross-section available for current flow.

For void nucleation, we choose the solution from [3] corresponding to the semi-infinite wire. We make this choice because the semi-infinite solution has a simple form which is easy to compute, is guaranteed-pessimistic, and closely matches the accurate stress solution in the region of interest for power grids, where wire lengths can go up to hundreds of microns. The analytical solution from [3] states that the time,  $t_n$ , at which a void nucleates.

$$t_n = \frac{K_{t_n}}{D_{eff}} \tag{11}$$

where 
$$K_{t_n} = \frac{\pi}{4} \left( \frac{\sigma_c^2 \Omega k_B T}{(e Z_{eff}^{\star} \rho j)^2 B} \right)$$
 (12)

where  $\sigma_c$  is the effective critical stress for void nucleation. After nucleation, the void begins to grow. Various void growth scenarios have been observed in Cu DD structures, depending on the direction of the current [12]. The scenario where the electron flow is downwards, shown in Figure 2(a) corresponds to the via-above case (i.e., the via is located above the void), and results in potential void formations at the via or in the wire, as illustrated. For the case where the electron flow is upwards, shown in Figure 2(b), an upstream void is potentially formed in the upper wire, typically at a corner of the wire or within the wire, as shown (i.e., the via is located below the void). Through process enhancements, voids inside the via trench have been resolved [22] and are not considered here.

The mechanics of void formation in each case – spanning growth (for both the via-above and via-below cases), when the void spans the entire interconnect, and *slit growth*, where it forms along the via (for the via-above case) - is different and necessitates different modeling approaches. Although slit voids tend to form earlier than spanning voids, it is easy to build redundancy into the power grid to guard against slit voids by inserting redundant vias; in fact, this is often implemented during the wire routing stage. Moreover, recent process enhancements in Cu DD metallization technology, such as the introduction of new barrier technologies [23] completely mitigate the possibility of slit void formation. Therefore, we focus our attention on the impact of spanning voids. For spanning voids, once a void is formed, the primary mechanism of growth in the void size is due to drift under an electron wind force, with a constant drift velocity  $v_d$  [4], [24].



(b) Via-below case.

Figure 2: Mechanisms of void evolution for the via-above and via-below cases (microstructure not shown for simplicity).

If the void nucleates at time  $t_n$ , then at an observation time  $t_o$ , the void has been growing for a length of time,  $t_o - t_n$ . The length of the void increases due to drift, as given by

$$L_{void}(t_o) = v_d \cdot (t_o - t_n) = \left(\frac{D_{eff}}{k_B T}\right) e Z_{eff}^{\star} \rho \ j \ (t_o - t_n) \ (13)$$

where the second equality follows from (5).

The set of equations for EM dynamics are computationally efficient, and the stress predicted is pessimistic [3]. This has been the basis of its usage in other circuit analysis works such as [11], [12]. Although, these equations are valid for single isolated interconnects, in power grid circuits the interconnects are connected through vias. In Section III-D, we illustrate that the impact of current flowing through neighboring wires can be modeled using the idea of current divergence.

# C. Effect of temperature

At first sight, if we observe the temperature dependence of the nucleation time,  $t_n$ , drift velocity,  $v_d$ , and void length,  $L_{void}$ , in (5), (11), and (13), we notice that  $t_n$  appears to increase, while  $v_d$  and  $L_{void}$  reduce as temperature increases. However, accelerated temperature EM experiments indicate the opposite trends. This apparent anomaly is explained by examining the exponential dependence of EM diffusivity on temperature [12]

$$D_{eff} = D_0 \exp\left(-\frac{E_a}{k_B T}\right) \tag{14}$$

where  $D_0$  depends on the microstructure of the wire, as discussed in Section II-A, and  $E_a$  is the activation energy for EM diffusion, which signifies the amount of energy that a thermally activated metal atom must gain in order to dislocate from its lattice site and migrate in the direction of electron flow along the dominant diffusion path(s). Alternatively,  $E_a$ represents the energy barrier that a thermally activated metal atom needs to overcome in order to dislocate and move in the direction of electron flow.

Observing the form of (14), it is clear that as the temperature increases, there is an exponential increase in

effective diffusivity, thus resolving the apparent anomaly in (5), (11), and (13) reported above, and showing that EM causes more damage at higher temperatures.

In fact, the above argument shows that small perturbations in T can offset EM calculations significantly, and using an accurate temperature value is of utmost importance in order to accurately analyze performance degradation due to EM. In a circuit context, current flow in a wire can result in Joule heating, which causes an increase in the temperature and thereby accelerates EM. Therefore, to quantify the performance impact of EM accurately, the temperature increase due to Joule heating must be accounted for.

We use the model described in [25] to evaluate the interconnect temperature due to Joule heating given as

$$T = T_{\rm ref} + \Delta T_J \tag{15}$$

where  $T_{\text{ref}}$  is the reference temperature of the interconnect, and  $\Delta T_J$  depends on the RMS current through the wire [25]

$$\Delta T_J = I_{rms}^2 R R_\theta \tag{16}$$

where R is the wire resistance and  $I_{rms}$  is the RMS current flowing through the interconnect. In our case, since the logical blocks which drive current are assumed to have steady state DC currents, therefore, the RMS current flowing through the wire is taken as the corresponding DC current. The parameter,  $R_{\theta}$ , represents the thermal impedance and is given by

$$R_{\theta} = \frac{t_{\rm ins}}{K_{\rm ins} \ L_{wire}(w + 0.88t_{\rm ins})} \tag{17}$$

where  $t_{ins}$  is the thickness of the dielectric below the interconnect and is a function of the metal layer occupied;  $K_{ins}$  is the thermal conductivity;  $L_{wire}$  and w denote the length and the width of the wire, respectively.

#### III. PROBABILISTIC MODELING OF EM FAILURE

The conventional explanation of EM in Al interconnects was predicated on the interaction between the electron wind force and the back-stress force. For some interconnects, with low current and/or small length, the two forces could be in equilibrium in the steady state so that the critical stress  $\sigma_c$  for void nucleation is never reached, implying that these wires are immortal to EM effects. For a wire of length L with current density *i*, the Blech criterion for immortality can be derived from (8) by considering the steady state with respect to stress where the stress does not change with respect to time and the forward and backward flux are in equilibrium. In this state, it can be shown from (10) that the stress profile settles to a linear relationship where  $\partial \sigma_H / \partial x = 2\sigma_{peak}/L$ . Here,  $\sigma_{peak}$ denotes the stress at the cathode when steady state is achieved. A wire is immortal at equilibrium if  $\sigma_{peak} \leq \sigma_c$ , which implies that the stress is below the critical stress for void nucleation. From (8), this occurs when  $eZ_{eff}^{\star} \rho j \leq 2\Omega \sigma_c/L$  [7], i.e.,

where

$$jL \le (jL)_{crit} \tag{18}$$

$$(jL)_{crit} = 2\Omega\sigma_c/eZ_{eff}^{\star}\rho \tag{19}$$

Clearly,  $(jL)_{crit}$  is a property of the material and the fabrication process. However, as noted in Section I, it has been observed that the immortality property does not always hold for Cu DD interconnects. This can be attributed to the observation of lower value of critical stress,  $\sigma_c$  for Cu DD compared to Al interconnects, which results in voids being formed easily, and lines are apt to show probabilistic behavior [5], [10]. In effect, every line has a nonzero probability of failure, regardless of its jL value and it is possible for voids to nucleate early, before providing the opportunity for opposing back-stress forces to build up.

This nonzero failure probability is our motivation for using an analytical model for probabilistic EM. Void evolution characteristics, which are required to calculate the EM-induced probabilistic resistance increase, are imported from the nucleation and growth model formulae [3], [26] discussed in Section II-B. Unlike the Blech criterion, these formulations consider the transient as well as the steady state for stress.

We construct our model by attributing the causes of variation to fundamental material parameters that impact the EM-induced void nucleation and growth, characterized by (11) and (13). In the remainder of this section, we will derive the formulae that predict the statistics of EM-induced void evolution as a result of the possible sources of variation. This analysis will allow us to evaluate the resistance change as a result of nucleation and growth of voids.

#### A. The role of microstructure in probabilistic EM behavior

Recent works have observed that EM failure is correlated to uncertainties in the microstructure parameters of an interconnect, which relate to the statistical distribution of the activation energy [4] and/or grain size [27].

1) Activation energy variation: As discussed in Section II-C, the activation energy,  $E_a$ , is a property of the microstructure. It has been experimentally observed that  $E_a$  can vary within the wire depending on the grain boundary orientation. For instance, EM activation energy can vary between grains depending on the orientation of the grain with respect to each other and with respect to the interfacial layer [28], [29]. Therefore, we work with the idea of the effective activation energy for each wire, which is an averaged activation energy value for that wire. In the rest of this paper, we use  $E_a$  to refer to the effective activation energy for each wire, taken at a macroscopic level. This parameter has been experimentally found to be normally distributed, and we model it as an independent Gaussian random variable; further, it is reasonable to assume that the effective activation energy is same for a wire and varies only between the wires [4], [28], [30]–[33].

2) Grain size variation: Experiments in [27] have shown a correlation between the experimental EM lifetimes and another microstructure property, the effective grain size, defined as the grain size value averaged over all grains in a wire.

# B. Statistical models for void dimensions

Based on the assumptions mentioned in the previous section about  $E_a$  and d, we will now present a probabilistic framework that will enable us to obtain the EM-induced void characteristics and the corresponding resistance change as a result of void nucleation and growth.

In our discussion below, for a distribution  $Z = N(\mu, \sigma)$  with the mean  $\mu$  and standard deviation  $\sigma$ , we denote a lognormal  $X = e^{Z}$  as  $\text{LogN}(\mu, \sigma)$ .

**Effective diffusivity:** The effective diffusivity,  $D_{eff}$ , plays a key role in the EM degradation of Cu DD wires, as discussed in Section II-A, and affects the physics of void nucleation and growth, as indicated in (11) and (13), respectively. Therefore, we investigate the statistics of  $D_{eff}$ .

As indicated in Section II-A, the primary diffusion mechanism in modern Cu DD interconnects is grain boundary (GB) diffusion. Due to this, the parameter  $D_0$  in (14) is determined by this mechanism. Neglecting the other mechanisms and considering the dominant term corresponding to the grain boundary mechanism in (9), we have

$$D_0 = D_{0GB} \left(\frac{\delta_{GB}}{d}\right)$$
  
or  $\log D_0 = \log \left(D_{0GB}\delta_{GB}\right) - \log d$  (20)

where  $D_{0GB}$  is a temperature independent constant. This shows that  $D_0$  is a random variable that depends on the effective grain size, d, which follows a lognormal distribution [27], i.e.,  $d = \text{LogN}(\mu_d, \sigma_d)$ , where  $\mu_d$  and  $\sigma_d$ represent the mean and standard deviation of the underlying Gaussian,  $\log d$ . Specifically,  $D_0 = \text{LogN}(\mu_{D_0}, \sigma_{D_0})$ , where the mean,  $\mu_{D_0} = \log(D_{0GB}\delta_{GB}) - \mu_d$  and the standard deviation,  $\sigma_{D_0} = \sigma_d$ .

Therefore, to model the variation in  $D_{eff}$ , we use the above, and the fact that  $E_a$  for a wire follows a Gaussian distribution. From (14), it is obvious that  $D_{eff}$  is the product of two lognormals, one attributable to  $D_0$  (via d) and the other attributable to  $E_a$ , and such a product results in a lognormal distribution. If  $E_a = N(\mu_{E_a}, \sigma_{E_a})$ , then  $D_{eff} = \text{LogN}(\mu_{D_{eff}}, \sigma_{D_{eff}})$ , where

$$\mu_{D_{eff}} = \log \left( D_{0GB} \delta_{GB} \right) - \mu_d - \frac{\mu_{E_a}}{k_B T}$$
(21)  
$$\sigma_{D_{eff}}^2 = \sigma_d^2 + \left( \frac{\sigma_{E_a}}{k_B T} \right)^2$$

The diffusion pathways during nucleation and growth may be different [4]. We refer to the effective diffusivity for the nucleation and growth phases as  $D_{eff,n}$  and  $D_{eff,g}$ , respectively, and next, we consider the impact of each of these individually. **Nucleation:** The expression for nucleation time  $t_n$  was provided in (11). From this, it is clear that  $t_n =$  $LogN(\mu_{t_n}, \sigma_{t_n})$ , where

$$\mu_{t_n} = \log(K_{t_n}) - \mu_{D_{eff,n}}$$
(22)  
$$\sigma_{t_n} = \sigma_{D_{eff,n}}$$

the above result relies on the observation that the distribution of a reciprocal of a lognormal  $\text{LogN}(\mu, \sigma)$  is another lognormal characterized as  $\text{LogN}(-\mu, \sigma)$ .

**Growth:** During void growth, the length of a void evolves with time according to (13). Grouping together all deterministic parameters in this equation, if a void nucleates, then from

(13), its length at given observation time, 
$$t_o$$
, has the form

$$L_{void}(t_o) = c_1 D_{eff,g} - c_2 t_n D_{eff,g}$$
(23)

where  $c_1 = (eZ_{eff}^*\rho jt_o)/k_BT$  and  $c_2 = c_1/t_o$ . The first term,  $c_1 D_{eff,g}$ , is lognormal, since  $c_1$  is a deterministic constant and  $D_{eff,g}$  is lognormal, and the product of a lognormal random variable with a scalar results in another lognormal random variable; the second term,  $c_2 t_n D_{eff,g}$  is a scaled product of lognormals, which is also a lognormal.

Therefore,  $L_{void}(t_o)$  is a difference of two correlated lognormals,  $c_1 D_{eff,g}$  and  $c_2 t_n D_{eff,g}$ . The difference of two lognormal random variables is approximated by a lognormal using a moment matching approach, similar to the widely-used Wilkinson approximation [34], which has been used to approximate the sum of two correlated lognormal random variables. The correlation between the random variables  $c_1 D_{eff,g}$  and  $c_2 t_n D_{eff,g}$  is required for evaluating the statistics, and the correlation coefficient r can be evaluated as

$$= c_1 c_2 \frac{\text{mean}(t_n) \text{variance}(D_{eff,g})}{\sqrt{\text{variance}(c_1 D_{eff,g}) \text{variance}(c_2 D_{eff,g} t_n)}}$$

r

 $\mu_{.}$ 

 $\sigma$ 

where the mean() and variance() for the corresponding lognormal variables. From (21) and (22), which provide the mean and variance of the underlying Gaussians, it is easy to compute these quantities. Specifically, if  $\mu_X$ ,  $\sigma_X$  ( $\mu_Y$ ,  $\sigma_Y$ ) are the mean and standard deviation of the underlying normal distribution for  $c_1 D_{eff,g}$  ( $c_2 t_n D_{eff,g}$ ) then we have

$$\begin{split} \mu_X &= \log c_1 + \mu_{D_{eff,n}} & \sigma_X = \sigma_{D_{eff,n}} \\ \mu_Y &= \log c_2 + \mu_{D_{eff,g}} + \mu_{t_n} & \sigma_Y = \sqrt{\sigma_{D_{eff,g}}^2 + \sigma_{t_n}^2} \end{split}$$

In order to find the analytical expression for the distribution of void length,  $L_{void}(t_o) = \text{LogN}(\mu_{L_{void}(t_o)}, \sigma_{L_{void}(t_o)})$ , we can use the above set of equations to compute the parameters of the distribution by applying the moment matching approach used in Wilkinson approximation. This will lead to the following set of equations

$$u_{1} = e^{\left(\mu_{X} + \sigma_{X}^{2}/2\right)} - e^{\left(\mu_{Y} + \sigma_{Y}^{2}/2\right)}$$

$$u_{2} = e^{\left(2\mu_{X} + 2\sigma_{X}^{2}\right)} + e^{\left(2\mu_{Y} + 2\sigma_{Y}^{2}\right)}$$

$$- 2e^{\left(\mu_{X} + \mu_{Y} + \frac{\left(\sigma_{X}^{2} + \sigma_{Y}^{2} + 2r\sigma_{X}\sigma_{Y}\right)}{2}\right)}$$

$$L_{void}(t_{o}) = 2\log(u_{1}) - \log(u_{2})/2$$

$$L_{void}(t_{o}) = \log(u_{2}) - 2\log(u_{1})$$

### C. Statistics of the EM-induced resistance change

We will now use the void length distribution to evaluate the distribution of resistance change due to EM-induced growth of a spanning void. For the case of the spanning void, the change in resistance,  $\Delta R$ , is given as [24]

$$\frac{\Delta R}{R_0} = \left(\frac{\rho_{Ta}}{\rho_{Cu}}\frac{A_{Cu}}{A_{Ta}} - 1\right)\frac{L_{void}(t_o)}{L_{wire}}$$
(24)

Here,  $\rho_{Cu}$  and  $\rho_{Ta}$  are, respectively, the resistivities of copper and tantalum,  $R_0 = \rho_{Cu}L_{wire}/A_{Cu}$  is the resistance of the interconnect wire segment, which is assumed to have length  $L_{wire}$  and cross-sectional area  $A_{Cu}$ , and  $A_{Ta}$  is the cumulative cross-sectional area of the tantalum barrier. Recall that the void length at time  $t_o$ ,  $L_{void}(t_o)$ , was shown in Section III-B to be lognormally distributed after nucleation. If we introduce a new symbol,  $k_B$ , defined as

$$k_R = \left(\frac{\rho_{Ta}}{\rho_{Cu}} \frac{A_{Cu}}{A_{Ta}} - 1\right) \frac{R_0}{L_{wire}},\tag{25}$$

we can rewrite (24) as

$$\Delta R = k_R \ L_{void}(t_o) \tag{26}$$

Since  $k_R$  is constant in (26), it can be seen that for a spanning void, for both the via-above and via-below cases,  $\Delta R$  is lognormal, since it is the product of a lognormal random variable with a scalar. The resistance change distribution can then be expressed as  $\Delta R = \text{LogN}(\mu_{\Delta R}, \sigma_{\Delta R})$ , where  $\mu_{\Delta R}$  and  $\sigma_{\Delta R}$  are the mean and standard deviation of the underlying Gaussian, given by

$$\mu_{\Delta R} = \mu_{L_{void}(t_o)} + \log k_R$$
(27)  
$$\sigma_{\Delta R} = \sigma_{L_{void}(t_o)}$$

We summarize the conditions that must be satisfied to achieve a resistance change of  $\Delta R$  at an observation time  $t_o$ . First, a void must nucleate, and then this nucleated void must grow to the point where the wire resistance increases by  $\Delta R$ . Using these notions, we can now determine the probability that a given wire will have a resistance change  $\Delta R$  as

$$\Pr\left(\Delta R\right) = \begin{cases} \Pr\left(\Delta R \mid \mathsf{nuc}\right) \cdot \Pr\left(\mathsf{nuc}\right) & \text{if } \Delta R > 0\\ 1 - \Pr\left(\mathsf{nuc}\right) & \text{if } \Delta R = 0 \end{cases}$$
(28)

The first case corresponds to a nonzero resistance change, i.e., the product of  $Pr(\Delta R \mid nuc)$ , the probability of a resistance change given that nucleation has occurred, and the probability of nucleation, Pr(nuc). The probability distribution for  $\Delta R$  for a nucleated void is given by  $LogN(\mu_{\Delta R}, \sigma_{\Delta R})$ as derived above, with the mean and standard deviation given by (27). The nucleation probability is given by  $LogN(\mu_{tn}, \sigma_{tn})$ in (22), and Pr(nuc) corresponds to the probability that the nucleation time,  $t_n$ , is less than the observation time,  $t_o$ , i.e., the cumulative distribution function (CDF) of  $t_n$ , evaluated at time  $t_o$ . The second case corresponds to the scenario where the void does not nucleate, with a probability of 1 - Pr(nuc).

### D. Incorporating the effect of current divergence

The conventional approach to estimating EM failure is based on a current density-based model. Under this model, for two wires of equal length, the one with the larger current density should have a shorter mean time to failure. However, the work in [35] demonstrated experimentally that this is not always the case, by showing test circuit where one wire has twice the current density as another, but experiences consistently later failures. This is consistent with other reported work where the *current divergence* effect comes into play: for example, [36] shows fabricated test structures where the failure rates on a wire segment depends not only on the current density on the segment, but also on those on adjacent segments that share via(s) with this segment. We model adjacent segments by computing the effective current density on a wire, which is based on the magnitude and directions of currents in neighboring wires. The effective current density for a wire is computed in terms of the flux-divergence criterion, similar to the work in [35]. This is illustrated in Figure 3, which shows two wires on metal layers  $M_x$  and  $M_{x+1}$  connected by a via. A via in a Cu DD interconnect structure acts as a blocking layer so that metal atoms are not permitted to migrate through it. Therefore, any flux that would have gone to the via is transmitted to a neighboring wire.



Figure 3: A via-tree structure where the effective current density is more than the density of current flowing through the wire.

In this example, the current on both segments of the wire on layer  $M_x$  flows towards the via, i.e., the electron flow direction is away from the via for both segments. Assuming equal current densities j on each segment, this implies that there is an effective divergence, which can eventually lead to void nucleation and growth, equivalent to a current density of 2j on both wires. In other words, as compared to the case where the left-hand segment is missing and the right-hand segment has the same current density of j, the expected rate of atomic transfer is doubled at this node. Using the via node vector notion [35], an effective current density of 2j is used for this wire instead of the actual current density of j.

## E. Mortal wire prediction

The Blech criterion, outlined in Section III, is predicated on the achievement of a steady state between the electron wind and back-stress forces, so that the stress gradient settles to a linear trend in space. The achievement of steady state requires significant mass transfer from the cathode to anode to balance the forward EM flux, and strictly speaking, immortality prediction by the Blech criterion cannot be guaranteed unless this steady state is reached soon. The observation that a finite time, which may be comparable to circuit lifetime, is elapsed before the achievement of steady state, can be backed up by experimental data, based on extrapolating experimental EM and back-stress results from [37], which observe the time elapsed for achievement of back-stress, in Cu wires of multiple wire lengths.

According to [3], the approximate time taken to reach steady state can be written as

$$t_{ss} = \frac{L^2}{4\kappa} \tag{29}$$

where  $\kappa = \frac{D_{eff} B \Omega}{k_B T}$ , as in Equation (10). For wires where the steady state may not be achieved, we propose an alternate void-nucleation-based mortality criterion, considering three cases:

**Case I**: A wire can be EM-mortal if it does not satisfy the Blech criterion  $(jL < (jL)_{crit})$ . For mortal wires, we have

$$jL > (jL)_{crit} \tag{30}$$

**Case II:** A wire can be EM-mortal if a void can nucleate before steady-state is achieved, i.e.,  $t_n < t_{ss} = L^2/4\kappa$ . Since  $\kappa = (D_{eff} B \Omega/k_B T)$ , from Equations (11) and (12),

$$\frac{\pi}{4} \left( \frac{\sigma_c^2 \ \Omega \ k_B T}{(eZ_{eff}^* \ \rho \ j)^2 \ BD_{eff}} \right) < \frac{L^2}{4} \frac{k_B T}{D_{eff} \ B \ \Omega}$$
(31)

i.e., 
$$jL > \frac{\sqrt{\pi}}{2}(jL)_{crit}$$
 (32)

where  $(jL)_{crit}$  is the conventional critical jL value from the Blech criterion, given by Equation (19). Note that in the first inequality, both the left and right hand sides are statistical quantities. However, both depend on  $D_{eff}$ , which cancels out, resulting in a deterministic criterion.

**Case III:** Let the earliest reasonable void nucleation time of a wire, taken to be the  $\mu - 3\sigma$  point of the underlying Gaussian of the nucleation time,  $t_n$ , be denoted as  $t_n^{\mu-3\sigma}$ . A wire is effectively EM-immortal if this earliest nucleation time is beyond the projected lifetime,  $t_{life}$ , of the circuit. In other words, it is EM-mortal if

$$t_n^{\mu-3\sigma} < t_{life} \tag{33}$$

Using (22), this inequality can be written as

$$t_n^{\mu-3\sigma} = e^{\mu_{t_n}-3\sigma_{t_n}} = e^{\log K_{t_n}-\mu_D} e_{f,n}^{-3\sigma_D} e_{f,n}^{-3\sigma_D} < t_{life}$$
  
i.e.,  $K_{t_n} < t_{life} e^{\mu_D} e_{f,n}^{+3\sigma_D} e_{f,n}$  (34)

Substituting  $K_{t_n}$  from Equation (12) and rearranging a few terms, this translates to the following mortality criterion for a wire carrying current j:

$$j > \frac{\sigma_c}{eZ_{eff}^{\star} \rho} \sqrt{\frac{\pi \ \Omega \ k_B T}{4 \ B \ t_o \ e^{\mu_D} eff, n^{+3\sigma_D} eff, n}}$$
(35)

For a wire to be EM-mortal, the criteria under all three cases must be satisfied. Since  $\sqrt{\pi}/2 \approx 0.89 < 1$ , the criterion for Case I is automatically satisfied by Case II. *Therefore, the EM-mortality criterion is given by* (32) and (35). Further, for both inequalities (32) and (35), all parameters on the right-hand side of the inequality are fundamental parameters of the technology; in particular, from (21), the statistics of  $D_{eff.n}$  can be seen to be based on the underlying process, and can be cheaply precomputed for a technology, without the need for any Monte Carlo simulations. We apply the mortality criteria, (32) and (35) to filter out wires that are safe with respect to EM, during the product lifetime. For the mortal wires, we perform Monte Carlo circuit simulations to analyze the impact on the power grid.

#### IV. MONTE CARLO SIMULATION FRAMEWORK

We use our probabilistic resistance model to perform Monte Carlo analysis of power grids in the presence of probabilistic resistance variations. Our probability distribution function (PDF) for the resistance change, derived in Section III-C builds a simple circuit-level abstraction for complex physical phenomena, facilitating simplified analysis at the circuit level by considering  $\Delta R$  as a random variable. However, given that EM is (and should be) a relatively unlikely event, it is essential for our Monte Carlo analysis to be biased appropriately: a truly random set of samples would probably see no resistance change in most (and possibly, for a small set of samples, no) wires. Most importantly, such an approach would see a large number of samples go to waste as they provide little meaningful information.

To overcome this, we use the notion of importance sampling (IS), which biases the distribution, but "unbiases" it as it interprets the results of sampling. Importance sampling is a Monte Carlo method that computes the expected value of a function f(x) of a random variable x, which is defined over a set of values  $\chi$ , and specified in terms of a distribution p(x). This method is particularly useful when p(x) is skewed or unevenly distributed, i.e., some values of x have a low probability of occurrence and are not sampled frequently enough, causing sampling errors. Importance sampling resolves this by sampling according to a function q(x) that is uniformly distributed over the range of x, and then correcting the error due to sampling from this different distribution by adding appropriate weights to f(x). For example, the expectation of f(x) under the distribution p(x), denoted  $E_p[f(x)]$ , is computed as:

$$\begin{split} E_p[f(x)] &= \int_{\chi} f(x)p(x)dx = \int_{\chi} f(x)p(x).q(x)/q(x)dx \\ &= \int_{\chi} w(x)q(x)dx = E_q[w(x)] \end{split}$$

where w(x) = f(x)p(x)/q(x) and  $E_p[f(x)]$  is the expectation of f(x) under the new distribution q(x). The pseudocode for our framework is shown in Algorithm 1

Algorithm 1 Power grid Monte Carlo simulation

- 1: Solve power grid to obtain nominal j for each wire
- 2: Calculate effective current density (Section III-D)
- 3: Filter immortal wires that are EM-safe (Section III-E)
- 4: for each mortal wire do
- 5: Use the resistance evolution model to obtain lognormal PDFs of wire resistance (Section III-C)
- 6: end for
- 7: for each Monte Carlo iteration do
- 8: **for** each mortal wire **do**
- 9: Sample the wire resistance using IS (Section IV)
- 10: end for
- 11: Build a circuit sample for the power grid using the above set of wire resistances
- 12: Solve the sample power grid and tabulate the IR drop13: end for
- 14: Report statistics (mean, standard deviation)

In this work, we use a sampling distribution q(x), which is a uniform distribution that stretches from 0 to the tail of the lognormal distribution of  $\Delta R$ : the values of this lognormal range from  $\Delta R = 0$  to the  $(\mu + 3\sigma)$  point of the underlying Gaussian,  $\log(\Delta R)$ , where  $\mu$  and  $\sigma$  represent, respectively, the mean and the standard deviation of the underlying Gaussian. If K is the span of this distribution from  $\Delta R = 0$  to the  $(\mu + 3\sigma)$  point of the underlying Gaussian, then every point within the span has a uniform probability of 1/K under q(x). The method samples points on this distribution, feeds them into a power grid simulator based on DC modified nodal analysis, and determines the voltage distribution at each node. The voltages are then translated back to the original distribution by scaling them to the original lognormal using the w(x) factor.

# V. RESULTS

# A. Failures in a single wire

To calibrate the correctness of our probabilistic model, we first work under assumptions similar to [4], which computes  $t_n$ , the time elapsed before a void nucleates in a wire, and  $t_g$ , the time elapsed from nucleation up to the instant at which length of the void,  $L_{void}$  becomes equal to  $L_{via}$ , i.e., allowing the void to grow until it spans across the length of the via. Our predicted values are then compared against the published Finite Element Analysis (FEA) simulations in [4]. For evaluating the corresponding values of time elapsed for void nucleation and growth, we use the probabilistic framework derived in Section III under accelerated aging conditions for temperature and current stress.

1) Calibration of correctness under accelerated aging: The material parameters for accelerated aging are set to ensure a fair comparison, drawing parameter values from [4] where available. Table I list the EM parameters along with their description, values, and the corresponding reference from where the values are imported. Some parameters that were unavailable were extracted from the literature. Specifically, B = 1GPa was used from [38].

The standard deviation for the normally distributed  $E_a$  is obtained from [28], by using the  $3\sigma$  value in  $E_a$ , which is specified as 0.11eV. Here  $\sigma$  denotes the standard deviation for  $E_a$ , and is obtained as 0.037eV. For our calibration simulations, we used the value for effective diffusivity and activation energy corresponding to the capping surface diffusion to align with the simulation setup in [4], which uses bamboo-like grains where the capping surface diffusion is the dominant EM mechanism, as discussed briefly in Section II-A.

-			
Name	Description	Value	
Ω	Atomic volume	$1.18 \times 10^{-29} \text{m}^3$ [2]	
j	Current density	$1.33 \times 10^{10}$ A/m <sup>2</sup> [4]	
ρ	Cu resistivity	$2.5 \times 10^{-8} \Omega m$ [4]	
T	Accelerated aging temperature	295°C [4]	
B	Effective bulk modulus	1GPa [38]	
$\sigma_c$	Critical stress for void nucleation	41MPa [5]	
$Z_{e\!f\!f}^{\star}$	Atomic charge number	5 [28]	
$D_0$	Diffusivity constant	$6.7 \times 10^{-13} \text{m}^2/\text{s}$ [28]	
$E_a$	Effective surface activation energy	0.45±0.11eV [28]	

Table I: EM parameters used for the single wire case.

Table II lists the expected value,  $\mu$ , of the lognormal and standard deviation,  $\sigma$ , for the underlying Gaussian of the lognormal for the failure parameters,  $t_n$  and  $t_g$ , obtained by our model, against the corresponding values obtained from FEA, mentioned in [4]. The values show a good level of consistency, despite some differences in the underlying assumptions. The discrepancies are attributed to factors such as the unavailability of some parameters in [4], and differences in the setup between the fully three-dimensional numerical simulations in the FEA approach against our analytical approach. Clearly, our method is much faster than the FEA approach since it merely involves the evaluation of an analytical expression. The three-dimensional models used by the numerical simulations in the FEA approach give an accurate estimate of the EM dynamics. However, due to the large simulation runtime, even for a single wire, the usage of such models for the statistical analysis of a multimillion-wire power grid system is unrealistic. Our work presents an approach that enables this level of scalability.

	Nucleation		Growth		
$\mu,\sigma$	$\mu_{t_n}$	$\sigma_{t_n}$	$\mu_{t_g}$	$\sigma_{t_g}$	
From [4]	8.5h	0.4h	8.0h	0.7h	
Analytical	7.2h	0.7h	8.4h	0.8h	

**Table II:** Void nucleation time  $(t_n)$  and growth time  $(t_g)$  comparison: Analytical method vs. [4].

Under the assumptions in [4], failure is defined as the time when  $L_{void} = L_{via}$ , and the time-to-failure (TTF) is the sum of the nucleation time,  $t_n$ , and the growth time,  $t_g$ . We apply the Wilkinson approximation [34] to obtain TTF as the sum of lognormal distributions of  $t_n$  and  $t_g$ . The TTF values for the 0.3% ile, 50% ile, and 99.7% ile points under accelerated aging are 12.7h, 15.6h, and 19.1h, respectively. These numbers indicate that every wire has a nonzero probability of failure, regardless of the value of its jL product that is traditionally used to screen out wires that are immortal under the Blech criterion. Indeed, wires that satisfy the Blech criterion will fail, as observed experimentally in [5], [10]. However, below a lifetime of 12.7h, there is very low probability that a specific wire will fail in any manufactured part, and wires that fall below this threshold can effectively be considered immortal.

2) Single-wire simulation at chip operating conditions: Now that we have compared our statistics with published work under accelerated aging conditions, we revert to performing our remaining evaluations under normal operating conditions. We use a similar setup as described in Section V-A1, but we perform this analysis at room temperature, using a current density value of  $1 \times 10^{10}$  A/m<sup>2</sup>. As expected, the reduction in temperature reduces the rate of EM degradation, and the TTF is now of the order of several years, as against accelerated aging, where it is of the order of several hours. We also perform MC simulations at these conditions to validate our approach using  $10^6$  samples on a normal distribution of activation energy.

We evaluate the resistance change ratio,  $\Delta R/R$ , of a wire according to our probabilistic formulation in (28), for the observation time,  $t_o = 12$  years. Figure 4 shows the comparison for the PDF of  $\Delta R/R$  as predicted by our formulation against a plot for the same PDF obtained from MC simulations. This figure demonstrates a close match between our analytical approximation with MC simulation



Figure 4: PDF of  $\Delta R/R$  for a wire under normal operating conditions.

#### B. Power grid simulation

Moving beyond a single wire, we now focus on analyzing the impact of EM on a set of power grid benchmark circuits described in [39]. Table III lists the power grid benchmarks that were evaluated for our EM analysis. For each power grid, the table lists the name, total number of wires, number of metal layers occupied, and the percentage nominal IR drop of the power grid, defined as the IR drop value of the node with the largest value of IR drop among all the nodes expressed as a percentage of supply voltage, evaluated at time 0, i.e., prior to EM degradation.

Name	Total	# Metal	% Nominal
	# wires	layers	IR drop
PG1	30027	2	8.2
PG2	208325	5	13.4
PG3	1401572	5	10.1
PG4	1560645	5	0.2
PG5	1076848	6	2.3
PG6	1649002	3	6.3
new1	2352355	6	12.2
new2	1422830	6	12.2

Table III: Power grid benchmarks evaluated in this paper.

For power grids PG1 and PG2, it was observed that the nominal IR drop for the original benchmarks, as described in [39], was abnormally high (>20% of the supply voltage). Similar to [9], we scale the original values of the current loads for these benchmarks such that the worst-case IR drop at nominal conditions is below 15% of the supply voltage.

For these benchmarks, we analyze the interconnects for EM risk in the power grid and simulate the distribution of the IR drop by solving the power grid to obtain the node voltage at every node for a given circuit lifetime,  $t_{life}$ . We assume constant current sources drawing current from the power grid, which consists of only resistive elements.

For the accelerated aging simulations described in Section V-A1, the capping surface diffusion was considered as the primary EM diffusion mechanism to align with the FEA simulations from [4]. However, for power grid simulations, we choose the EM process parameters corresponding to the grain boundary (GB) diffusion mechanism, since EM diffusion through the grain boundaries is indicated as the primary EM diffusion mechanism for advanced technology Cu DD interconnects, as indicated in [18], and briefly discussed in Section II-A. Table IV lists the values of the process parameters used in our simulations. We remind the reader again that for the lognormals, we provide mean and variance values that refer to the underlying Gaussians. Therefore, a negative mean value for the Gaussian is permissible since it translates to a positive mean for the lognormal.

Name	Description	Value
T	Chip operating temperature	105°C [40]
В	Effective bulk modulus	28GPa [12]
$\sigma_c$	Critical stress for void nucleation	41 <b>MP</b> a [5]
$Z_{e\!f\!f}^{\star}$	Atomic charge number $(GB)$	1 [12]
$D_0$	Diffusivity constant $(GB)$	$1.3 \times 10^{-9} \text{m}^2/s$ [12]
$\delta_{GB}$	Effective GB width	0.5nm [41]
$\mu_d$	Mean of underlying Gaussian of $d$	-16.2m [27]
$\sigma_d$	Standard deviation	0.38m [27]
	of underlying Gaussian of $d$	
$E_a$	Effective GB activation energy	0.8±0.11eV [12], [28]

Table IV: EM parameters used in power grid simulation.

We perform MC circuit simulation using samples from the EM-induced resistance increase,  $\Delta R$ , for every wire in the power grid using a statistical importance sampling approach, described in Section IV. We realize our implementation using C++ and MATLAB. For a confidence of  $P_{\text{target}}$  that the worst-case IR drop predicted from our MC simulation does not cross the 99.7% ile value predicted by our method, it can be shown that the number of simulations,  $N_{MC}$ , can be evaluated as  $N_{MC} = \frac{\log(1-P_{\text{target}})}{\log(0.997)}$ . We choose  $P_{\text{target}} = 95\%$ , which provides  $N_{MC} = 997$ , and for convenience, we round this upwards to 1000 simulations.

In our implementation, for convenience, we have used the matrix solver from MATLAB. However, to demonstrate that it is realistic to run a Monte Carlo simulation with 1000 simulations on these power grids, we use the runtime per iteration from [42], listed in Table V, to estimate realistic runtimes if a specialized power grid simulator were to be used instead. This table indicates that the MC-based evaluation is computationally reasonable.

	Single iteration	Peak Memory	Expected runtime for
	runtime [42]	in MB [42]	1000 MC simulations
PG1	0.2s	4	4min
PG2	1.4s	72	24min
PG3	8.3s	172	139min
PG4	19.4s	606	325min
PG5	9.4s	296	156min
PG6	15.4s	406	257min
new1	14.6s	349	243min
new2	16.4s	495	273min

**Table V:** Expected runtime values for MC power grid evaluation based on single iteration runtimes from [42].

# C. Mortal wire prediction

We now evaluate our new mortality criterion from Section III-E. We identify the number of mortal wires predicted from our proposed mortality criterion with those from the traditional deterministic Blech criterion, and list the



Figure 5: Mortal wire comparison: Our criterion vs. traditional Blech criterion.

number of such wires for each benchmark in Figure 5. It can be seen that our implementation indicates that a larger number of wires must be considered mortal under our probabilistic formulation. As derived in Section III-E, the mortal wires identified by our approach is a superset of those that are mortal under the traditional criterion, and therefore the number of mortal wires is larger than the traditional number.

#### D. EM-induced IR drop degradation

Next, for the power grid benchmarks, we discuss the statistics of performance degradation from part to part. This variation is a result of EM-induced increases in wire resistances due to probabilistic variations in  $E_a$  and d, which leads to statistical shifts in the IR drop, and is computed through an MC simulation on each power grid.

For each MC sample, we tabulate the IR drop value of power grid, defined previously as the IR drop value of the node which has the largest IR drop, since it is this node which will decide the overall performance of the circuit. Based on this distribution of IR drop values, we define the maximum IR drop value,  $V_{\text{max}}$ , as the 99.7%ile point of this distribution, and the spread,  $\Delta V$ , in the IR drop values, as the difference between the 99.7%ile and 0.3%ile values. The maximum IR drop is normalized as a percentage of the supply voltage,  $V_{dd}$ , and the spread as a function of the maximum IR drop.

1) Impact of  $E_a$  and d on IR drop: In order to quantify the impact on IR drop due to variations in activation energy,  $E_a$ , and grain size, d, we perform three sets of circuit simulations, for a specific lifetime  $t_{life} = 10$  years. In the first set, we do not consider any variation in both activation energy,  $E_a$ , and grain size, d, and we choose fixed values for  $E_a$  and d, which correspond to the mean values of their corresponding distributions. For the second set of simulations, we consider variations in the activation energy and a constant grain size, and in the third set, we assume variation in both  $E_a$  and d. Table VI shows the normalized maximum IR drop value and the normalized spread, as defined previously, for every benchmark for each of the three sets of simulations.

For the first set, clearly, the spread is zero since no variation is assumed. For the second and third set, the normalized maximum IR drop increases and there is a clear spread in the IR drop. The spread due to variation in both  $E_a$  and *d* variation, in the third simulation set, is observed to be marginally more than the spread due to variation in only  $E_a$ ,

	No	$E_a$		$E_{a,d}$	
	variation	variation		varia	ation
	$\frac{V_{\text{max}}}{V_{dd}}$	$\frac{V_{\text{max}}}{V_{dd}}$	$\frac{\Delta V}{V_{\text{max}}}$	$\frac{V_{\text{max}}}{V_{dd}}$	$\frac{\Delta V}{V_{\text{max}}}$
PG1	9.1%	10.5%	18.1%	11.1%	22.3%
PG2	15.8%	17.3%	5.9%	17.8%	9.3%
PG3	12.3%	12.8%	0.2%	13.9%	0.3%
PG4	0.7%	0.9%	2.2%	1.1%	3.2%
PG5	3.1%	3.4%	20.2%	3.7%	24.7%
PG6	8.9%	10.8%	9.1%	11.5%	6.4%
new1	12.7%	12.8%	0.3%	12.9%	0.4%
new2	12.4%	12.5%	0.2%	12.7%	0.3%

**Table VI:** The impact of  $E_a$  and d variation on the normalized 99.7% ile value and normalized spread of IR drop.

in the second set. This indicates that the variation in  $E_a$  has a relatively larger impact on the overall variation in IR drop. This can be attributed to the actual values chosen for mean and standard deviation of the process parameters which have been extracted from literature. Besides showing the relative contributions of process parameter variations on the IR drop of power grids, we also want to emphasize the fact that, under statistical variation of process parameters, the IR drop is not a fixed value but follows a distribution.

2) Impact of temperature variation due to Joule heating: In order to quantify the impact of temperature rise due to Joule heating we repeat the third set in the previous circuit simulation, but this time we artificially force temperature rise due to Joule heating,  $\Delta T_J$ , in (15) to zero in our simulation.

Figure 6 shows the normalized maximum IR drop for the eight benchmarks, and demonstrates that the maximum IR drop values for each benchmark is lower when Joule heating is not incorporated. The percentage error in the IR drop, relative to its correct value after considering  $\Delta T_J$ , varies from 6% (for PG2) to 40% (for PG4). These variations across benchmarks can be attributed to multiple factors that vary between the power grids, such as the RMS current and the ILD thickness, which depends on the metal layers used.



Figure 6: Effect of Joule heating on IR drop.

3) Impact of current redistribution: The flow of current in the power grid drives EM, which induces probabilistic wire resistance changes. These changes, in turn, affect the distribution of current through the wires, thereby impacting further EM-induced degradation. In order to capture the evolution of IR drop, our MC circuit simulation are performed using an iterative approach where the wire resistance and the current density value are updated after incremental steps leading to the circuit lifetime. For the power grid benchmarks, when we compare this iterative approach with a noniterative method, where the currents are not updated after t = 0, we observe that the noniterative approach predicts a larger IR drop compared to the iterative approach for all benchmarks. Figure 7 illustrates the normalized maximum IR drop for a representative benchmark, PG1, as a function of time. The



Figure 7: IR drop evolution of PG1 (iterative vs. noniterative).

lower IR drop values in the iterative approach can be attributed to the current redistribution in the redundant paths of the power grid. This results in lower current flow through the EM-affected wires, thereby attenuating further EM-induced resistance degradation. In contrast, for the noniterative case, the current stress for the EM-affected wires remains constant predicting a relatively larger damage than is really seen. For PG1 the error in the IR drop at circuit lifetime,  $t_{life} = 10$  years, is observed to be 9% of the IR drop value at that instant.

4) Statistics of the worst-case IR drop for the power grid: In order to study the time evolution of variation of the IR drop, we observe the CDF of the IR drop corresponding to the node with the largest value, according to our definition of  $V_{\text{max}}$ , for power grid PG1. The data is generated for various values of the lifetime,  $t_{life}$ , using our iterative MC approach. Figure 8 shows the CDF of the IR drop at  $t_{life} = 5$ , 10, and 20 years, corresponding to the typical product lifetime values for mobile, computing, and automotive applications, respectively.



Figure 8: CDF plots for IR drop of PG1 for different circuit lifetimes,  $t_{life}$ .

For a given threshold value, e.g., 10% as indicated by a vertical line on the x-axis, the CDF corresponding to  $t_{life} = 5$  years lies completely to the left of this threshold. This implies that for short lifetime applications (e.g., mobile), the power grid will remain functional since the IR drop is below the threshold for all the samples. In contrast, the worst percentage

resistance degradation in PG1 at  $t_{life} = 5$  years is 48%, which is above the typical 10–20% resistance increase criterion that is typically used by designers today. This demonstrates that the circuit lifetime, which corresponds to the time during which the IR drop is satisfactory, can be longer than the lifetime of any of its component wires. In other words, the power grid is robust to some EM failures in individual wires.

The probability that the IR drop is larger than 10% increases with lifetime since a larger fraction of the samples crosses the chosen threshold for larger values of  $t_{life}$ . For the CDF corresponding to  $t_{life} = 10$  years, 9% of the samples cross the threshold, resulting in functional failure, and this value increases to a value of 33% for  $t_{life} = 20$  years as more voids nucleate and grow over this longer period, thereby resulting in larger EM-induced IR drop degradation. Thus, for long lifetime applications, a significant fraction of samples will be EM-affected if the IR drop threshold is chosen as 10%. On the other hand, if the design specifications are changed so that the IR drop threshold criterion is relaxed from 10% to 12%, there is a 98% likelihood that the power grid will remain functional up to 20 years for the modified threshold. We also observe the worst resistance increase corresponding to  $t_{life} = 10$  years and  $t_{life} = 20$  years to be 124% and 287% respectively. Thus, even though the EM-induced wire resistance change increases by  $2.3 \times$  between  $t_{life} = 10$  years to  $t_{life} = 20$  years, the IR drop threshold changes by only 2% in order to maintain a significantly large (98%) probability for correct circuit functioning. This reemphasizes the resiliency of the power grid to EM-induced wire resistance change.

Note that for a well-designed power grid the fraction of samples crossing the IR drop threshold, thereby resulting in functional failure, should be a low value. Depending on the product lifetime this value can be of the order 1000ppm to 1ppm depending on the product lifetime [43]. However, the failure fraction is significantly larger than 1000ppm. This is due to the fact the power grid benchmarks are not completely optimized. Nevertheless, the designer may encounter them during design iterations, and it is important to analyze them to inform the designer that the grid has EM problems. The designer can then reduce the failure rate, for example, by adjusting the current densities through wire width tuning, and such optimization would be informed by the analysis of the type proposed here.

#### VI. CONCLUSION

We have developed a method for EM analysis of power grids taking into account two effects that were neglected in past work: first, that EM is a probabilistic phenomenon for Cu DD interconnects, and second, that the power grid has inherent resilience to EM failures. Our results indicate that both effects are substantial. Further, we perform an analysis that determines an improved immortality criterion that accounts for steady-state behavior. In addition to microstructural variations, the variation in EM process parameters, such as critical stress can also influence the performance. Our methodology can provide a framework to address these additional variations, and this constitutes a part of our future work.

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