

# Analysis and Optimization of Structured Power/Ground Networks

Haihua Su	Kaushik H. Gala
IBM Austin Research Lab	Motorola Inc.
11501 Burnet Rd.	7700 W Parmer Ln.
Austin, TX 78758	Austin, TX 78729
haihua@us.ibm.com	kgala@adttx.sps.mot.com

Sachin S. Sapatnekar  
 Department of Electrical and Computer Engineering  
 University of Minnesota, 200 Union St. SE  
 Minneapolis, MN 55455  
 sachin@ece.umn.edu

## Abstract

This paper presents an efficient method for optimizing power/ground (P/G) networks by widening wires and adding decoupling capacitors (decaps). It proposes a structured skeleton that is intermediate to the conventional method that uses full meshes, which are hard to analyze efficiently, and tree-structured networks, which provide poor performance. As an example, we consider a P/G network structure modeled as an overlying mesh with underlying trees originating from the mesh, which eases the task of analysis with acceptable performance sacrifices. A fast and efficient event-driven P/G network simulator is proposed, which hierarchically simulates the P/G network with an adaptation of PRIMA to handle non-zero initial conditions. An adjoint network that incorporates the variable topology of the original P/G network, as elements switch in and out of the network, is constructed to calculate the transient adjoint sensitivity over multiple intervals. The gradients of the most critical node with respect to each wire width and decap are used by a sensitivity-

based heuristic optimizer that minimizes a weighted sum of the wire and the decap area. Experimental results show that this procedure can be used to efficiently optimize large networks.

## I. INTRODUCTION

The design of power/ground (P/G) networks is critical to the correct functioning of a chip. With the rapid increases in the clock frequency and reductions in the feature sizes of high-speed electronic circuits, it is becoming more and more important to design and optimize P/G networks fast and efficiently. The major effects that influence the circuit functionality are the voltage drop due to current flow in the network, ground bounce due to inductive effects, and possible electromigration effects due to excessive current densities. The first two can lead to unacceptable circuit switching speeds and/or glitches, while the latter places a limit on the useful lifetime of a chip [5].

Various algorithms and simplified device models for P/G networks that offer faster but less accurate results have been explored in the past. Early work on P/G networks focuses on tree-like structures so as to allow the use of path tracing algorithms for efficiency [6,24] and assumes resistance-only models for the network. A 3-stage IR-drop analysis methodology during the whole design process is presented in [9]. The authors of [27] propose a hierarchical analysis technique and a novel sparsification method based on 0-1 integer linear programming. A PDE-like multigrid method is proposed in [16] to perform both DC and transient simulation of power grids efficiently. Each of the above methodologies aims at speeding up the analysis and predicting the power grid performance properly.

Other related work on optimizing P/G networks includes [22,23,25], which use techniques ranging from simulated annealing to the solution of a sequence of linear programs for wire widening, or [15], which optimizes the topology of the P/G network. A frequency domain

sensitivity-based decoupling capacitor optimization method is proposed in [1]. The work in [3] formulates the P/G network optimization problem as a nonlinear convex optimization problem.

Most of the existing techniques have focused on methods that optimize a specific topology that is typically specified by the user to be a large and complex mesh. There is an inherent conflict between P/G networks that are easy to analyze, and those that provide reliable power levels and evenly distributed current densities. While tree structures provide all of the former benefits, they result in poor quality in P/G signal delivery. On the other hand, dense meshes are excellent in satisfying the latter requirement but are very computationally difficult to analyze. For example, the work in [5] shows that it requires several hours to analyze a P/G network using SPICE. The key idea used in this work is that an approach that meets both of these requirements would be something between a pure tree and a full mesh. In this work, we use one such topology skeleton with a global mesh feeding local trees, as described later in this section; a similar method has been used in [21]. However, we emphasize that this approach can be modified to other topologies that are intermediate to the two extremes of full trees and full meshes: one such example is a global mesh that feeds smaller unconnected local meshes.

We point out that such an approach may not be optimal for a high-performance full-custom microprocessor, where a dense mesh may be essential for reliable P/G levels<sup>1</sup>. However, we believe that it will be of great utility in ASIC design, where fast turnaround time of the design is a major criterion, and ease of analysis of the P/G network with an acceptable performance hit can greatly ease the task of P/G network optimization. For this scenario, we present an analysis/sensitivity calculation/optimization procedure in this paper.

The P/G network model used here, characterized by the mesh/tree topology of [21],

<sup>1</sup> Even for processor designs, the use of more general hierarchical structures is not uncommon [27].

is illustrated in Fig. 1; for simplicity, only one tree is shown in the figure. An overlying coarse mesh structure of a user-specified topology provides global distribution of the P/G signals across the chip. From various nodes of this mesh, tree structures of user-specified topologies originate and distribute the supply voltage to the utilization points, each of which is modeled as an equivalent RC element, as is shown in Fig. 1. The advantage of using an RC element instead of an equivalent current source (as is used in most P/G network analysis work, e.g., [9], [16] and [27]) is that such a model also captures the loading effects of the utilization points on the P/G network.

Practically, the designer can estimate a list of candidate nodes that are potential worst-case voltage drop nodes. They often correspond to a sampling of the nodes close to the most active macros or regions. Therefore, we assume that the list of critical nodes is user-specified. A set of worst-case switching patterns can also be obtained [2, 7, 14], and are assumed to be provided as inputs to our approach. Each specified switching event in a switching pattern at a utilization point provides information on which RC elements at that utilization point load the network at a given time. A schematic of an example switching pattern at a utilization point is shown in Fig. 2, where each arrow indicates that at that time, a set of RC elements has entered or left the network due to switching events at gates. We assume, at the beginning of each switching event, that the initial voltage across the capacitor in an RC element is at the supply voltage level,  $V_{dd}$ , if this element is to be switched into the ground network. Therefore, the RC elements with non-zero initial conditions<sup>2</sup> are the only sources that inject currents into the ground network. Similarly, for supply networks, the initial voltages on the capacitances associated with the switching RC elements are assumed to be zero, and they are the only sources that draw currents from the supply network.

An efficient noise metric for the performance of every node in a power/ground network

<sup>2</sup> Non-zero initial conditions can be modeled using independent sources as in [21].

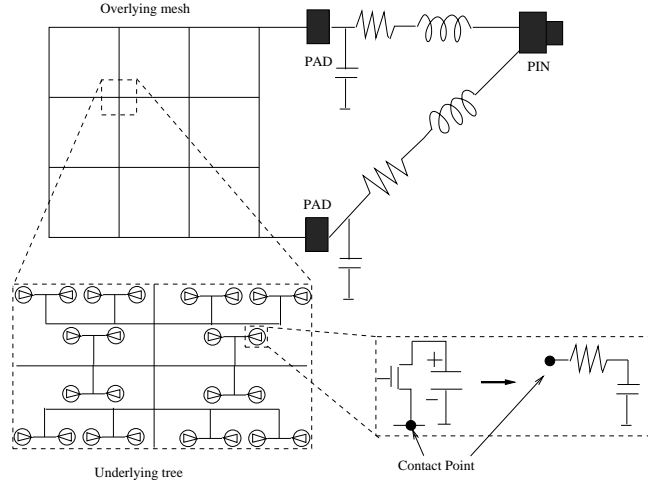


Fig. 1. A structured P/G bus topology.

is the integral of voltage drop beyond the noise margin, which is represented by the shaded area in Fig. 3. The voltage drop integral is always greater or equal to zero. This idea was first introduced in [8] and it proves to be an efficient measure for circuit optimization.

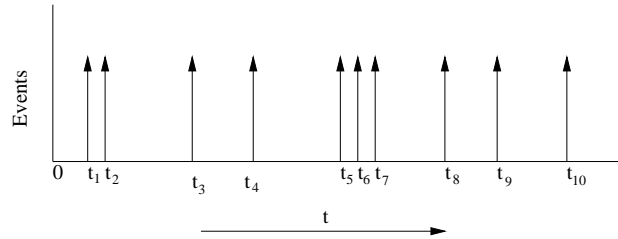


Fig. 2. Switching events at a node in a P/G network.

According to this noise metric and our assumption on the given list of critical nodes, the most critical node in the P/G network becomes the one with the worst-case voltage drop integral among all the given critical nodes. Then our optimization problem is to minimize the total P/G bus area, subject to the constraints that the voltage drop integral of the most critical node is zero, and subject to the technology-dependent constraints on minimum/maximum wire widths. The process of optimizing the P/G network requires an iterative loop within which it is necessary to analyze the network to determine whether it satisfies the constraints

or not, and to determine gradient information to guide the optimization.

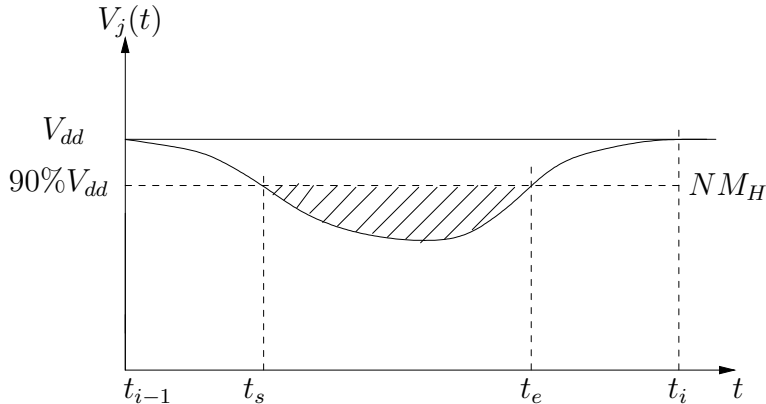


Fig. 3. Voltage drop of node  $j$  in a power network during Event  $i-1$  and  $i$ .

Several techniques may be used for this optimization: varying the topology, varying wire widths, and adding decoupling capacitors. In this work, we focus on optimization by varying wire widths and extend this technique to add decoupling capacitors.

The structure in Fig. 1 is amenable to fast analysis, while also maintaining the performance by using mesh structures that reduce the voltage drops and current densities in the highest current regions. In [21], an AWE-based technique is proposed for simulating P/G networks. While AWE tends to be unstable at higher orders of approximation, for such a structure, the task of analysis is rapidly performed using PRIMA [17], a reduced order modeling technique that produces provably passive macromodels.

Other P/G network analysis work using PRIMA-based model order reduction technique include [4] and [26]. Both approaches use a large number of piece-wise linear (PWL) current sources to model the loads, which brings non-constant terms in the frequency domain and is inefficient for multi-port model reduction. To overcome this inefficiency, the extended Krylov subspace (EKS) method and an improved EKS method for calculating PWL current source moments are proposed in [26] and [4], respectively. In our work, we use an RC element with non-zero initial conditions across the capacitor instead of a current source to model the loads.

This has the advantage of providing convenient PRIMA-based analysis using the standard Krylov subspace method, where all the inputs to the system are constant in the frequency domain (as will be described in Section II). Moreover, the current drawn by a load is not truly independent of the supply voltage, as assumed in [4, 26], and our RC element model reflects this and captures the dependency.

Transient sensitivity has been particularly useful in circuit optimization and tuning and has been used to provide gradient information [8, 10, 11]. In the case of P/G network optimization, the optimization of the objective function requires the computation of transient sensitivity of the most critical node with respect to all the elements in the whole network, and we employ the adjoint method [18].

Traditionally, transient sensitivity computation for a circuit with a fixed topology is performed by a convolution between the forward-in-time voltage/current slope of the element (capacitor, resistor or inductor) in the original circuit and the backward-in-time voltage/current across the same element in the adjoint circuit, where the same fixed topology is used for the pair of original and adjoint circuits.

In our work, the topology of the original P/G network changes at the beginning of each switching event as new RC elements are added to the network or removed from it. This paper presents an appropriate extension of the adjoint network technique over multiple-intervals for the variant topology so that the sensitivities can be efficiently computed. Our sensitivity computation is coupled with an efficient PRIMA-based order reduction approach so that it can handle large-scale P/G networks. A closed-form transient sensitivity expression is provided for a PRIMA approximation of a given order.

To the best of our knowledge, this is the first work to use time domain sensitivity for P/G network optimization. In addition, we have augmented time-domain sensitivity to handle

the case where the network topology undergoes changes as RC elements switch into or out of the network.

In the next section we discuss in detail the hierarchical P/G network simulator. We then describe in Section III the transient adjoint sensitivity technique with respect to R, L and C elements over multiple intervals and then present the closed-form formula. The detailed theoretical derivation can be found in the appendix. In Section IV we describe the heuristic optimization procedure. The simulation and optimization results are presented in Section V, followed by concluding remarks in Section VI.

The following notation will be used throughout the paper. The voltages [currents] in the original network are denoted by  $v$  [ $i$ ], while the voltages [currents] in the adjoint network are  $\psi$  [ $\varphi$ ]. The symbols  $t$  and  $\tau$  denote the temporal variables in the original and adjoint network, respectively.

## II. HIERARCHICAL ANALYSIS OF THE P/G NETWORK INCORPORATING NON-ZERO INITIAL CONDITIONS

It is well-known that the procedure for analysis of the power and ground network is symmetric, implying that it is enough to develop a solution for one of these problems. In this section, we will develop a hierarchical analysis method that can be applied for both the original and the adjoint network.

The interconnect in the P/G network is modeled as follows. Each wire on the mesh or tree structure is modeled as a set of connected segments under the  $\pi$ -model, with each segment modeled using lumped RLC parameters given by

$$\begin{aligned} R_s &= \rho l_s / w_s \\ C_s &= (\beta w_s + \alpha) l_s \\ L_s &= \gamma l_s / w_s \end{aligned} \tag{1}$$



where  $l_s$  and  $w_s$  are the length and the width of the segment, and the parameters  $\rho$ ,  $\beta$ ,  $\alpha$  and  $\gamma$  are the sheet resistance per square, capacitance per square, fringing capacitance per unit length and the inductance per square of the metal layer that is being used for routing the P/G network. Each package pin is modeled as an RLC branch connected to pads on the mesh. The pin parameters were found from IBM public-domain product documents. Although the wire inductive model is approximate, since it does not consider the mutual inductance and uses a simple model for the self-inductance, it reasonably captures the nature of wire inductance in current technologies where their magnitude is small and is dominated by pin inductances. In principle, the approach can be extended to handle more complex models.

The simulation is event-driven, proceeding one interval at a time, starting from the first interval until the last, updating the corresponding switch states specified in the event list while moving from one interval to the next. The final state (i.e., capacitor voltages and inductor currents) at the end of each interval constitutes the initial state for the next interval. At the beginning of the first event, initial conditions on all capacitors and inductors are given, i.e., those initial voltages on capacitor in the ground nets are zero and  $V_{dd}$  for those in supply nets, those across capacitors in the RC elements switching to ground nets are  $V_{dd}$  and zero for those switching to supply nets and all the inductors have zero initial currents.

The entire system may be modeled as a linear system characterized by the modified nodal analysis (MNA) equation

$$(\mathbf{G} + s\mathbf{C})\mathbf{V}(s) = \mathbf{J}(s) \quad (2)$$

where  $\mathbf{G}$  and  $\mathbf{C}$  represent the conductance and susceptance matrices. The vector  $\mathbf{V}(s)$  of the MNA variables is of dimension  $N \times 1$ , and includes the nodal voltages and the branch currents for voltage sources and inductors. The  $N$  variables correspond to various levels of the hierarchy that we will use later: the variables that relate to the mesh, the variables that

correspond to the connections between the mesh and the trees, and the variables related to the tree structures. The right hand side vector  $\mathbf{J}(s)$  contains all the sources in the system. Our fast analysis method reduces this system to a smaller system that captures the response of the system to the given set of switching events including sources that model the initial conditions in the system.

The hierarchical model reduction and simulation proceeds in three stages: first, each tree is reduced to an equivalent passive model. Next, the mesh is solved, along with these passive models to find all nodal voltages in the mesh, i.e., mesh voltages. Finally, these mesh voltages provide the voltage source at the root of each tree and are used to solve each tree individually and independently. This hierarchical approach serves to reduce the amount of computation required during the analysis.

#### A. Reduction of the trees

The MNA equation for each of the trees with initial conditions can be written as

$$\begin{aligned} (\mathbf{G}_{\mathbf{T}} + s\mathbf{C}_{\mathbf{T}})\mathbf{V}_{\mathbf{T}}(s) &= \mathbf{B}_{\mathbf{T}}\mathbf{u}_{port} \\ \mathbf{i}_{port} &= \mathbf{L}_{\mathbf{T}}^T\mathbf{V}_{\mathbf{T}}(s) + \mathbf{i}_{\mathbf{T}init} \end{aligned} \quad (3)$$

where  $\mathbf{G}_{\mathbf{T}}$  and  $\mathbf{C}_{\mathbf{T}}$  are the conductance and susceptance matrices for the tree.  $\mathbf{i}_{port}$  and  $\mathbf{u}_{port}$  are vectors denoting the port currents and voltages. The constant vector  $\mathbf{i}_{\mathbf{T}init}$  captures the initial conditions stored in capacitors or inductors in the tree. In our P/G network, there are at most three “ports” for a tree, which correspond to (a) the tree root (the node connected to one of the mesh nodes), (b) all non-zero initial conditions on capacitors in the RC elements and wire inductors, which are represented by independent sources and, (c) for the adjoint network only, the most critical node where the adjoint current source (see Section III for details) is applied. Therefore,  $\mathbf{B}_{\mathbf{T}} = [\mathbf{J}_1(s) \ \mathbf{J}_2(s) \ \mathbf{J}_3(s)]$ ,  $\mathbf{u}_{port} = [\mathbf{u}_{root} \ 1 \ \mathbf{u}_{critical}]^T$ ,  $\mathbf{i}_{port} = [\mathbf{i}_{root} \ \mathbf{i}_{critical}]^T$ ,  $\mathbf{i}_{\mathbf{T}init} = \mathbf{J}_2(s)$ , and  $\mathbf{B}_{\mathbf{T}}$  captures all the potential sources in the tree (these

are described in further detail later). Since the admittance matrix  $\mathbf{Y}(s)$  of a circuit (defined by  $\mathbf{i}_{port} = \mathbf{Y}(s)\mathbf{v}_{port}$ ) is assuming zero initial conditions (setting  $\mathbf{J}_2(s)$  as  $\mathbf{0}$ ), let  $\mathbf{B}\mathbf{1}_T = [\mathbf{J}_1(s) \mathbf{J}_3(s)]^T$ , then  $\mathbf{L}_T = \mathbf{B}\mathbf{1}_T$ , which guarantees no sources inside the system except for the two ports. The property of  $\mathbf{L}_T = \mathbf{B}\mathbf{1}_T$  is used in the proof of PRIMA to preserve the passivity of the system [17].

Each column in  $\mathbf{B}_T$  is described as follows.  $\mathbf{J}_1(s)$  is the input excitation to the tree, which has an entry of 1 for the root node since we are interested in the transfer function (impulse response) of the tree during the later waveform propagation step. An initial condition at time  $t_0$  on a capacitor  $C_i$ [inductor  $L_i$ ] may be modeled as a voltage [current] source of value  $V_{C_i}(t_0)$  [ $I_{L_i}(t_0)$ ] in series [parallel] with a capacitor [inductor] with zero initial conditions. The vector  $\mathbf{J}_2(s)$  captures these initial conditions of the tree and has entries of the type  $C_i V_{C_i}(t_0)$  and  $L_i I_{L_i}(t_0)$ , where the multiplications by  $C_i$  and  $L_i$  correspond to conversions between Thevenin and Norton forms for ease of application for the formulation, and  $V_{C_i}(t_0)$  and  $I_{L_i}(t_0)$  corresponds to the Laplace Transform of the nodal voltage and branch current with non-zero initial conditions. The vector  $\mathbf{J}_3(s)$  is only considered when an impulse current source (with a Laplace Transform of 1) or a current source of square wave is applied to the most critical node in the adjoint network. Detailed derivations on adjoint circuit analysis will be discussed in Section III. However, we point out here that the right hand side of Eqn. (3) contains constant entries only.

The PRIMA reduction procedure is applied to obtain a provably passive tree reduction. A RICE-like tree traversal [19] computes the orthonormal basis  $\mathbf{X}$  of the Krylov space, so that the procedure is extremely fast. The three-column right hand side matrix in Eqn. (3) tells us that three columns are added to  $\mathbf{X}$  in each iteration and to obtain a reduction of order  $q_T$ ,  $\lceil \frac{q_T}{3} \rceil$  iterations are required. As described in the introduction section, we will apply

the transient adjoint sensitivity technique [10, 11] to find out the voltage noise sensitivity with respect to all the RLC elements in the network. This technique requires the analysis of the circuit itself (original circuit) and an adjoint circuit, which is constructed according to the topology of the original circuit and the responses of nodes/branches of interest. While for the analysis of the original network (comparing to the adjoint network), the right hand side only includes two columns ( $[\mathbf{J}_1(s) \ \mathbf{J}_2(s)]$ ) and consequently the number of iterations is  $\lceil \frac{qt}{2} \rceil$ . Details of the PRIMA reduction procedure may be found in [17].

### B. Solving the mesh

Substituting the reduced order model of each tree can reduce the MNA equation (2) for the whole system to

$$(\mathbf{G}_M + s\mathbf{C}_M)\mathbf{V}_M(s) = \mathbf{J}_M(s), \quad (4)$$

where

$$\mathbf{G}_M = \begin{bmatrix} \mathbf{G} \text{ Stamps for} & 0 & 0 \\ \text{the mesh} & \mathbf{I}_{port} & 0 \\ 0 & 0 & \mathbf{I}_{port} & -\tilde{\mathbf{L}}_T^T \\ 0 & -\mathbf{B}\tilde{\mathbf{I}}_T & 0 & \tilde{\mathbf{G}}_T \end{bmatrix}, \quad (5)$$

$$\mathbf{C}_M = \begin{bmatrix} \mathbf{C} \text{ Stamps for} & 0 & 0 \\ \text{the mesh} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \tilde{\mathbf{C}}_T \end{bmatrix}, \quad (6)$$

and

$$\mathbf{J}_M = \begin{bmatrix} \mathbf{i}_{Minit} \\ 0 \\ \tilde{\mathbf{i}}_{Tinit} \end{bmatrix}. \quad (7)$$

where “**G Stamps for the mesh**” and “**C Stamps for the mesh**” are the MNA matrix stamps [18] for the conductances and capacitances in the mesh structure shown in Fig. 1.

$I_{port}$  is an  $N_T \times N_T$  identity matrix, where  $N_T$  is the total number of trees.

As compared the size of vector  $\mathbf{V}(s)$ , the size of vector  $\mathbf{V}_M(s)$  is reduced to the sum of total number of mesh nodes, number of non-zero mesh and package inductances, total number of trees and each reduced tree stamps. Generally speaking, the number of columns of  $\mathbf{J}_M(s)$  can be 2, which corresponds to non-zero initial conditions in the mesh and reduced non-zero initial conditions of each tree contributing to the mesh, and, for adjoint analysis only, the adjoint current source applied to the most critical node, if it is one of the mesh nodes. However, the most critical node is typically in the underlying trees, so  $\mathbf{J}_M(s)$  has only one column as shown in Eqn. (7). Similar to the right-hand-side vector of a tree,  $\mathbf{J}_M(s)$  contains constant entries only.

The size of Eqn. (4) is still large, so PRIMA is applied to Eqn. (4) again to this reduced system to further reduce the system to a smaller order:

$$(\tilde{\mathbf{G}}_M + s\tilde{\mathbf{C}}_M)\tilde{\mathbf{V}}_M = \tilde{\mathbf{J}}_M(s) \quad (8)$$

where  $\tilde{\mathbf{G}}_M$ ,  $\tilde{\mathbf{C}}_M$ ,  $\tilde{\mathbf{V}}_m$  and  $\tilde{\mathbf{J}}_M$  are the reduced matrices/vectors obtained from PRIMA.

Since  $\mathbf{G}_M$  is sparse, sparse matrix technique can be used to compute the orthonormal basis  $\mathbf{X}$  of the Krylov space, where the inverse of the matrix  $\tilde{\mathbf{G}}_M$  is required. Since the overlying mesh is typically small in terms of the number of nodes and the order of the final system is small, the computational cost of this is also reasonably small. As previously mentioned, a more detailed description of the PRIMA reduction procedure may be found in [17].

The transient response (in Laplace domain) of each mesh node in the P/G net is found to be:

$$V_{Mesh}(s) = \sum_{i=1}^{q_m} \frac{r_i}{s - \lambda_i} \quad (9)$$

where  $\lambda_i$  and  $r_i$  are the  $i$ th pole and residue of a mesh node.  $q_m$  is the number of dominant

poles for the mesh, which is determined by the reduced order of the mesh matrix. After taking an inverse Laplace transform, we have

$$V_{Mesh}(t) = \sum_{i=1}^{q_m} r_i e^{\lambda_i t}, \quad 0 \leq t \leq T_f, \quad (10)$$

where  $T_f$  is the period of time between two continuous events.

### C. Propagating Waveforms Down the Trees

The mesh node voltages are contained in the solution to Eqn. (8). These values are used to compute the voltage at each of the internal node in the local trees. The voltage at each tree node is computed as the sum of the zero input response and the zero initial condition response; note that the input for the tree is the voltage at the mesh node (root of the tree), which is typically non-zero.

The propagation formula of a tree node in Laplace domain is

$$V_{Tree}(s) = \sum_{j=1}^{q_T} \frac{r_{Tz_j}}{s - \lambda_{Tz_j}} + \sum_{i=1}^{q_m} \sum_{j=1}^{q_T} \frac{r_i}{s - \lambda_i} \times \frac{r_{Timp_j}}{s - \lambda_{Timp_j}}, \quad (11)$$

where  $\lambda_{Tz_j}$  and  $r_{Tz_j}$  are the  $j$ th pole and residue of the local tree's zero input response,  $\lambda_{Timp_j}$  and  $r_{Timp_j}$  are the  $j$ th pole and residue of its impulse response.  $q_T$  is the order of the approximant for each local tree. Eqn. (11) is obtained from classical linear circuit theory which states that the total response of any node in a circuit is equal to the sum of two component responses: its zero-input response and its zero-state response [13]. Zero-state response can be calculated from the transfer function (Laplace transform of the impulse response) of this node. This equation can further be derived into the following form using the partial fractional method:

$$V_{Tree}(s) = \sum_{i=1}^{Q_T} \frac{r_{T_i}}{s - \lambda_{T_i}} \quad (12)$$

where  $Q_T = q_m + q_T$  and the poles of the tree are

$$\lambda_T = \begin{cases} \lambda_i, & i = 1 \cdots q_m \\ \lambda_{Timp_j} = \lambda_{Tz_j}, & j = 1 \cdots q_T \end{cases} \quad (13)$$

and the corresponding residues are

$$r_T = \begin{cases} \sum_{j=1}^{q_T} \frac{r_i r_{Timp_j}}{\lambda_i - \lambda_{Timp_j}}, & i = 1 \cdots q_m \\ r_{Tz_j} + \sum_{i=1}^{q_m} \frac{r_{Timp_j} r_i}{\lambda_i - \lambda_{Timp_j}}, & j = 1 \cdots q_T \end{cases} \quad (14)$$

By taking inverse Laplace Transform we get:

$$V_{Tree}(t) = \sum_{i=1}^{Q_T} r_{T_k} e^{\lambda_{T_k} t}, \quad 0 \leq t \leq T_f \quad (15)$$

Currents flowing through mesh branches are solved from the MNA equation of the mesh, while every tree branch current flowing through node  $i$  and  $j$  is found through  $i(s) = (v_i(s) - v_j(s))/(R_{ij} + sL_{ij})$  and by taking an inverse Laplace transform of  $i(s)$  we can get  $i(t)$ .

#### D. A Simple RC Example

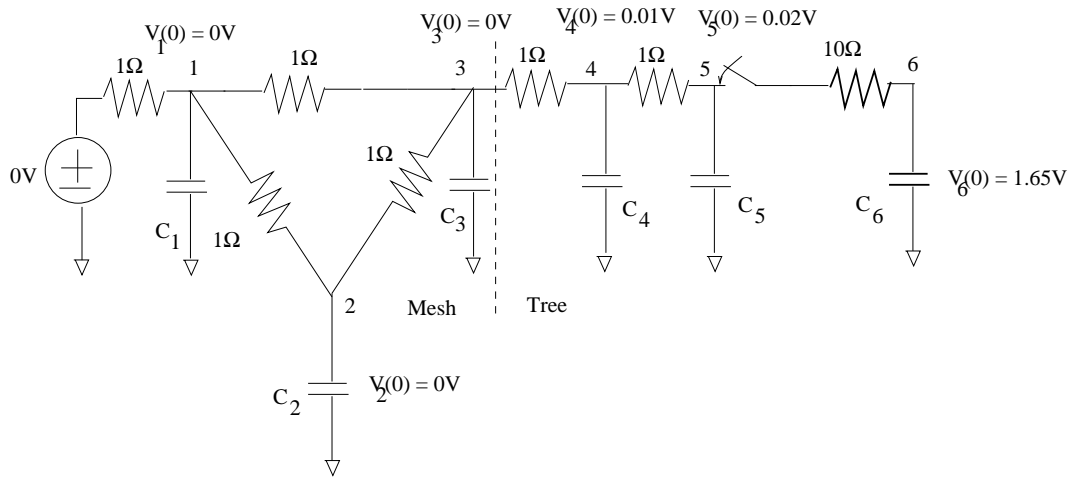


Fig. 4. A simple example (original circuit).

We show a small and simplistic example (Fig. 4) to illustrate our hierarchical analysis method. For simplicity we use RC modeling for wires. The circuit shown in Fig. 4 is a

ground network with a mesh (nodes 1, 2 and 3) driving a tree (nodes 3, 4, 5 and 6) at node 3. An RC element ( $R_{56}$  and  $C_6$ ) with  $C_6(0) = 1.65V$  is switching into the tree. We assume  $C_1 = C_2 = C_4 = 0.2pF$ ,  $C_3 = 0.3pF$ ,  $C_5 = 0.1pF$  and  $C_6 = 1pF$ . Initial voltages on  $C_4$  and  $C_5$  are assumed to be  $0.01V$  and  $0.02V$  (non-zero due to previous switching events).

The MNA equation for the tree:

$$\begin{aligned}
& (\mathbf{G}_T + s\mathbf{C}_T)\mathbf{V}_T(s) \\
& = \left( \begin{bmatrix} 1 & -1 & 0 & 0 & 1 \\ -1 & 2 & -1 & 0 & 0 \\ 0 & -1 & 1.1 & 0.1 & 0 \\ 0 & 0 & -0.1 & 0.1 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} + s \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0.2e-12 & 0 & 0 & 0 \\ 0 & 0 & 0.1e-12 & 0 & 0 \\ 0 & 0 & 0 & 1e-12 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \right) \begin{bmatrix} v(3) \\ v(4) \\ v(5) \\ v(6) \\ i(3) \end{bmatrix} \\
& = \begin{bmatrix} 0 & 0 \\ 0 & 2e-15 \\ 0 & 2e-15 \\ 0 & 1.65e-12 \\ -1 & 0 \end{bmatrix} \begin{bmatrix} u_3 \\ 1 \end{bmatrix} = \mathbf{B}_T \mathbf{u}_{port}
\end{aligned}$$

$$\mathbf{i}_{port} = \mathbf{L}_T^T \mathbf{V}_T(s) + \mathbf{i}_{Tinit} = [0 \ 0 \ 0 \ 0 \ -1] \begin{bmatrix} v(3) \\ v(4) \\ v(5) \\ v(6) \\ i(3) \end{bmatrix} + \begin{bmatrix} 0 \\ 2e-15 \\ 2e-15 \\ 1.65e-12 \\ 0 \end{bmatrix} \tag{16}$$

We choose  $q_T = 3$  and therefore the orthonormal basis  $\mathbf{X}$  can be obtained by two iterations and truncation of the last column.

$$\mathbf{X} = \begin{bmatrix} -0.500 & -0.389 & -0.491 \\ -0.500 & -0.283 & 0.226 \\ -0.500 & -0.179 & 0.415 \\ -0.500 & 0.852 & -0.150 \\ 4.44e-17 & 0.106 & 0.716 \end{bmatrix} \tag{17}$$



Reduced matrices for the tree:

$$\begin{aligned} \tilde{\mathbf{G}}_{\mathbf{T}} &= \begin{bmatrix} 2.08e-17 & -0.0528 & -0.358 \\ 0.0528 & 0.128 & -0.19 \\ 0.358 & 0.264 & 0.581 \end{bmatrix}, \quad \tilde{\mathbf{C}}_{\mathbf{T}} = \begin{bmatrix} 3.25e-13 & -3.88e-13 & 3.19e-14 \\ -3.88e-13 & 7.44e-13 & -1.48e-13 \\ 3.19e-14 & -1.48e-13 & 5.01e-14 \end{bmatrix}, \\ \tilde{\mathbf{B}}_{\mathbf{T}} &= \begin{bmatrix} -4.44e-17 & -8.45e-13 \\ -0.106 & 1.40e-12 \\ -0.716 & -2.35e-13 \end{bmatrix}, \quad \tilde{\mathbf{L}}_{\mathbf{T}} = \begin{bmatrix} -4.44e-17 \\ -0.106 \\ -0.716 \end{bmatrix} \end{aligned} \quad (18)$$

Poles and residues can be further calculated out and the zero-input response and impulse response of every tree node can be evaluated.

Stamping the reduced tree matrices into the mesh MNA equation:

$$\begin{aligned} &(\mathbf{G}_{\mathbf{M}} + s\mathbf{C}_{\mathbf{M}})\mathbf{V}_{\mathbf{M}}(s) \\ &= \begin{pmatrix} \begin{bmatrix} 3 & -1 & -1 & 0 & 0 & 0 & 0 \\ -1 & 2 & -1 & 0 & 0 & 0 & 0 \\ -1 & -1 & 2 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 4.44e-17 & 0.106 & 0.716 \\ 0 & 0 & 4.44e-17 & 0 & 2.08e-17 & -0.0528 & -0.358 \\ 0 & 0 & 0.106 & 0 & 0.0528 & 0.128 & -0.190 \\ 0 & 0 & 0.716 & 0 & 0.3580 & 0.264 & 0.581 \end{bmatrix} \\ +s \begin{bmatrix} 0.2e-12 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0.2e-12 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0.3e-12 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 3.25e-13 & -3.88e-13 & 3.19e-14 \\ 0 & 0 & 0 & 0 & -3.88e-13 & 7.44e-13 & -1.48e-13 \\ 0 & 0 & 0 & 0 & 3.19e-14 & -1.48e-13 & 5.01e-14 \end{bmatrix} \end{pmatrix} \begin{bmatrix} v(1) \\ v(2) \\ v(3) \\ i(3) \\ \\ \tilde{\mathbf{v}}_{\mathbf{T}} \end{bmatrix} \\ &= \begin{bmatrix} 0 & 0 & 0 & 0 & -8.45e-13 & 1.40e-12 & -2.35e-13 \end{bmatrix}^T = \mathbf{J}_{\mathbf{M}}(s) \end{aligned} \quad (19)$$

After solving Eqn. 19 using PRIMA again, the poles and residues of every mesh node

can be obtained, and so is the zero-input response of every mesh node. The total response of every tree node can be computed by propagating the waveform of node 3 using Eqn. (11).

### III. ADJOINT SENSITIVITY COMPUTATION OVER MULTIPLE SWITCHING INTERVALS

Adjoint sensitivity analysis is a standard technique for circuit optimization where the sensitivity of one output with respect to many parameter values is required [18]. In adjoint sensitivity analysis, Tellegen's theorem is applied to a pair of circuits with the same topology by combining the branch currents and voltages at any two instants of time.

For our problem, we simulate the P/G network over the specified event list. At the beginning of each event, a set of switching activities occurs, with some RC elements switching out of the network and others switching in. This complicates the task of adjoint sensitivity computation since the topology changes for each interval. One contribution of this work is to extend adjoint analysis to handle this variant topology.

#### A. Adjoint sensitivity analysis over variant topology

For multiple switching intervals in which the structure of the circuit can change between intervals, with elements being added or removed from the circuit, the traditional adjoint sensitivity approach [18] cannot be directly applied. In this section, we show an extension of adjoint sensitivity to our problem, and a detailed derivation and proof is provided in the appendix.

Suppose there are a total of  $f+1$  events, each event is lasting from  $t_{k-1}$  to  $t_k$ ,  $k=1$  to  $f$ , where  $t_0=0$ , and suppose the worst-case voltage drop happens at  $T_{peak}$  and  $t_{p-1} < T_{peak} < t_p$ , the procedure of the variant adjoint sensitivity analysis is summarized as follows:

- Select the initial topology of the adjoint circuit the same as the original circuit between event  $f$  and  $f+1$ . Set initial conditions in the adjoint circuit zero.

- Apply a current source of  $-\delta(t - T_{peak})$  or  $u(t - t_{sk}) - u(t - t_{ek})$  to the worst-case voltage drop node, depending on the chosen noise metric.
- Analyze the adjoint circuit in the backward order of switching event (from event  $f+1$  to 1). Set the initial condition of the circuit at the beginning of each backward event. This ensures the adjoint circuit the same topology as the original one between pairs of corresponding switching intervals.
- Convolve the original and adjoint waveforms using Eqn. (41), (42) (43) and (44) to compute the adjoint sensitivities with respect to every capacitor, resistor and inductor in the circuit.

### B. Closed-form Transient Sensitivity Formula

The simulation technique as discussed in Section II can be applied to analyze the adjoint P/G network in backward time. This requires the computation of the response to the input  $u(\tau - \tau_{sk}) - u(\tau - \tau_{ek})$  applied to the most critical node, where  $u(t)$  represents the step function. If we compute the impulse response,  $\omega(s)$ , corresponding to an excitation of  $\delta(\tau)$  applied to the most critical node, then the response to the above signal is  $v(s) = \omega(s)(e^{-s\tau_{sk}} - e^{-s\tau_{ek}})/s$ .

The event-driven simulation of the adjoint P/G network is performed in a backward order of the specified events, so that the topology of the adjoint network is also changing in the reverse temporal order. The response of the tree with the most critical node is the superposition of  $v(\tau) = L^{-1}(v(s))$ , the voltage response propagated from the root (mesh node) and its zero-input response which is non-zero for all the backward events except for the very first one, where  $L^{-1}$  is the inverse Laplace operator.

Given the nodal voltage  $v(t)$  (for capacitors) and branch current  $i(t)$  (for resistors or

inductors) having the following form as indicated from Eqn. (10) and (15):

$$f^k(t) = \sum_{i=1}^P r_i e^{\lambda_i t}, \quad 0 \leq t \leq T_k, \quad T_k = t_k - t_{k-1}, \quad (20)$$

the nodal voltage  $\psi(\tau)$  (for capacitors) and branch current  $\varphi(\tau)$  (for resistors or inductors) can be represented as

$$g^k(\tau) = \begin{cases} \sum_{j=1}^Q r_{z_j} e^{\Lambda_j \tau}, & 0 \leq \tau \leq T_k - t_{e_k} \\ \sum_{j=1}^Q r_{z_j} e^{\Lambda_j \tau} + \sum_{j=1}^{Q+1} R_j e^{\Lambda_j(\tau - T_k + t_{e_k})}, & T_k - t_{e_k} \leq \tau \leq T_k - t_{s_k} \\ \sum_{j=1}^Q r_{z_j} e^{\Lambda_j \tau} + \sum_{j=1}^{Q+1} R_j e^{\Lambda_j(\tau - T_k + t_{e_k})} - \sum_{j=1}^{Q+1} R_j e^{\Lambda_j(\tau - T_k + t_{s_k})}, & T_k - t_{s_k} \leq \tau \leq T_k, \end{cases} \quad (21)$$

where  $T_k = t_k - t_{k-1}$ ,  $\Lambda_j$  is the  $j$ th pole,  $r_{z_j}$  is the  $j$ th residue of the zero-input response and  $R_j$  is the  $j$ th residue of the response to the current source of  $u(\tau - \tau_{s_k}) - u(\tau - \tau_{e_k})$  at every switching event  $k$ .

Transient adjoint sensitivity calculation is performed using Eqn. (41), (42) (43) or (44). As an example, the transient adjoint sensitivity of the noise integral, denoted as  $Z$ , with respect to a capacitor  $C$  can be computed as:

$$\begin{aligned} \frac{\partial Z}{\partial C} &= \sum_{k=1}^f \left\{ - \int_0^{T_k} \sum_{i=1}^P r_i \lambda_i e^{\lambda_i t} \sum_{j=1}^Q r_{z_j} e^{\Lambda_j(T_k - t)} dt \right. \\ &\quad \left. - \int_0^{t_{e_k}} \sum_{i=1}^P r_i \lambda_i e^{\lambda_i t} \sum_{j=1}^{Q+1} R_j e^{\Lambda_j(t_{e_k} - t)} dt + \int_0^{t_{s_k}} \sum_{i=1}^P r_i \lambda_i e^{\lambda_i t} \sum_{j=1}^{Q+1} R_j e^{\Lambda_j(t_{s_k} - t)} dt \right\} \\ &= \begin{cases} - \sum_{i=1}^P \sum_{j=1}^Q r_i \lambda_i r_{z_j} e^{\Lambda_j T_k} T_k - \sum_{i=1}^P \sum_{j=1}^{Q+1} r_i \lambda_i R_j e^{\Lambda_j t_{e_k}} t_{e_k} + \sum_{i=1}^P \sum_{j=1}^{Q+1} r_i \lambda_i R_j e^{\Lambda_j t_{s_k}} t_{s_k}, & \lambda_i = \Lambda_j \\ - \sum_{i=1}^P \sum_{j=1}^Q \frac{r_i \lambda_i r_{z_j} [e^{\lambda_i T_k} - e^{\Lambda_j T_k}]}{\lambda_i - \Lambda_j} - \sum_{i=1}^P \sum_{j=1}^{Q+1} \frac{r_i \lambda_i R_j [e^{\lambda_i t_{e_k}} - e^{\Lambda_j t_{e_k}}]}{\lambda_i - \Lambda_j} + \sum_{i=1}^P \sum_{j=1}^{Q+1} \frac{r_i \lambda_i R_j [e^{\lambda_i t_{s_k}} - e^{\Lambda_j t_{s_k}}]}{\lambda_i - \Lambda_j}, & \lambda_i \neq \Lambda_j \end{cases} \quad (22) \end{aligned}$$

#### IV. HEURISTIC OPTIMIZATION

The optimization technique used in this work is a sensitivity-based heuristic that is similar to the TILOS [12] algorithm, which is a greedy heuristic optimizer that changes the

parameters that provide the “biggest bang for the buck.” The basic philosophy of optimizing the P/G network using this technique is to try to reduce the maximum voltage drop violation in the network with the minimum increase in the area, by successively increasing parameter sizes by a small amount in each iteration.

The problem of optimizing a P/G network by varying wire widths can be formulated as

$$\begin{aligned} \text{Minimize Area} &= \sum_i l_i w_i \\ \text{Subject to } \text{Max}(Z) &= 0 \\ \text{and } w_{min} &\leq w_i \leq w_{max} \end{aligned}$$

In the objective function,  $l_i$  represents the total length of a set of the P/G wire segments with width  $w_i$ , where  $w_i$ 's are the optimization variables and they are subject to the minimum and maximum wire width constraints. In each iteration, we first analyze the original network to identify the most critical node with the maximum voltage drop integral, then determine the parameter of the network that this critical node is most sensitive to, by transient adjoint analysis, and finally bump up the width of this parameter by a certain small amount so that the most critical voltage drop integral is reduced. It should be noted that the most critical node can be different during different iterations.

In our method, we divide each wire in the mesh/trees into several  $\pi$ -segments, but model a set of adjacent wires as having the same width in order to reduce the network of optimization parameters. The gradients with respect to the area  $A_i$  of each set of  $N$  wires with width  $w_i$  is computed using the chain rule as follows:

$$\frac{\partial Z}{\partial A_i} = \frac{\partial Z}{\partial w_i} \times \frac{\partial w_i}{\partial A_i} = \frac{\partial Z}{\partial w_i} \times \frac{1}{\sum_{j=1}^N l_j} \quad (23)$$

and

$$\frac{\partial Z}{\partial w_i} = \sum_{j=1}^N \left[ \frac{\partial Z}{\partial C_{j1}} \frac{\partial C_{j1}}{\partial w_j} + \frac{\partial Z}{\partial C_{j2}} \frac{\partial C_{j2}}{\partial w_j} + \frac{\partial Z}{\partial R_j} \frac{\partial R_j}{\partial w_j} + \frac{\partial Z}{\partial L_j} \frac{\partial L_j}{\partial w_j} \right] \quad (24)$$

where the set of wires with width  $w_i$  consists of  $N$  wire segments; each of the segment  $j$  has resistance  $R_j$ , inductance  $L_j$ , and capacitance  $C_{j1}$ ,  $C_{j2}$  at each terminal of the wire.

From (1), it is easy to see that

$$\frac{\partial R_j}{\partial w_j} = -\rho l_j / w_j^2 \quad (25)$$

$$\frac{\partial L_j}{\partial w_j} = -\gamma l_j / w_j^2 \quad (26)$$

$$\frac{\partial C_{j1}}{\partial w_j} = \frac{\partial C_{j2}}{\partial w_j} = \frac{\beta l_j}{2} \quad (27)$$

The overall optimization procedure is as follows:

- Simulate the original P/G network over the entire period using the hierarchical simulation method discussed in Section II.
- Determine the most critical node with its  $Z_{max}$ .
- Save voltage approximants (poles and residues) for all C's and current approximants for all R's and L's in the network.
- Simulate the adjoint network backward in time (event) with zero initial conditions.
- Save voltage/current waveforms for the adjoint network.
- Compute the voltage sensitivities with respect to all R's, L's and C's.
- Compute the voltage sensitivities with respect to  $A_i$  using Eqn. (23), (24), (25), (26) and (27).
- Bump up the width of the set of wires with maximum sensitivity by multiplying it with a small factor ( $< 1.1$ ).
- Repeat the above procedure until the maximum voltage drop integral in the network is below zero.

The above procedure can be extended to include the optimization of decoupling capacitors. The objective of this optimization is to determine appropriate sizes of each wire and each decoupling capacitor for the minimum area overhead. Initially, decoupling capacitors

with some small values are connected to some user-specified nodes in the P/G network. The gradients of the most critical node with respect to these decoupling capacitors are exactly the transient adjoint sensitivities calculated in each iteration. The cost function for the optimization is a weighted sum of the wire area and the areas of all the decoupling capacitors. In each iteration, either the wire width or the decoupling capacitor with the maximum sensitivity with respect to the objective function will be increased with a small factor until the constraints are met.

## V. EXPERIMENTAL RESULTS

The simulation and optimization procedure was implemented in C, and the results on several P/G networks were tested. The networks were constructed randomly for power delivery to a 2cm x 2cm chip in a  $0.18\mu m$  technology with  $V_{dd} = 1.65V$ . The set of events is randomly generated and is different for each P/G network. The set of most critical nodes are chosen as the nodes close to those actively switching RC elements. The results shown here can be considered to correspond to a top level P/G distribution network, since complete P/G networks may have several millions of nodes. The utilization points here would correspond to functional blocks, each of which is reduced to an equivalent RC representation.

We have used the commercial simulator, HSPICE, to analyze the speed and accuracy of our simulation results. All experiments are performed on Sun Ultra-60 Workstations.

The waveforms for two networks are shown in Fig. 5, with the waveforms using HSPICE plotted concurrently on the same figures using dotted lines. In each case, our waveform and that of HSPICE are quite close. The order of approximation is chosen such as the integral of noisy area is within 10% to that of HSPICE.

The comparison of the run-time for the two cases and the speedup are shown in Table I. It can be seen that our simulation runs significantly faster than HSPICE.

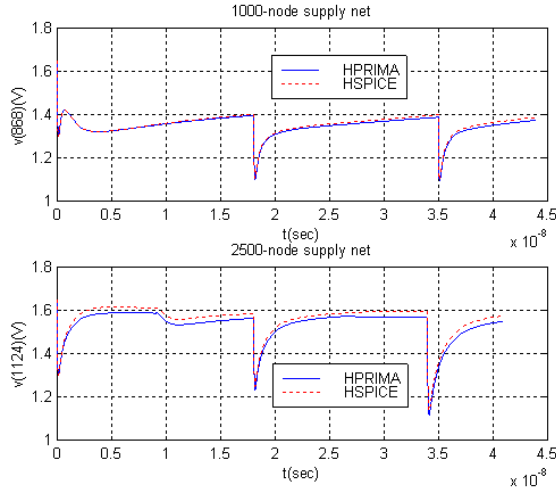


Fig. 5. Simulation results on a 1000-node and a 2500-node supply network. The reduced orders for the two networks are 13 and 15, respectively. HPRIMA stands for our Hierarchical PRIMA simulator.  $V_{dd} = 1.65V$ .

Table II lists the results of optimization and the run-time for five different P/G networks with and without decaps. Two rows are listed for each case, with the first row showing wire sizing results only and the second row showing both wire sizing and decap optimization. The total number of nodes (“total”) and the number of user-specified critical nodes (“crt”) are listed. The results for the specific voltage constraint, listed in the “spec” column, are shown, along with the total wire area. The “ $Z_{max}$ ” and the “Init  $V_m$ ” column refer to the worst-case noise integral and the worst-case voltage level when all wires are unsized. The “Opt  $V_m$ ” column shows the voltage drop after the specifications are met or when  $Z_{max}$  is optimized to zero. The CPU times and the number of iterations of the heuristic optimizer are shown in the last two columns.

Table III shows the comparison between two networks with different topologies. Circuit 1 deviates from the one-level hierarchical scheme shown in Fig. 1, and is a two-level hierarchy in which the top level is a 9-node mesh with a tree of 112 nodes originating from each mesh node; we will refer to such a structure as a “9x112 structure”. Some of the tree nodes of this upper level are connected to separate 9x112 structures. Specifically, in the structure



here, we have a total of nine such 9x112 bottom level structures. Pads are assigned to each of these bottom level networks. The optimization is performed hierarchically. The bottom-level net is first optimized to within 7% of  $V_{dd}$  with a voltage source of  $97\%V_{dd}$  applied to the connecting node to the top-level network. The top-level net is then optimized to within 3% of  $V_{dd}$  with the reduced order model connected to the top-level network. As a result, the two-level hierarchical network has a worst-case voltage drop of  $10\%V_{dd}$ . Optimizing a network to within 3% of  $V_{dd}$  normally takes more CPU time than optimizing it to 7%. Since we have only 1 top-level network and 9 bottom-level networks in the 2-level hierarchical structure, intuitively the selection of the constraint of 3% for the 1 top-level network and 7% for the 9 bottom-level networks should lead to some smaller total amount of CPU time. For comparison, a one-level 90x112 network (circuit 2) is constructed and optimized. The optimization results show that the two-level hierarchy can be performed far more quickly than the one-level network with similar wire areas and performance.

Ckt	# of nodes		$T_{HPRIMA}$ (s)	$T_{HSPICE}$ (s)	Speed $U_p$
	Mesh/Tree	Crt			
1	9/1008	10	1.59	82.42	51.84
2	25/2500	25	4.24	232.09	54.74
3	25/3000	32	7.50	325.42	43.39
4	25/4000	38	9.42	499.53	53.03
5	25/5000	38	10.37	680.15	65.59
6	49/10800	78	18.87	1641.02	86.96

TABLE I  
RUNTIME COMPARISONS WITH HSPICE.

## VI. CONCLUSION

An efficient transient sensitivity computation method for P/G network design and optimization is presented. A fast and efficient event-driven P/G network simulator is developed. Experimental results show that the simulation is accurate and fast. The optimization procedure involves a procedure for fast calculation of adjoint sensitivities in a heuristic optimiza-

Ckt	# of nodes		Spec	$Z_{max}$ ( $V \times ns$ )	Init $V_m$ ( $V$ )	Opt $V_m$ ( $V$ )	Wire Area ( $cm^2$ )	Max Decap ( $nF$ )	Num of Decap	CPU time ( $hrs$ )	Num of Itr
	Total	Crt									
1	1017	10	0.165	7.50	0.698	0.161	0.083	-	-	0.35	109
1	1017	10	0.165	1.13	0.718	0.165	0.045	0.0379	9	0.41	142
2	2016	19	1.485	8.34	1.080	1.488	0.172	-	-	0.92	125
2	2016	19	1.485	2.39	1.174	1.485	0.125	0.3450	13	0.78	117
3	3025	32	0.165	6.60	0.760	0.165	0.347	-	-	3.64	276
3	3025	32	0.165	1.46	0.544	0.165	0.225	1.7700	20	2.42	186
4	5025	38	1.485	4.81	1.058	1.485	0.651	-	-	4.60	231
4	5025	38	1.485	0.59	1.058	1.485	0.476	0.1460	24	3.51	195
5	9849	78	1.485	0.81	1.224	1.485	0.119	-	-	8.60	256
5	9849	78	1.485	0.42	1.224	1.485	0.109	1.3310	30	7.58	227

TABLE II  
OPTIMIZATION RESULTS.

Ckt	# level	# of nodes		Spec	$Z_{max}$ ( $V \times ns$ )	Init $V_m$ ( $V$ )	Opt $V_m$ ( $V$ )	Wire Area ( $cm^2$ )	Max Decap ( $nF$ )	Num of Decap	CPU time ( $hrs$ )
		Mesh/Tree	Crt								
1	2	90/10080	100	1.485	12.07	1.260	1.486	1.323	1.1918	30	3.74
2	1	90/10080	100	1.485	16.72	1.120	1.485	1.308	1.2100	30	33.51

TABLE III  
TOPOLOGY COMPARISON

tion loop. This procedure is illustrated on a specific family of topologies described in Fig. 1, with an example of two-level hierarchy of such a topology. It can also be extended to other mesh topologies that have an overall tree-like structure, e.g., a tree-like macro structure in which each vertex is a mesh.

Because of the changing of topology, our PRIMA-based analysis technique has to perform model order reduction for each topology and is not able to take the advantage of circuit changes, because any such changes will change the reduction matrix  $\mathbf{X}$ . The procedure could be made more efficient if the model order reduction can be done incrementally.

## REFERENCES

- [1] G. Bai, S. Bobba, and I. N. Hajj. Simulation and Optimization of the Power Distribution Network in VLSI Circuits. In *Proc. International Conference on Computer-Aided Design*, pages 481–486, San Jose, CA, November 2000.

- [2] S. Bobba and I. N. Hajj. Estimation of Maximum Current Envelope for Power Bus Analysis and Design. In *Proc. International Symposium on Physical Design*, pages 141–146, Monterey, CA, April 2001.
- [3] S. Boyd, L. Vandenberghe, A. E. Gamal, and S. Yun. Design of Robust Global Power and Ground Networks. In *Proc. International Symposium on Physical Design*, pages 60–65, Napa, CA, April 2001.
- [4] Y. Cao, Y.-M. Lee, T.-H. Chen, and C. C.-P. Chen. HiPRIME: Hierarchical and Passivity Reserved Interconnect Macromodeling Engine for RLKC Power Delivery. In *Proc. Design Automation Conference*, pages 379–384, New Orleans, LA, June 2002.
- [5] H. H. Chen and D. D. Ling. Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design. In *Proc. Design Automation Conference*, pages 638–643, Anaheim, CA, June 1997.
- [6] S. Chowdhry and J. S. Barkatullah. Estimation of Maximum Currents in MOS IC Logic Circuits. *IEEE Transactions on Computer-Aided Design*, 9:642–654, June 1990.
- [7] S. Chowdhury and J. S. Barkatullah. Estimation of Maximum Currents in MOS IC Logic Circuits. *IEEE Transactions on Computer-Aided Design of ICs and Systems*, 9(6):642–654, June 1990.
- [8] A. R. Conn, R. A. Haring, and C. Visweswariah. Noise Considerations in Circuit Optimization. In *Proc. International Conference on Computer-Aided Design*, pages 220–227, San Jose, CA, November 1998.
- [9] A. Dharchoudhury, R. Panda, D. Blaauw, and R. Vaidyanathan. Design and Analysis of Power Distribution Networks in PowerPC<sup>TM</sup> Microprocessors. In *Proc. Design Automation Conference*, pages 738–743, June 1998.
- [10] S. W. Director and R. A. Rohrer. The Generalized Adjoint Network and Network

- Sensitivities. *IEEE Transactions on Circuit Theory*, CT-16:318–323, August 1969.
- [11] P. Feldmann, T. V. Nguyen, S. W. Director, and R. A. Rohrer. Sensitivity Computation in Piecewise Approximate Circuit Simulation. *IEEE Transactions on Computer-Aided Design*, 10:171–183, February 1991.
- [12] J. P. Fishburn and A. E. Dunlop. TILOS: A Posynomial Programming Approach to Transistor Sizing. In *Proc. International Conference on Computer-Aided Design*, pages 326–328, San Jose, CA, November 1985.
- [13] A. D. Kraus. *Circuit Analysis*. West Publishing Company, St. Paul, MN, 1991.
- [14] A. Krstic and K.-T. T. Cheng. Vector Generation for Maximum Instantaneous Current Through Supply Lines for CMOS Circuits. In *Proc. Design Automation Conference*, pages 383–388, Anaheim, CA, June 1997.
- [15] T. Mitsuhashi and E. S. Kuh. Power and Ground Network Topology Optimization for Cell-based VLSIs. In *Proc. Design Automation Conference*, pages 524–529, June 1992.
- [16] S. R. Nassif and J. N. Kozhaya. Fast Power Grid Simulation. In *Proc. Design Automation Conference*, pages 156–161, Los Angeles, CA, June 2000.
- [17] A. Odabasioglu, M. Celik, and L. T. Pilleggi. PRIMA: Passive Reduced-order Interconnect Macromodeling Algorithm. *IEEE Transactions on Computer-Aided Design*, 17:645–654, Aug 1998.
- [18] L. T. Pillage, R. A. Rohrer, and C. Visweswariah. *Electronic and System Simulation Methods*. McGraw-Hill, New York, NY, 1995.
- [19] C. L. Ratzlaff, N. Gopal, and L. T. Pillage. RICE: Rapid Interconnect Circuit Evaluator. In *Proc. Design Automation Conference*, pages 555–561, June 1991.
- [20] W. Rudin. *Real and Complex Analysis*. McGraw-Hill, New York, NY, 1987.
- [21] J. C. Shah, A. A. Younis, S. S. Sapatnekar, and M. M. Hassoun. An Algorithm for

- Simulating Power/Ground Networks Using Padé Approximants and its Symbolic Implementation. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 45:1372–1382, October 1998.
- [22] B. R. Stanasic, R. A. Rutenbar, and L. R. Carley. Addressing Noise Decoupling in Mixed-signal IC's: Power Distribution design and Cell Customization. *IEEE Journal of Solid-State Circuits*, 30:321–326, March 1995.
- [23] B. R. Stanasic, N. K. Verghese, R. A. Rutenbar, L. R. Carley, and D. J. Allstot. Addressing Substrate Coupling in Mixed-mode IC's: Simulation and Power Distribution Synthesis. *IEEE Journal of Solid-State Circuits*, 29:226–238, March 1994.
- [24] D. Stark and M. Horowitz. Techniques for Calculating Currents and Voltages in VLSI Power Supply Networks. *IEEE Transactions on Computer-Aided Design of ICs and Systems*, 9:126–132, February 1979.
- [25] X. Tan, C. J. R. Shi, D. Lungeanu, J. Lee, and L. Yuan. Reliability-Constrained Area Optimization of VLSI Power/Ground Networks Via Sequence of Linear Programmings. In *Proc. Design Automation Conference*, pages 156–161, New Orleans, LA, June 1999.
- [26] J. M. Wang and T. V. Nguyen. Extended Krylov Subspace Method for Reduced Order Analysis of Linear Circuits with Multiple Sources. In *Proc. Design Automation Conference*, pages 247–252, Los Angeles, CA, June 2000.
- [27] M. Zhao, R. V. Panda, S. S. Sapatnekar, T. Edwards, R. Chaudhry, and D. Blaauw. Hierarchical Analysis of Power Distribution Networks. In *Proc. Design Automation Conference*, pages 481–486, Los Angeles, CA, June 2000.

## APPENDIX

This appendix describes the extension of the traditional adjoint sensitivity analysis technique to our scenario where the structure of the circuit can change between intervals, with

elements being added to and removed from the circuit from one interval to the next. The basic approach was outlined in Section III A, and a formal proof for the extension is provided within this appendix.

The basis for adjoint analysis comes from Tellegen's theorem, which when integrated over a time period of interest from  $t_0$  to  $t_f$ , gives

$$\sum_{\text{all branches}} \int_{t_0}^{t_f} [\varphi(\tau)\delta v(t) - \psi(\tau)\delta i(t)]dt = 0 \quad (28)$$

Suppose there are a total of  $f + 1$  events, each event is lasting from  $t_{k-1}$  to  $t_k$ ,  $k=1$  to  $f$ , where  $t_0=0$ . Then (13) becomes

$$\sum_{\text{all branches}} \sum_{k=1}^{f-1} \int_{t_{k-1}}^{t_k} [\varphi^{(k)}(\tau)\delta v^{(k)}(t) - \psi^{(k)}(\tau)\delta i^{(k)}(t)]dt = 0 \quad (29)$$

The superscript  $(k)$  denotes the voltage or current response corresponding to the topology between switching event  $k-1$  and  $k$ .

If we are interested in the sensitivity of  $v(t)$  at some moment  $t$ , we isolate  $\delta v(t)$  by setting all voltage sources in the adjoint circuit to zero. The left-hand side of the sensitivity term becomes

$$\sum_{\text{all current sources}} \left[ \sum_{k=1}^{f-1} \int_{t_{k-1}}^{t_k} -\varphi^{(k)}(\tau)\delta v^{(k)}(t)dt \right] \quad (30)$$

Suppose the most critical voltage drop occurs at  $t = T_{peak}$ . To obtain the term  $\delta v(T_{peak})$ , we set an impulse current source at the node of interest in the adjoint network, i.e.,

$$\varphi^{(p)}(\tau) = -\delta(t - T_{peak}) \quad (31)$$

where  $t_{p-1} < T_{peak} < t_p$ . Only for interval  $t_{p-1} < T_{peak} < t_p$ , this term is non-zero:

$$\int_{t_{p-1}}^{t_p} \delta(t - T_{peak})\delta v^{(p)}(t)dt = \delta v^{(p)}(T_{peak}) \quad (32)$$

which is exactly what is desired in the left-hand side of the sensitivity term.

As described in Section I, in our work, the performance of power/ground network is measured using the shaded area beyond the threshold voltage (noise margin) shown in Fig. 3. Suppose the most critical node has only one overshoot between  $t_{sk}$  and  $t_{ek}$  during event  $k$ , the sum of shaded area, denoted by  $Z$ , over all switching events can be represented as

$$Z = \sum_{k=1}^f \int_{t_{sk}}^{t_{ek}} [NM_H - v(t)] dt \quad (33)$$

As discussed in [8], instead of applying an impulse current source of  $-\delta(t - T_{peak})$ , a current pulse of  $u(t - t_{sk}) - u(t - t_{ek})$ ,  $k = 1 \dots f$ , is applied to the most critical node. Then Eqn. (30) becomes:

$$\sum_{k=1}^f \int_{t_{k-1}}^{t_k} [-u(t - t_{sk}) + u(t - t_{ek})] \delta v(t) dt = \sum_{k=1}^f \int_{t_{sk}}^{t_{ek}} -\delta v(t) dt = \delta Z \quad (34)$$

which, similar to Eqn. (32), is exactly what is desired in the left-hand side of the sensitivity term.

#### A. Sensitivity with respect to capacitors

For capacitors, we have the device equation

$$\begin{aligned} i_C &= C \dot{v}_C(t) \\ \delta i_C(t) &= C \delta \dot{v}_C(t) + \dot{v}_C(t) \delta C \end{aligned} \quad (35)$$

From Eqn. (29), the right-hand side of the sensitivity term becomes

$$\sum_{k=1}^f \int_{t_{k-1}}^{t_k} \{ \varphi_C^{(k)}(\tau) \delta v_C^{(k)}(t) - \psi_C^{(k)}(\tau) [C \delta \dot{v}_C^{(k)}(t) + \dot{v}_C^{(k)}(t) \delta C] \} dt \quad (36)$$

We can integrate by part the  $\delta \dot{v}_C^{(k)}(t)$  term in Eqn. (36) to obtain<sup>3</sup>:

$$\begin{aligned} & \sum_{k=1}^f [-\psi_C^{(k)}(\tau) C \delta v_C^{(k)}(t) \Big|_{t_{k-1}}^{t_k} - \delta C \int_{t_{k-1}}^{t_k} \psi_C^{(k)}(\tau) \dot{v}_C^{(k)}(t) dt] \\ & + \sum_{k=1}^f \int_{t_{k-1}}^{t_k} [\varphi_C^{(k)}(\tau) \delta v_C^{(k)}(t) + C \dot{\psi}_C^{(k)}(\tau) \delta v_C^{(k)}(t)] dt \end{aligned} \quad (37)$$

<sup>3</sup> Note that  $\dot{\psi}_C$  and  $\dot{v}_C$  are not defined everywhere. In particular, at switching time points, the derivatives can be discontinuous although the function is continuous. However, removing a finite number of points constitutes the removal of a set of zero measure and does not alter the evaluated value of the integral, where  $\dot{\psi}_C$  and  $\dot{v}_C$  are continuous [20].

As in normal adjoint calculation, to avoid negative energy storage elements, we choose  $\tau$  to be the backward time in each interval  $k$ . Thus we have

$$\tau = t_{k-1} + t_k - t \quad (38)$$

The capacitor in the adjoint circuit can be chosen as

$$\varphi_C(\tau) = -C\dot{\psi}_C(\tau) = -C\frac{d\psi(\tau)}{dt} = C\frac{d\psi(\tau)}{d\tau} \quad (39)$$

which is an ordinary capacitor. So Eqn. (37) becomes

$$\begin{aligned} & \sum_{k=1}^f \left[ -\psi_C^{(k)}(\tau)C\delta v_C^{(k)}(t)|_{t_{k-1}}^{t_k} - \delta C \int_{t_{k-1}}^{t_k} \psi_C^{(k)}(\tau)\dot{v}_C^{(k)}(t)dt \right] = \\ & -\psi_C^{(1)}(t_0)C\delta v_C^{(1)}(t_1) + \psi_C^{(1)}(t_1)C\delta v_C^{(1)}(t_0) - \delta C \int_{t_0}^{t_1} \psi_C^{(1)}(\tau)\dot{v}_C^{(1)}(t)dt \\ & -\psi_C^{(2)}(t_1)C\delta v_C^{(2)}(t_2) + \psi_C^{(2)}(t_2)C\delta v_C^{(2)}(t_1) - \delta C \int_{t_1}^{t_2} \psi_C^{(2)}(\tau)\dot{v}_C^{(2)}(t)dt \\ & \dots\dots\dots \\ & -\psi_C^{(f)}(t_{f-1})C\delta v_C^{(f)}(t_f) + \psi_C^{(f)}(t_f)C\delta v_C^{(f)}(t_{f-1}) - \delta C \int_{t_{f-1}}^{t_f} \psi_C^{(f)}(\tau)\dot{v}_C^{(f)}(t)dt \end{aligned} \quad (40)$$

To remove the integration-by-parts term in Eqn. (40), we use the following procedure:

- $\psi_C^f(t_{f-1}) = 0$ (initial conditions for the adjoint circuit is set to zero)
- $\psi_C^k(t_k) = \psi_C^{k-1}(t_{k-2}), k = 2, \dots, f$
- $\delta v_C^1(t_0) = 0$ (by definition, since the initial conditions of the original circuit are known)

This will set all the non-integral terms in Eqn. (40) to zero. In case there is only one interval, this result reduces to the conventional adjoint sensitivity calculation procedure [18] that sets  $\psi_C(t_0) = 0$ . It can be inferred from this that the adjoint circuit simulation proceeds in the backward order of event (time).

The transient sensitivity formula with respect to capacitor  $C$  at the moment of  $T_{peak}$  is as follows:

$$\frac{\delta v^{(p)}(T_{peak})}{\delta C} = - \sum_{k=1}^p \int_{t_{k-1}}^{t_k} \psi_C^{(k)}(t_{k-1} + t_k - t)\dot{v}_C^{(k)}(t)dt \quad (41)$$

where  $t_{p-1} < T_{peak} < t_p$ . Notice that since zero-initial conditions are set in the adjoint circuit and there is no excitation until  $t = T_{peak}$  (assuming  $t_0 = 0$ ), i.e. until  $\tau = t_f - T_{peak}$ ,



$\psi_C(\tau) = 0$  when  $\tau < t_f - T_{peak}$ .  $\psi_C(\tau)$  is continuous over the period  $t_f \geq \tau \geq t_f - T_{peak}$ . In other words,  $\psi_C(t)$  is continuous over the period  $0 \leq t \leq T_{peak}$ .

Similarly, the sensitivity of  $Z$  with respect to capacitor  $C$  is:

$$\frac{\delta Z}{\delta C} = - \sum_{k=1}^f \int_{t_{k-1}}^{t_k} \psi_C^{(k)}(t_{k-1} + t_k - t) \dot{i}_C^{(k)}(t) dt \quad (42)$$

where  $\psi_C(\tau)$  is the voltage drop across capacitor  $C$  under the current excitation of  $u(\tau - \tau_{sk}) - u(\tau - \tau_{ek})$ ,  $\tau_{sk} = t_{k-1} + t_k - t_{ek}$  and  $\tau_{ek} = t_{k-1} + t_k - t_{sk}$ , applied to the most critical node.

### B. Sensitivity with respect to resistors and inductors

The sensitivity with respect to resistors and inductors can be derived similarly:

- Apply a current source of  $-\delta(t - T_{peak})$  (referring to Eqn. (32)) or  $u(t - t_{sk}) - u(t - t_{ek})$  (referring to Eqn. (34)) at the most critical node.
- Set  $\tau = t_{k-1} + t_k - t$  for each interval  $k$  to maintain  $d\tau/dt = -1$ .
- Choose  $\psi_R(\tau) = R\varphi_R(\tau)$  and  $\psi_L(\tau) = L\dot{\varphi}_L(\tau)$ .
- Set initial conditions in the adjoint circuit to zero.
- Simulate the circuit in the backward order of event

Specifically, for RLC circuits, the transient sensitivity formula with respect to  $R$  and  $L$  at  $T_{peak}$  are

$$\begin{aligned} \frac{\delta v^{(p)}(T_{peak})}{\delta R} &= \sum_{k=1}^p \int_{t_{k-1}}^{t_k} \varphi_R^{(k)}(t_{k-1} + t_k - t) i_R^{(k)}(t) dt \\ \frac{\delta v^{(p)}(T_{peak})}{\delta L} &= - \sum_{k=1}^p \int_{t_{k-1}}^{t_k} \varphi_L^{(k)}(t_{k-1} + t_k - t) \dot{i}_L^{(k)}(t) dt \end{aligned} \quad (43)$$

where  $t_{p-1} < T_{peak} < t_p$ . Similarly,  $\varphi_R(t)$  and  $\varphi_L(t)$  are continuous over the period  $0 \leq t \leq T_{peak}$ .

Similarly, the sensitivity of  $Z$  with respect to  $R$  and  $L$  are

$$\begin{aligned} \frac{\delta Z}{\delta R} &= \sum_{k=1}^f \int_{t_{k-1}}^{t_k} \varphi_R^{(k)}(t_{k-1} + t_k - t) i_R^{(k)}(t) dt \\ \frac{\delta Z}{\delta L} &= - \sum_{k=1}^f \int_{t_{k-1}}^{t_k} \varphi_L^{(k)}(t_{k-1} + t_k - t) \dot{i}_L^{(k)}(t) dt \end{aligned} \quad (44)$$