EE 8351
Design Automation Techniques for Variation-Aware Computing
3 credits

Prerequisites
This class is open to graduate students. It is recommended that students have some background in VLSI design and/or design automation. This is not a formal prerequisite for the class, but such prior exposure will make the experience in the class much more meaningful to the student.

Overview
Moore's law has dictated scaling trends for the past 50+ years, but age is beginning to take a toll and business-as-usual can no longer serve the needs of future systems. Consequently, several changes are beginning to emerge in the way chips are designed.

First, CMOS technologies are harder to scale than they used to be, with numerous challenges associated with uncertainty as designs are translated to manufactured products. This uncertainty arises from factors such as random manufacturing process variations, predictable layout-dependent performance variations, environmental variations during circuit operation, and performance degradations due to aging. Conventional methods have added conservative guardbands to allow for variations, but their overheads are unsustainable and must be replaced by new techniques that comprehend the nature of these variations and "tame" them.

Second, the traditional design paradigm was primarily directed towards the design of processor-like chips, but as the center of gravity of design moves to mobile and distributed computation that enables IoT-like systems, the requirements on individual chips begin to change. Absolute accuracy is no longer essential, and is replaced by the need for building systems that are miserly in their use of power, and deliver just enough accuracy for the application. Traditional von Neumann systems are now being supplemented by coprocessors that perform functions such as neuromorphic computing, or efficient logic-in-memory processing.

These changes require design automation tools that comprehend the needs of the designer and deliver solutions that can correctly analyze and optimize these systems. The objective of this class is to deliver a view of this emerging universe and acquaint students with new research in this area.

Specific topics to be covered include:
- Overview of technology trends and emerging systems; impact on chip design
- Variation-aware design
    - Sources of variation
    - Circuit performance (timing and power) shifts due to variations
    - Layout-dependent variations due to process, stress, etc.
    - Aging and reliability
    - Environmental variations due to temperature and voltage drops
    - The impact of subwavelength lithography on design
- Design automation issues associated with emerging computing paradigms, such as imprecise computation, logic-in-memory systems, and neuromorphic systems

Textbook
None. Since the topics covered in the class are in areas of active research, much of the material will be extracted from conference and journal publications. Accordingly, students can expect a significant reading workload.

Grading
Evaluation mechanisms will include individual explorations and group work (30%), a take-home midterm exam (20%), and a term project (50%). It is expected that in most (if not all) cases, the term project will involve a computer programming component.