

Exploration of Design / Layout Tradeoffs for RF Circuits using ALIGN

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Abstract— The extended manual layout process for RF and analog/mixed-signal design restricts design space exploration and limits design productivity. This work demonstrates the efficacy of an automated layout generator versus a manual approach using a state-of-the-art MIMO receiver. Multiple smaller floorplans of the layout are generated automatically in hours compared to weeks for a single manual layout. Measured results from an automatically generated layout fabricated in TSMC 65nm CMOS show performance numbers comparable to the manual design. Measured in-band/in-notch IIP_3 and out-of-band/in-notch IIP_3 are 18.3dBm and 23.64dBm, respectively.

Keywords— Automated RF-AMS layout synthesis, Design space exploration, Design productivity, MIMO receiver

I. INTRODUCTION

RF/analog/mixed-signal (RF-AMS) circuits require careful design to avoid expensive respins and failures in the field. To build robust, high-performance RF-AMS blocks, it is desirable to evaluate a number of design options. However, conventional design methods are mostly manual, time-consuming and do not allow the designer to fully explore the design space. A typical RF-AMS design flow involves: (a) architecture design, (b) sub-block design, (c) device sizing, (d) layout, typically done manually, (e) final verification with post-layout parasitics. In particular, for RF circuits the layout step is a critical determinant of circuit performance. During design iterations, devices may be resized in step (c) based on post-layout parasitics, but such sizing operations perturb the layout, leading to further changes in the parasitics, leading to long iterations between steps (c)–(e) till the design specifications are met. The layout step (d) is a tedious manual process, requiring expert human layout/mask designers. Advanced process technologies involve complex design rule checks (DRCs), which further slow the layout process. Typical design/layout iterations run into multiple weeks, limiting the number of designs that can be evaluated before tape-out. To reduce the design/layout iterations, designers resort to conservative parasitic estimates, resulting in designs with sub-optimal power and/or performance [1].

An automated RF-AMS layout synthesis flow can be useful to a designer as it addresses the critical bottleneck of long layout times while simultaneously handling complex DRCs. An automated tool can help explore the design space by generating multiple designs/layouts in the same amount of time it takes for a single manual layout. There have been multiple recent open-source approaches to achieve this goal including [2]–[4], and ALIGN [5]. In this work, we compare the efficacy of automatic layout generation using ALIGN versus a manual layout for a state-of-the-art MIMO receiver [6]. Multiple automated layouts are generated simultaneously, all of which satisfy the required layout

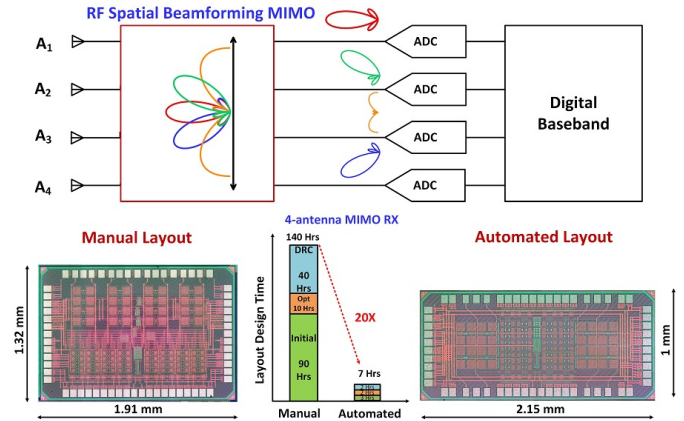


Fig. 1. MIMO design used to illustrate the process. Chip micrographs for manual and automatic layouts and productivity improvement using the tools.

constraints such as symmetry, ordering, common-centroid and matching. With rapid layout synthesis, ALIGN quickly estimates parasitics during the design phase, reducing the number of design/layout iterations. The designer’s intent for a floorplan can be specified in ALIGN in the form of user-defined constraints provided to the layout generator [7]. The layout is generated hierarchically and the designer can pick the best-performing layout for each hierarchy using post-layout extracted simulations. Fig. 1 shows the manual and automated layouts (microphotos) of the MIMO RX and shows a measure of how design productivity is enhanced by the latter. The manual approach took weeks for a single layout, as against a few hours required by the automated process to generate multiple complete chip-level MIMO layouts.

We describe the ALIGN flow in Section II. Section III overviews the MIMO design and compares a manual layout against multiple automated layouts. One of the automated layouts was fabricated and tested. Section IV compares its measured performance against the fabricated manual design. Section V discusses the productivity gain from automation and Section VI concludes the paper.

II. DESIGN FLOW

An overview of the steps involved in the ALIGN flow is shown in Fig. 2. At the very basic level, the input can be a netlist and the output is a hierarchical layout in GDSII format. There are four major steps which are briefly described: (a) Constraint generation identifies known sub-circuits in the netlist and layout constraints such as symmetry, common-centroid, ordering, and matching. ALIGN uses graph convolutional network (GCN) to identify hierarchies like OTA, LNA, etc. The designer may examine these identified hierarchies and constraints and augment them

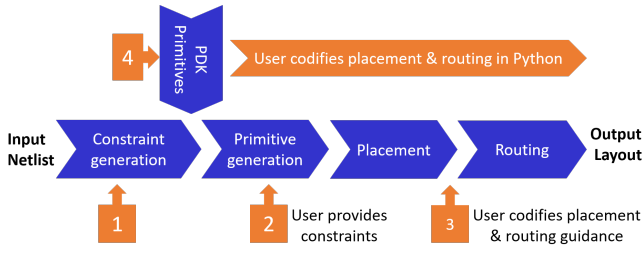


Fig. 2. Overview of the ALIGN flow.

to reflect designer intent. Primitives are one or more devices that are typically laid out as a single layout entity such as resistors, capacitors, current mirrors, and differential pairs. (b) The second step generates layouts for each of the primitives in the first step. (c) The third step assembles these primitive layouts into a legal layout that meets layout constraints. (d) The last step is routing which connects various nets with wires of appropriate widths. This step also generates power grids for the supply/ground nets and connects them to the devices. Apart from the auto-generated constraints in the first step, users can input placement constraints such as maximum width/height, aspect ratio, and spacing between any pair of blocks, and routing constraints such as shielding for critical nets, clock nets, and matched routing for symmetric nets. As shown in Fig. 2, the user can intervene in the ALIGN flow at multiple points and add/delete constraints within the flow. There is also support to code the entire placement and routing using relative positions of blocks. To ensure that the layouts generated are compatible with foundry-specified PDKs, an abstract set of rules are honoured by all the layout generators. These rules are chosen to be broad enough to work for all tested foundries with minimal changes to the flow. The arithmetic values for the layout rules change for different foundries and technologies.

Black-box methodology: Designers can reuse layouts of sub-circuits whose performance is verified either in silicon or via simulation. ALIGN supports the inclusion of such layouts through a black box methodology. In this methodology, the user-input layouts are abstracted into the library exchange format (LEF) with defined pins, ports and obstacles. The abstraction step is automated for the input layouts in GDSII format. These layouts are instantiated in the placement step and appropriate connections are made during routing.

Engineering change order (ECO): Design/layout iterations are performed to subsume the impact of layout parasitics. In each iteration, the layout is perturbed due to one of the following: alteration of device sizes, the spacing between devices, or inclusion of new placement/routing constraints. Depending on the hierarchy at which such a change is made, the impact on the layout could be localized or span the entire design. ALIGN handles such a change using an ECO methodology. As an example, we may add space between blocks to reduce coupling, which could perturb the corresponding hierarchy, its parents and neighbours. ALIGN automatically identifies such a perturbation and rapidly performs incremental placement and routing on those blocks.

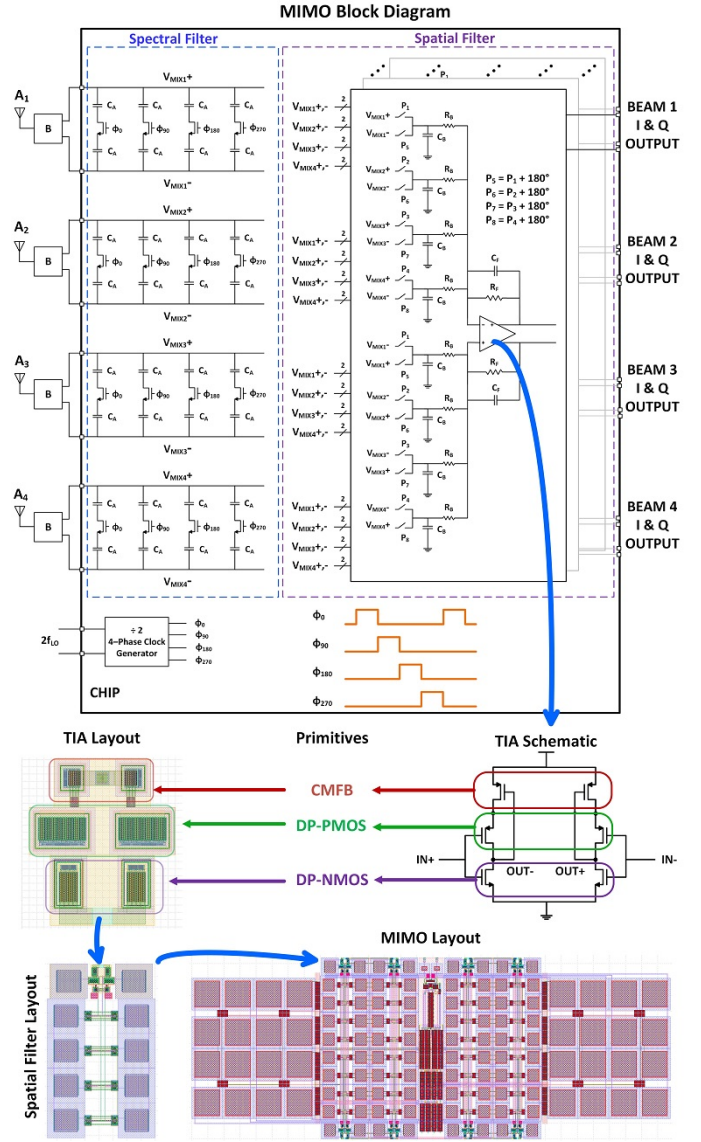


Fig. 3. Auto-annotation and hierarchical layout generation of the spatial filter.

III. MIMO

Fig. 3 shows the MIMO architecture with four spectral filters, eight spatial filters and the clock generation block. The spectral filter consists of a differential bottom-plate mixer architecture for improved IIP_3 . The spatial filter consists of a differential summing amplifier with capacitor C_B acting as the voltage source. Spatial beamforming is performed by combining different antenna inputs with phase shifts. Fig. 3 shows some blocks recognized by ALIGN: the transimpedance amplifier (TIA) with common primitives such as common mode feedback (CMFB) transistor pairs, differential NMOS and PMOS pairs. After identifying these primitives associated with the amplifier, ALIGN automatically creates a symmetrical layout based on the device sizes. Internal routing widths can be user-defined, based on performance needs.

Fig. 4 compares various MIMO layouts generated using ALIGN with the aforementioned placement and routing constraints against a manual layout. For a fair comparison

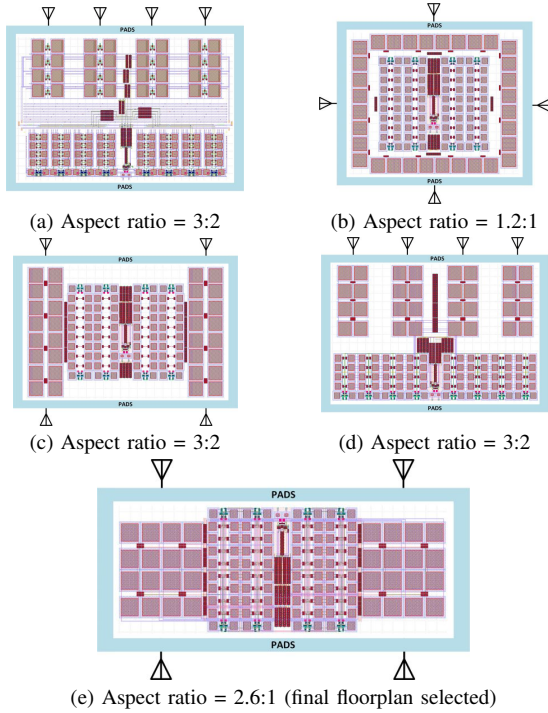


Fig. 4. Various MIMO layouts (a) Manual layout, (b) and (c) automatically generated layouts, (d) ALIGN mimicking manual layout through constraints, and (e) ALIGN layout with user-specified maximum height constraint.

between manual and ALIGN-generated layouts, the layouts of primitive cells such as MIM capacitors and special RF transistors used in the manual layout were reused in ALIGN layouts using the black-box methodology. Fig. 4(a) shows the manual layout and Fig. 4(b) and (c) show two ALIGN-generated layouts with just the clock net constraint. The layout in Fig. 4(b) is the most compact of all variants, and its square aspect ratio of the layout makes it easy to match routing parasitics using an H-tree structure.

In each iteration, simulations with post-layout extracted parasitics were used to identify the performance-critical nets and blocks. The following changes were made in successive iterations based on the simulations: (a) improving the resistance of critical nets by widening wires using the net-specific routing width constraint, (b) reducing coupling by (i) increasing the spacing between blocks, and (ii) adding shielding between adjacent signal nets. These changes involved perturbation to both placement and routing and were implemented automatically using the ECO mode described in Section II. The entire placement and routing in ECO mode took only tens of minutes in each iteration. Fig. 4(d) shows the layout generated by ALIGN mimicking the manual layout. This ALIGN layout was achieved by manually specifying constraints for all the hierarchies. An external limitation on the die size constrained the maximum height of the MIMO layout to be $600\mu\text{m}$ which when input to ALIGN generated the layout in Fig. 4(e). This layout was selected for the tapeout.

IV. MEASUREMENT

A prototype of a four antenna MIMO system was implemented in TSMC's 65nm CMOS process. The die photo

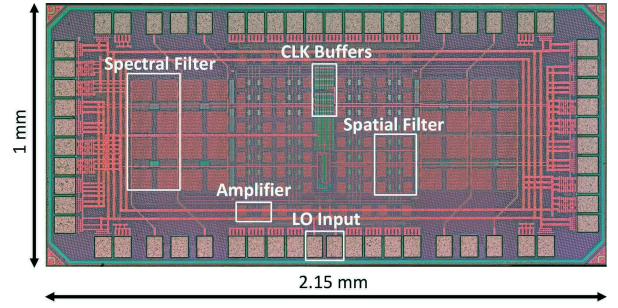


Fig. 5. Die Photo

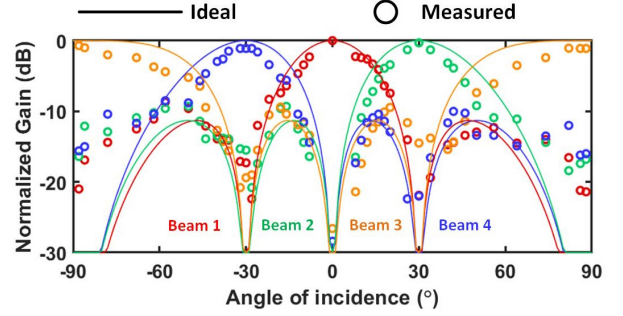


Fig. 6. Spatial gain across four beams.

is shown in Fig. 5. The dies were wire bonded to a 60-pin QFN and then mounted on a two-layer PCB. Four BALUNs were placed on the PCB to create differential RF signals.

Spatial Gain: For gain measurement, the RF output from a signal generator is split into four via a power divider. These four outputs are then passed through different PCB traces to create different phase shifts for a beam. The spatial gain for all four beams were measured from 1GHz to 2.5GHz and exploits the phase versus delay relationship. Fig. 6 shows the spatial gain for all four beams. A maximum spatial suppression of 28.4dB was measured between the broadside (Beam 1) beam and $+30^\circ$ (Beam 4) beam at 0° angle of incidence.

Gain and Bandwidth: Fig. 7 shows the measured gain of four output beams (Beam 1-Beam 4) for a broadside input beam at 1GHz. The measured low frequency gain and 3dB bandwidth for output Beam1 were 13dB and 30MHz respectively. As seen, we observe additional parasitic poles around 80MHz IF. The gain was measured for operating range of 1–2.5GHz. The measured gain of 13dB dropped after 2.3GHz. Hence, the measured operating range for this design is 1–2.3GHz.

IIP_3 and B_{1dB} : Figure 8 shows the measured IIP_3 and

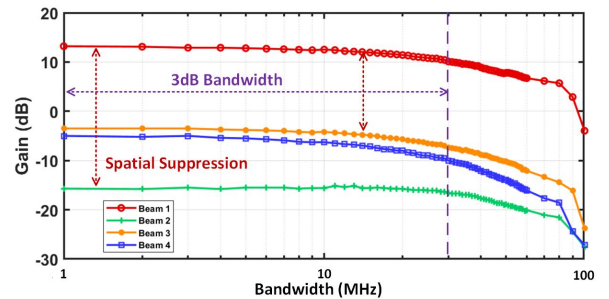


Fig. 7. Measured gain versus IF bandwidth for all four beams.

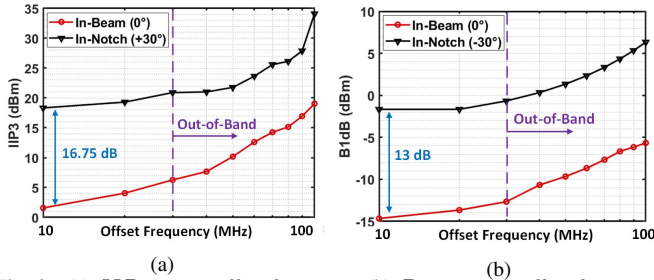


Fig. 8. (a) IIP_3 versus offset frequency. (b) B_{1dB} versus offset frequency.

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Technology	65nm CMOS	65nm CMOS
Layout type	Manual	Automated
Operating frequency range (GHz)	1-3	1-2.3
Single element conversion gain (dB)	15	13
Max spatial suppression (dB)	27	28.4
In-band/In-beam OIP_3 (dBm)	17.4	14.6
Out-of-band/In-beam IIP_3 (dBm)	18.8 $\Delta f/BW=4.6$	19.3 $\Delta f/BW=4.6$
In-band/In-notch IIP_3 (dBm)	17.8	18.3
Out-of-band/In-notch IIP_3 (dBm)	19.3 $\Delta f/BW=2$	23.64 $\Delta f/BW=2$
In-band/In-beam B_{1dB} (dBm)	-11.97	-14.66
In-band/In-notch B_{1dB} (dBm)	1	-1.66
Area (sq.mm)	2.53	2.15
Power (mW)	130-242	130-175

Table 1. Measured performance comparison for manual vs ALIGN layouts.

B_{1dB} values for different offset frequencies. The two-tones in the IIP_3 measurement were kept at broadside. Thus, in-beam IIP_3 measurement were taken at Beam 1 (0°) beam and in-notch IIP_3 measurement were taken at Beam 2 ($+30^\circ$) beam. The measured in-band/in-beam IIP_3 and in-band/in-notch IIP_3 at 10MHz offset were 1.58dBm and 18.33dBm respectively. In the B_{1dB} measurement, the signal was kept at 0° angle and blocker was kept at either 0° angle (in-beam case) or -30° angle (in-notch case). The measured in-band/in-beam B_{1dB} and in-band/in-notch B_{1dB} at 10MHz offset were -14.66dBm and -1.66dBm respectively.

Performance Comparison: A comparison of the measured performance for the manual and automated layouts is shown in Table 1. The performance parameters of the manual layout [6] has been included with a loss calibration of 5dB. As can be seen, spatial suppression, IIP_3 and B_{1dB} of the automated layout are close to/exceeds manual layout's performance except for RF frequency range. We suspect this is because all the clock buffers were placed in the center for the automated placement, resulting in an operating frequency of 1-2.3GHz as opposed to manual layout's 1-3GHz range. This parameter can be improved with few additional iterations in ALIGN.

V. PRODUCTIVITY IMPROVEMENT

Fig. 9 compares the time required to generate the layout of a MIMO receiver using manual and automated approaches. FP 1 and FP 2 correspond to the floorplans shown in Fig. 4(b) and (e) respectively. FP 2.1 refers to the default layout generated by ALIGN with the maximum height constraint of $600\mu\text{m}$. Post-layout extracted simulations on this layout identified critical nets whose resistance needed to be improved. Resistance parasitics were improved using net-specific routing

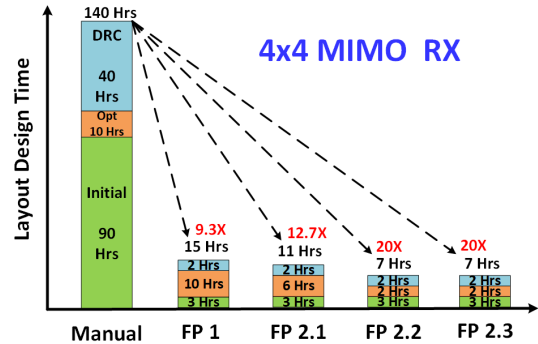


Fig. 9. Productivity gain: manual vs automated layout (four iterations)

width constraints and ECO mode described in Section II was used to realize these constraints. Simulations based on this layout identified nets whose coupling capacitance needed improvement. Using this feedback, shielding and increased spacing constraints were added and a second iteration of ECO was used to arrive at the final layout. As seen in Fig. 9, each of the iterations took hours to generate the layout and cleanup DRCs against the manual approach that took days for a single layout. The resultant automated layout has a similar performance to the manual layout as shown in Section IV. The productivity gain chart shows that within the same amount of time spent in generating a single manual layout, multiple automated layouts can be explored. As demonstrated, each layout can also be iteratively improved in a short time using performance evaluated with post-layout simulations.

VI. CONCLUSION

The efficacy of an automated RF-AMS layout synthesis flow has been demonstrated using productivity improvement on a state-of-the-art MIMO design. The layout is iteratively improved using an ECO mode with feedback from post-layout simulations. The automated flow generates a layout with performance similar to the manual layout with an order of magnitude smaller overall time. The time saved helps explore the design space and other architectures for the same design.

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