Reliability analysis of a Delay-Locked Loop under HCI and BTI Degradation

Tonmoy Dhar and Sachin S. Sapatnekar
Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN, 55455, USA.

Introduction Analog/mixed-signal (AMS) have become increasingly important performance-critical components of larger integrated systems, and they are highly susceptible to aging-induced variation. Systematic analysis of AMS components is imperative, and should address AMS-specific features such as the prevalence of feedback loops, the impact of bias conditions, and sensitivity to reactive components. Prior efforts have studied standalone analog blocks [1], low noise amplifiers (LNAs) [2], LC oscillators/phase-locked loops [3], and current-starved voltage-controlled delay lines [4], and does not clearly separate the impact of bias temperature instability (BTI) and hot-carrier injection (HCI). We explore aging in the AMS components in circuits for clock/data recovery, clock generation, frequency synthesis, and signal synchronization.

A DLL delays an input signal $S_{ref}$ by a clock cycle, $T_{clk}$, to produce an aligned output signal $S_0$. It consists of (Fig. 1(a)):
- a phase detector (PD) that compares $S_0$ with $S_{ref}$, and outputs $U_p$ and $D_n$ that indicate the phase relation.
- a charge pump (CP), which uses $U_p$ and $D_n$ to generate voltage $V_{control}$ and drives a capacitive loop filter (LF).
- a voltage controlled delay line (VCDL) whose delay is adjusted, depending on the value of $V_{control}$.

Impact of aging Aging degrades DLL precision over time by increasing the misalignment between $S_{ref}$ and $S_0$ at steady state, eventually rendering the DLL inoperable. We investigate the effect of aging on the DLL at two levels of hierarchy: first, individually on each component of the DLL, and then on the entire DLL. For the simulation results included in the abstract, we use a dynamic BTI model [5] and an energy-driven HCI framework [6], under 45nm NCSU MOSFET models and an $S_{ref}$ clock period. $T_{clk}=1$ns. We will also include analyses for finFET based DLL design in the full-length paper.

Phase detector (Fig. 1(b)) The key timing parameters for the PD are: (1) propagation delay, $T_{delay}$, between the later of the rising edge of $S_0$ or $S_{ref}$, and the falling edge of Reset pulse width $\Delta R$ of the Reset signal. These two parameters place an upper bound on the allowable frequency of $S_{ref}$, which degrades with time as aging increases gate delays. Our simulations show that the reset operation is 42.6% slower after 10 years (Fig. 2(a)), slowing down the DLL response.

Recall that the phase difference between $S_0$ and $S_{ref}$ should settle to $T_{clk}$, but may have a discrepancy, $\Delta P$. The relative pulse widths, $PW$, of the $U_p$ and $D_n$ signals indicate whether $\Delta P > 0$ or $< 0$, and activate feedback action. When $\Delta P > 0$, ideally $PW_{D_n} > PW_{U_p}$, but as PW changes under aging-related slowdowns, the circuit can incorrectly set $PW_{D_n} \leq PW_{U_p}$. At this stage the PD is no longer responsive to $\Delta P$.

Charge pump (Fig. 1(c)) Considering identical inputs ($U_p$ and $D_n$) and $I_{CP}$ of 10$\mu$A, the simulation shows a significant mismatch, of 73% over 10 years, induced between $T_{4,CP}$ and $T_{5,CP}$, due to asymmetric HCI aging (Fig. 3(a)). Transistor aging is accelerated with increasing $I_{CP}$ (Fig. 3(b)) and can be slowed down with increasing transistor widths (Fig. 3(c)). Although, $V_{control}$ should have been steady if $U_p$ and $D_n$ signals are identical, transistor aging causes $V_{control}$ to decrease with time as illustrated in Fig. 3(d).

VCDL (Fig. 1(d)) Fig. 4(a) compares the degradation $\Delta V_{th}$ of each transistor of a shunt capacitor inverter with an identical inverter without the tunable load, $T_{4,\text{VCDL}}$, which indicates NMOS transistor of the VCDL, $T_{2,\text{VCDL}}$, faces 157% higher degradation compared to the NMOS of the inverter without load, $T_{2,\text{Inverter}}$. Fig. 4(b) compares $\Delta V_{th}$ at the minimum (0V) and maximum (1V) value of $V_{control}$. To achieve a designated delay with reference to an edge in $S_{ref}$, the VCDL must be within a specified delay band. If $S_{ref}$ has a period of $T_{clk}$, then the VCDL must maintain the following constraints to stably create the one-cycle phase difference:
\[ 0.5T_{clk} < D_{min} < T_{clk} ; T_{clk} < D_{max} < 1.5T_{clk} \] (1)
where $D_{min}$ ($D_{max}$) is the delay under the minimum [maximum] $V_{control}$. Under transistor aging (Fig. 4(c)):
- $D_{min}$ and $D_{max}$ rise by ~100% in 5 years, violating (1).
- Intermediate stages of the VCDL are unable to fully transition (Fig. 4(d)) which may render the VCDL inoperable.

Unlike the CP, aging-induced $\Delta V_{th}$ in the VCDL cannot be reduced by transistor sizing. A higher width for $T_{1,\text{VCDL}}$ and $T_{2,\text{VCDL}}$ will require higher widths for $T_{3,\text{VCDL}}$ and $T_{4,\text{VCDL}}$ to satisfy (1). The inverter transistors thus must drive higher currents, inducing more HCI aging. As a result, the optimal transistor size remains virtually unchanged (Fig. 5).

DLL-level impact Figs. 6 – 8 present the impact of the aforementioned block-level variations to the DLL level. The increase of $PW_{U_p}$ and $PW_{D_n}$ with transistor aging causes the misalignment between $S_{ref}$ and $S_0$ to increase with time in the steady state (Fig. 6(a),(b)). This misalignment also causes mismatch between the transistors $T_{0,CP}$ and $T_{1,CP}$ (Fig. 7(a)). Aging-induced mismatch between $T_{5,CP}$ and $T_{4,CP}$ causes current through $T_{0,CP}$ and $T_{1,CP}$ to increase with time. This reduces the acquisition time of the DLL (Fig. 7(b)).

Fig. 8 illustrates how aging in the PD and VCDL can render the DLL inoperable. Without aging, for a new $S_0$, a lag of $T_{clk}$ w.r.t. $S_{ref}$ is created within ~ 30 cycles, setting $\Delta P$ to 0. Aging in the PD and VCDL can induce functional failures: PD-induced DLL failure: As stated earlier, PD aging can make the $PW$ of its outputs unresponsive to $\Delta P$; the DLL then fails to alter $S_0$ to bring $\Delta P$ to zero (red curve in Fig. 8).

VCDL-induced DLL failure: As aging shifts $D_{min}$ and $D_{max}$, if $D_{min}$ goes above $T_{clk}$, then constraint (1) is violated, and the DLL fails to bring $\Delta P$ to 0 (orange curve in Fig. 8).

We will provide further details in the full paper.
Fig. 1. (a) Block diagrams of: (a) DLL, (b) PD, (c) CP, and (d) VCDL.

Fig. 2. Effects of aging on $T_{\text{delay}}$ and $\Delta R$ of the PD.

Fig. 3. (a) $V_{th}$ degradation of CP transistors due to aging; (b) Transistor aging trends with (b) current, $I_{CP}$; (c) transistor width; and (d) $V_{\text{control}}$ under aging.

Fig. 4. (a) $\Delta V_{th}$ of transistors in Fig. 1(d) after aging. (b) Comparison of $\Delta V_{th}$ at minimum and maximum $V_{\text{control}}$. (c) Change in delay range of VCDL with aging. (d) Failure in VCDL operation due to aging.

Fig. 5. $\Delta V_{th}$ for various VCDL transistor sizes after 10 years.

Fig. 6. (a) Transients of DLL operation without aging. (b) Phase difference between $S_{\text{ref}}$ and $S_0$ after alignment with aging.

Fig. 7. (a) Mismatch induced by DLL operation between $T_{0,CP}$ and $T_{1,CP}$. (b) Change of $T_{\text{acquisition}}$ due to transistor aging.

Fig. 8. Change of $\Delta P$ without aging, and under PD and VCDL aging.

REFERENCES


