Circuit Reliability: From Physics to Architectures

Embedded Tutorial Paper

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Abstract: In the period of extreme CMOS scaling, reliability issues are becoming a critical problem. These problems include issues related to device reliability, in the form of bias temperature instability, hot carrier injection, time-dependent dielectric breakdown of gate oxides, as well as interconnect reliability concerns such as electromigration and TSV stress in 3D integrated circuits. This tutorial surveys these effects, and discusses methods for mitigating them at all levels of design.

Keywords

Bias temperature instability, hot carriers, oxide breakdown, electromigration, 3D ICs, stress.

1. Introduction

Variational effects are increasingly important in nanometer-scale technologies. Prior research has greatly focused on process variations, which cause individual parts to show significant performance variations "at birth." For deeply-scaled technology nodes, however, the impact of aging, which causes temporal variations in the behavior of a circuit over its lifetime, are gaining prominence and must be compensated for during design. This presentation surveys methods for analyzing and optimizing reliability effects and provides a bibliography of source material.

Temporal variations can affect both devices and interconnects. The classical bathtub curve [1] pictorially explains the effect of temporal variations: after a steep initial failure rate, the number of failures levels off for a while before rising again. Process variations form a special case on this curve, corresponding to the static variations baked into the chip at time zero, while aging variations are represented on the rest of the curve. Many of these variations have strong sensitivity to the on-chip temperature.

The paper is organized as follows. In Sections 2 and 3, we will overview temporal variations due to device-level effects and interconnect-level effects, respectively. Our discussion focuses on aging effects and transient errors such as soft errors are not considered here. In Section 4, we will outline and classify methods for optimizing temporal aging effects.

2. Device failure physics and models

2.1 Bias temperature instability

Bias temperature instability (BTI) is a phenomenon that causes threshold voltage shifts over long periods of time, eventually causing the circuit to fail to meet its specifications. The word "bias" refers to the fact that this degradation is heightened by the application of a bias on the gate node of a transistor, and this degradation is sensitive to the temperature. A PMOS transistor in an inverter experiences negative BTI stress when its gate node is at logic 0, and the resulting increase in the threshold voltage is partially reversed when the voltage stress is removed (i.e., a logic 1 is applied). A similar phenomenon of positive BTI affects the threshold voltage of NMOS devices when they are stressed, and relaxes the degradation on the removal of stress. The magnitude of degradation depends on the ratio of the stressed time to unstressed time, i.e., the signal probability (SP) of the gate input.

There are two widely-accepted theories for BTI, both of which partially explain the phenomenon. The *reaction-diffusion* (R-D) model [2]–[8] explains the degradation due to the accumulation of positive charges as Si-H bonds at the interface are broken and hydrogen diffuses away; the removal of this stress allows partial restoration of these bonds. Over the years, several limitations to this theory have been discovered. For instance, unlike the predictions from R-D theory, measured degradations are sensitive to the applied gate bias, and the recovery begins faster and lasts longer than predictions from the R-D model. The *charge trapping* (CT) model [9]–[12] provides an alternative explanation, where defects in gate dielectrics can capture charged carriers, causing the threshold voltage to degrade; however, it also predicts asymptotically complete recovery when stress is removed, inconsistent with experiments. It has been posited that R-D and CT mechanisms coexist, and a superposition of both matches experimental data [13]. The CT model predicts high variability in small devices [9], making variability a major factor for memories. For logic circuits, however, large transistors and averaging effects on critical paths significantly mitigate variability [14].

2.2 Hot carrier injection

Hot carrier injection (HCI) effects in MOSFETs are caused by the acceleration of carriers (electrons/holes) under lateral electric fields in the channel, to the point where they gain enough energy and momentum to cause damage, degrading mobilities and threshold voltages [15]. Hot carrier effects cumulatively build up over prolonged periods, causing the circuit to age, resulting in irreversible degradations that may lead to circuit failure.

The traditional theory of HCI mechanisms was based on a field-driven model where the peak energy of carriers was determined by the lateral field of the channel, based on the theory of the so-called lucky electron model [16]. Extrapolating this model, it was expected that at today's supply voltages, HC effects would almost disappear as carriers cannot gain enough energy when the electric field is at today's levels. However, experimental evidence on nanometer-scale technologies shows that this is not true, and hot carrier degradation remains significant for MOSFETs at lower voltages, and is projected to worsen in future. Recently, newer energy-driven theories [17]–[19] have been introduced to generalize the ideas of the lucky electron model, and to explain the mechanism of carrier-induced degradation for short-channel devices at low supply voltages. These theories have been experimentally validated on nanometer-scale technologies. The energy-driven framework includes the effects of electrons of various energies, from high-energy channel hot carriers (CHCs) to

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low-energy channel cold carriers (CCCs). However, much circuit-level work on HCI is based on the lucky electron model.

For large-scale circuit analysis, some scalable approaches for timing analysis under HC effects have been developed. One approach [20] applies a duty factor to capture the effective stress time for HC effects, which assumes constant HC stress during signal transitions and models the duty factor to be proportional to the transition time, and also simultaneously incorporates BTI effects. Another method [21] uses the new energy-driven theories described above, and defines an age gain per transition using quasistatic characterization. Using abstractions based on the signal probability (SP) and transition density (TD), this is used to build a methodology for timing analysis of large-scale circuits.

The HCI rate increases as $t^{1/2}$, where t is the time variable. Since the multiplicative constant is relatively small, in the short term, HCI is overshadowed by BTI effects, which vary as t^n, for $n \approx 0.1–0.2$, but with a larger constant multiplier.

2.3 Time-dependent dielectric breakdown

Time-dependent dielectric breakdown (TDDB) in gate oxides is an irreversible reliability phenomenon that results in a sudden discontinuous increase in the conductance of the gate oxide at the point of breakdown, as a result of which the current through the gate insulator increases significantly. This is of concern as gate oxide thicknesses become thinner with technology scaling, and gates become more susceptible to breakdown.

Various TDDB models have been proposed, e.g., the hydrogen model, the anode-hole injection model, the thermochemical model (also known as the *E* model), and the percolation model [22,23]. The time to breakdown can be modeled statistically using a Weibull distribution [22,24]. Circuit-level analysis approaches for TDDB are limited. Memory effects have been addressed in [25]. For logic circuits, a conventional area-scaling based method is presented in [26]. However, that logic circuits are inherent resilient to variation [27,28], and the area-scaling model is pessimistic by about half an order of magnitude.

3. Interconnect failure mechanisms

3.1 Electromigration

When a current flows through an on-chip wire over a long period of time, it can cause a physical migration of atoms in the wire, particularly if the current density is high. The current conducting electrons can form an *electron wind*, which leads to momentum exchange with the constituent atoms of metal. This effect will lead to a net flux of metal atoms in the direction of electron flow (opposite of current direction), creating voids (depletion of material) upstream and hillocks (accumulation of material) downstream at locations of atomic flux divergence. Electromigration can cause uneven redistribution of resistance, dielectric cracking, and undesired open circuits.

Electromigration is witnessed most notably in supply (power and ground) wires [29,30], where the flow of current is mostly unidirectional, but AC electromigration is also seen in signal wires [31,32]. More recent models capture reverse stresses due to Blech effects [33]–[35], and move beyond aluminum interconnect models to address copper-specific issues [36,37].

3.2 Thermomechanical stress in 3D ICs

Thermomechanical reliability effects arise due to significant thermal effects that can cause mechanical stress. For example, through-silicon vias (TSVs) in three-dimensional integrated circuits (3D ICs), which connect different wafers/dies in the stack, are subject to stress, and affect within-silicon stress.

In manufacturing, the TSV and silicon wafer undergo thermal cycles before a final annealing step that embeds the TSV in the wafer. During annealing and cooling, the structure is subjected to a thermal ramp from 250°C down to 25°C, i.e., room temperature [38]. Because of the difference in the coefficient of thermal expansion (CTE) of the copper TSV and the silicon, a residual thermal stress is induced in the region surrounding the TSV [38]–[40]. This thermally-induced stress may affect the reliability of the TSV, making it susceptible to fatigue. Moreover, the timing behavior of the circuit may be affected as transistors are stressed. According to piezoresistivity theory [41], stress affects the electrical conductivity of devices and hence the mobility of the transistors. The amount of the mobility variation depends upon the stress levels, which is determined by the position and channel orientation of a transistor with respect to the TSV and crystallographic axis, respectively. Several approaches have been presented for timing analysis under thermomechanical stress [42]–[45], and for stress analysis of TSVs to determine their susceptibility to electromigration faults and to cracks [46,47].

4. Circuit Optimization

Circuit-level research on reliability optimization has primarily addressed BTI, with limited work on other device-level effects [27]; these have been addressed using older, traditional models by architects. Today's EM optimization strategies primarily operate by limiting the current density on a wire to a specified threshold through, for example, wire widening in the power grid, but do not address newer models directly. Our discussion below focuses largely on BTI, the effect that has been studied most.

BTI optimization techniques can largely be classified into a few categories. *First*, there are methods that attempt to rebalance the signal probabilities in a circuit to even out the wearout on pull-up and pull-down paths in a circuit: such methods have been applied to memory [48], logic [49], and at the processor level [50]. An alternative approach temporarily deactivates memory units on a rotating basis to allow for recovery from wearout [51].

The GNOMO approach [52] leverages BTI recovery, and uses a greater-than-nominal supply voltage to reduce aging. The key observation is that at a higher supply voltage, a computation completes faster. To maintain iso-performance with the nominal supply voltage, a GNOMO circuit is periodically put to sleep. This allows for BTI recovery and reduces aging. Power savings are achieved through inactivity during the sleep period and from reduced delay margining overheads under this reduced aging.

A *second* class of methods applies static presilicon [53] or adaptive postsilicon techniques to pad the circuit against BTI degradation. Published methods based on adaptive margins have used time sensors [54], history sensors that track usage patterns [55], or surrogate sensor circuits. Optimization knobs include changing the supply voltages [56], body biases, or both [54], using using dynamic cooling [55], and through redundancy and disposable cores [57]. At the architecture level, the concept of dynamic reliability management [58] has been incorporated into the notion of reliability banking in [59]. Adaptive sense/respond mechanisms require sensing capabilities: related work includes "silicon odometers" and similar sensors to capture BTI, but also HCI and TDDB [60]–[63]. Online test techniques for analyzing failures are proposed in [64]–[66]. Other ideas include introspective sensor-based methods for reducing aging have been [67], intelligent power gating [68]–[70], and scheduling [71].

Third, some approaches have suggested the use of setting up specific sleep states that are designed to minimize BTI

degradation through input vector control [72,73]: however, the gains of such methods are relatively small. A related method introduces NOPs between instructions to reduce aging [74].

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