# A Charge Flow Formulation for Guiding Analog/Mixed-Signal Placement

Tonmoy Dhar[1], Ramprasath S.[1], Jitesh Poojary[1], Soner Yaldiz[2],
Steven Burns[2], Ramesh Harjani[1], Sachin S. Sapatnekar[1]
[1]University of Minnesota, Minneapolis, MN [2]Intel Corporation, Hillsboro, OR

***Abstract*—An analog/mixed-signal designer typically performs circuit optimization, involving intensive SPICE simulations, on a schematic netlist and then sends the optimized netlist to layout. During the layout phase, it is vital to maintain symmetry requirements to avoid performance degradation due to mismatch: these constraints are usually specified using user input or by invoking an external tool. Moreover, to achieve high performance, the layout must avoid large interconnect parasitics on critical nets. Prior works that optimize parasitics during placement work with coarse metrics such as the half-perimeter wire length, but these metrics do not appropriately emphasize performance-critical nets. The novel charge flow (CF) formulation in this work addresses both symmetry detection and parasitic optimization. By leveraging schematic-level simulations, which are available "for free" from the circuit optimization step, the approach (a) alters the objective function to emphasize the reduction of parasitics on performance-critical nets, and (b) identifies symmetric elements/element groups. The effectiveness of the CF-based approach is demonstrated on a variety of circuits within a stochastic placement engine.**

## I. Introduction

The placement problem for analog/mixed signal (AMS) circuits optimizes objectives such as area and wire parasitics, with constraints on circuit performance, as well as symmetry/matching constraints to mitigate variability. Issues in modeling the objective and constraint functions include the following:

- In the *objective* function, the half-perimeter wirelength (HPWL) metric, i.e., the semiperimeter of the bounding box of all pins, is widely used to represent interconnect parasitics, but this metric incorrectly treats all nets as equally important.
- The evaluation of *performance constraint* functions requires circuit simulation, which is prohibitive within the inner loop of a placement engine. Such constraints are handled by assigning *ad hoc* weights or penalties to net parasitics in the objective function. For example, important nets are marked based on signal flow analysis [1], [2] or designer annotation, but it is nontrivial to use this information to automatically quantify the relative criticality of nets. Recent machine learning (ML) based methods [3]–[5] can capture the complex relationships among net parasitics and performance metrics, but require a large training set that is onerous to generate, and do not generalize across circuits: each circuit has different performance metrics, and separate ML models must be trained for each circuit type.
- The evaluation of *symmetry constraints* is typically supported by an expert designer who manually identifies the constraints, or a tool that automatically extracts the constraints either from the sensitivity [6] or topological [7], [8] analysis of the circuit.

This work develops a **charge flow (CF)** formulation for AMS circuit placement. We leverage information available in a typical design flow, where a netlist designer first optimizes the circuit structure and transistor sizes through extensive SPICE simulations, and then hands off the circuit to layout design. During this process, data about current flows in various nets of the design is available "for free" from the simulations at the netlist design stage. These currents provide a good deal of information about net criticality and even symmetry, and can be leveraged by placement tools. For example, interconnect parasitics on nets between pin-pairs with higher currents tend to have higher impact in resistance-dominated FinFET technologies due to larger IR drops along these signal wires, which could potentially change biasing conditions or limit voltage headroom. Moreover, nets with high current densities must use wider/parallel wires to satisfy electromigration (EM) constraints: keeping these nets short results in better use of routing resources. In addition, current symmetries can be used to identify layout symmetries, e.g., in differential circuits, the current transients of symmetric elements mirror each other.

We use these principles to build a CF-based methodology. Note that the CF metric draws on core circuit principles, hence it can be *generically applied* to any AMS circuit, and is not restricted to any specific functionality or topology. Given the simulation data, the procedure for generating CF metrics involves very low additional computational overhead. The results of this method can easily be incorporated in a stochastic placer, and this paper demonstrates the scheme within an existing analog layout synthesis tool.

## II. Current paths and Limitations of Monotonicity

We explore the notion of a *current path*, defined as a chain of drain- and source-connected transistors starting from the supply net and ending at the ground net. The concept was used in [1] to address critical nets during placement and a sequential placement method was proposed where all transistors on a current path are placed in a row, from left to right, but a single row for each path may not be optimal. The idea of current path monotonicity is used in [9]–[11], but this has limitations, as illustrated later in this section.

Consider the fully-differential folded-cascode (FC) OTA in Fig. 1. We highlight current paths $C_1$–$C_4$ in the figure. For placement purposes, we group together symmetric pairs

This work is supported in part by the DARPA IDEA program, as part of the ALIGN project, under SPAWAR Contract N660011824048.

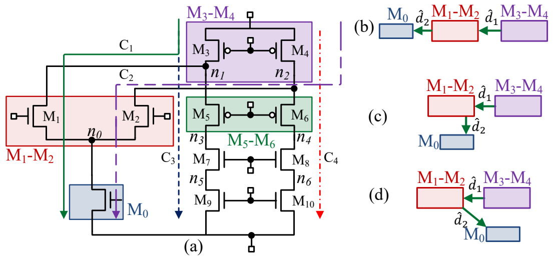


Fig. 1. (a) Schematic of the folded-cascode OTA. (b)–(d) Various placement configurations for paths C$_1$ and C$_2$. (b) and (c) are monotonic but (d) is not.

(M$_1$, M$_2$), (M$_3$, M$_4$), and (M$_5$, M$_6$) into blocks, since these transistor layouts will be interleaved to reduce mismatch [12]. While the examples in this paper use hard blocks with fixed aspect ratio to illustrate the limitations of current path and potential of CF metrics in AMS layout generation, similar conclusions can be reached with soft macros, which have flexible aspect ratios.

The relative placement of two consecutive blocks of a current path can be represented by a unit vector that connects the closest pair of points on their boundaries. In Fig. 1(b)–(d), unit vectors between blocks (M$_3$–M$_4$, M$_1$–M$_2$) and (M$_1$–M$_2$, M$_0$) on paths C$_1$ and C$_2$ are denoted as $\hat{d}_1$ and $\hat{d}_2$, respectively.

**Definition:** In a placement, a current path is considered to be *monotonic* if all consecutive unit vector pairs of the current path form an angle in the range of $[-90°, 90°]$.

Current path C$_1$ is seen to be monotonic in Fig. 1(b) and (c), but non-monotonic in Fig. 1(d): intuitively, we see that under Manhattan routing, the wires in the latter case must "backtrack" (as compared to Fig. 1(c), which has a more direct connection to M$_0$), leading to higher wirelengths and parasitics.

Existing techniques, based on sequential [1] and monotonic [9]–[11] placements on a current path, attempt to reduce parasitics in the current paths by establishing proximity based on connectivity. These techniques have several limitations.

*First*, merely maintaining monotonicity does not guarantee optimal wirelength on the current paths. Figs. 2(a) and 2(b) show two possible configurations of the blocks on current paths C$_1$–C$_4$. In this linear placement, the HPWLs of $n_1$ and $n_2$ are the linear distances between their pins. It can be seen that both nets have the same HPWL in both layouts, and all four current paths are monotonic in both layouts. However, Fig. 2(b) is preferable to Fig. 2(a) since it has a lower total net length for the high-current paths C$_3$ and C$_4$. This leads to lower resistive losses on these paths: high resistance can degrade the overdrive voltage of one or more transistors in the current path, which could lead to circuit malfunction if the transistor(s) are moved out of their operating point in the saturation region. This issue is particularly concerning in FinFET technologies, where the per-unit wire resistances are high and the devices operate with a lower supply voltage compared to the older technologies.

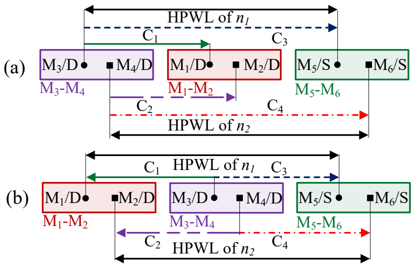


Fig. 2. Two different monotonic placements, (a) and (b), for interleaved transistor blocks M$_3$–M$_4$, M$_1$–M$_2$, and M$_5$–M$_6$ of Fig. 1.

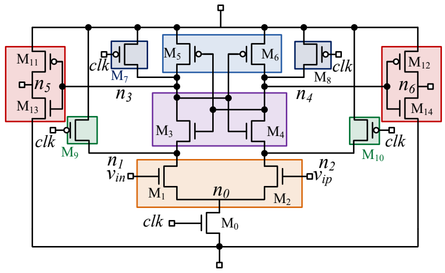


Fig. 3. Schematic of the high-speed comparator circuit.

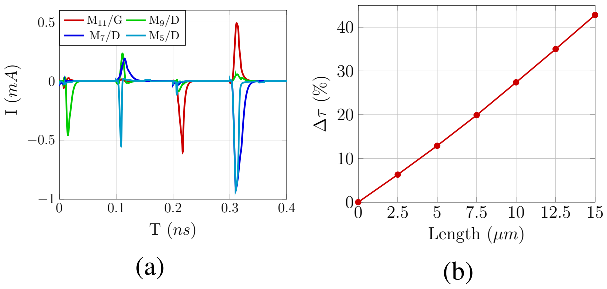


Fig. 4. (a) Comparison of the gate current of M$_{11}$ and drain currents of M$_5$, M$_7$, M$_9$. (b) Change in response time ($\Delta\tau$) with the net parasitics.

*Second*, existing approaches that enforce current path monotonicity focus only on source-drain connected paths and ignore gate connections. These connections are especially important in multi-stage AMS designs, where the stages typically interface through transistor gate terminals. For the high-speed comparator in Fig. 3, Fig. 4(a) shows that the dynamic current on net $n_3$, which charges and discharges the capacitance on the gate terminal of M$_{11}$, is comparable to the drain currents of M$_5$, M$_7$, and M$_9$. The RC parasitics on $n_3$ affect the response time, $\Delta\tau$, of the comparator.[1] For a 12nm FinFET design operating at 5GHz, Fig. 4(b) shows $\Delta\tau$ as we sweep the length of net $n_3$ from zero to the layout semi-perimeter.

## III. Charge Flow Metrics

We now devise CF metric for placement that defines an attraction metric between a pair of connected pins in a placement whose strength is determined by the estimated current flow between the pins. Our description illustrates CF metrics for signal nets, and a similar approach can be used for supply nets.

### A. Graph Representation of CFs

Consider a netlist, $H$, consisting of a set of nets, $N = \{n_i \mid i \in \mathbb{N}^+\}$. Each net, $n_i$, is connected to a set of two or more pins, $P_i$, from multiple instances.

[1] The response time is defined as the time spent to cross the threshold value of output logic from the positive edge of the clock signal.

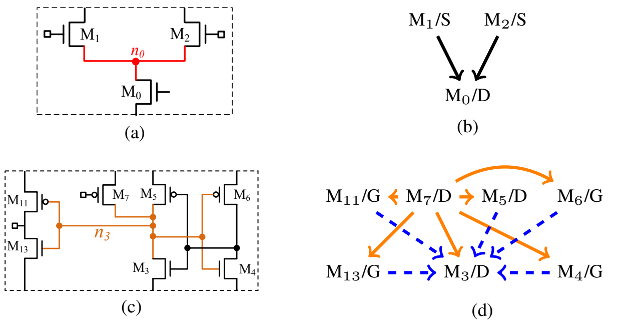


Fig. 5. G, D and S represent the gate, drain and source terminals of the transistors respectively; (a) Connectivity of net $n_0$ of Fig. 1. (b) Pin-to-pin current flow of $n_0$ of Fig. 1 at any time during steady state operation. (c) Connectivity of net $n_3$ of Fig. 3. (d) Pin-to-pin current flow of $n_3$ of Fig. 3 at time instances in pre-charge (solid line) and evaluation phase (dashed line).

At any time instant $t$, each pin can be classified either as a *transmitter* if current flows out of the pin, or as a *receiver* if the current flows into the pin. The same pin can act as a transmitter or a receiver at different time instants, e.g., the gate of transistors M$_{11}$–M$_{13}$ in Fig. 3 is a receiver during precharge, when outputs $n_5$ and $n_6$ are set to zero, and a transmitter during evaluation, when these outputs react to the comparator inputs.

The direction of current at any time instant $t$ can be represented using directed edges between a transmitter and a receiver. For example, Fig. 5(a) shows the connections of net $n_0$ from Fig. 1 and Fig. 5(b) is its graph representation. The three pins, M$_0$/D, M$_1$/S, and M$_2$/S, are the vertices, and the directed edges show the direction of current flow: here, M$_1$/S and M$_2$/S act as transmitters at all times. Fig. 5(c) and (d) show the connections for net $n_3$ of Fig. 3 and the graph representation: the solid (dashed) lines represent the current flow directions during the precharge (evaluation) phase of the comparator. Here, M$_4$/G, M$_5$/D, M$_6$/G, M$_{11}$/G and M$_{13}$/G act as transmitters and receivers at different time instants.

### B. Formulating CF Metrics

CF metrics are based on the cumulative charge transfer between every pair of pins of a circuit, and depends on the current flow between the respective pin-pairs. We use the results of transient simulations, which are available "for free" from functional verification, to generate the CF metrics. These simulations capture both the static and dynamic behavior of the circuit.

For multipin nets, it is necessary to estimate the pairwise pin-to-pin currents from the pin currents obtained from simulation, without knowing the layout parasitics. We assume the contribution to the current at each receiver is in proportion to the current from each transmitter. The instantaneous current from a transmitter pin $A$ to a receiver pin $B$ can be evaluated as:

$$i_{A,B}(t) = i_B(t) \times \frac{i_A(t)}{\sum_{S \in Tx(B)} i_S(t)} \tag{1}$$

where $Tx(B)$ is the set of all transmitters to pin $B$ of net $n_i$ at time instant $t$. This current estimate is exact at a time $t$ if at that instant there is either only one receiver or one transmitter for the net $n_i$. For other scenarios, it is an approximation. In practice, since $i_{A,B}(t)$ will be used to construct an attraction metric for the placer, high accuracy is not needed: the primary purpose of the metric is to distinguish pin pairs with high or low attraction. Therefore, the approximation is adequate, and we demonstrate its usefulness in our experimental evaluation.

For a pin pair ($A$, $B$), the attraction metric consolidates the current over all time and is defined using the absolute CF,

$$q_{A,B} = \int_{t_0}^{t_0+T} |i_{A,B}| dt \tag{2}$$

where $t_0$ is the start time and $T$ is the period of operation. Note that the impact of parasitics on circuit performance is independent of the direction of the current flow, and by using the absolute value of the current flow in Eq. (2), we make the attraction metric direction-independent.

Finally, we normalize each $q_{A,B}$ value to $\hat{q}_{A,B}$ as follows:

$$\hat{q}_{A,B} = q_{A,B}/q_{max} \tag{3}$$

where $q_{max}$ is the maximum pin-to-pin CF in the circuit.

### C. Formulation of the Placement Problem

A typical conventional cost function for placement is [13]:

$$F(P) = \lambda_1 \cdot f_1(A(P)) + \lambda_2 \cdot f_2(L(P)) \tag{4}$$

where $A$ is the area of the placement $P$, $L$ is the sum or mean of wirelengths (typically estimated as HPWL) of all nets in the design. Each $f_i$ is a normalization function that ensures that the cost function components are of similar magnitude (e.g., normalized to lie in the interval $[0, 1]$); and each $\lambda_i$ is the weight associated with cost function component $f_i$, specifying its relative importance. We solve the problem using a stochastic solver based on [14]. During optimization of the cost function, the solver considers only placement solutions $P$ that preserve the symmetric and self-symmetric constraints given to the placer. We use the CF formulation in two ways:

(1) To specify symmetric and self-symmetric constraints, we utilize CF data to automatically identify symmetry group(s) in a circuit. Details are provided in Section V.

(2) To optimize parasitics on performance-critical nets, we modify (4) using the normalized CF, $\hat{q}_{A,B}$, and the distance metric, $d_{A,B}$, by adding a component to the objective function:

$$f_3(P) = \sum_{i=1}^{|n_i|} \sum_{A,B \in P_i; A \neq B} \hat{q}_{A,B} \times d_{A,B} \tag{5}$$

where $P$ is a given placement configuration. The objective function to be optimized is now altered to:

$$F(P) = \lambda_1 \cdot f_1(A(P)) + \lambda_2 \cdot f_2(L(P)) + \lambda_3 \cdot f_3(P) \tag{6}$$

Thus, CF metrics are incorporated into an unconstrained objective function using a weighted-sums formulation.

The component $f_3$ in the objective function induces the placer to minimize the pin-to-pin distance based on the CF between the pins. The CF metrics also weight the nets based on the charge transfer, thereby giving importance to critical nets. This approach overcomes the limitations of prior work listed in Section II: (1) Contrary to the current path method,

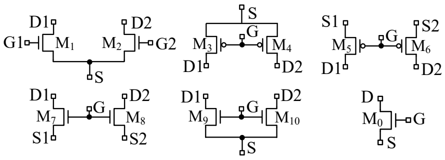


Fig. 6. Primitives identified in the folded cascode OTA of Fig. 1.

the CF methodology does not rigidly restrict the solution space to monotonic CFs but merely incentivizes solutions that optimize CF, potentially providing better and more compact layouts. (2) Unlike current path constraints in prior work that are limited to source-drain connections, our CF formulation considers flows to the gate connection of a transistor.

## IV. Generating CF Metrics

Our flow takes a circuit netlist and data from its transient simulation as inputs, available "for free" from functional simulation during schematic design. These simulations are exhaustive enough to exercise all important modes in the circuit. The steps in our CF-based placement framework are:

**(1) Netlist Preprocessing** We process the netlist to identify *primitives* [15]–[18], or basic structures in analog circuits such as differential pairs, current mirrors, or clocked switches. These primitives, shown in Fig. 6 for the FC OTA, group transistors to identify easy matching/symmetry requirements.

TABLE I
Connectivities of the nets of the FC OTA.

| Net name | Pins | Net name | Pins |
|---|---|---|---|
| $n_1$ | $P_1$ = {M$_1$/D, M$_3$/D, M$_5$/S} | $n_2$ | $P_2$ = {M$_2$/D, M$_4$/D, M$_6$/S} |
| $n_3$ | $P_3$ = {M$_5$/D, M$_7$/D} | $n_4$ | $P_4$ = {M$_6$/D, M$_8$/D} |
| $n_5$ | $P_5$ = {M$_7$/S, M$_9$/D} | $n_6$ | $P_6$ = {M$_8$/S, M$_{10}$/D } |
| $n_0$ | $P_0$ = {M$_0$/D, M$_1$/S, M$_2$/S} | | |

**(2) Connectivity and pin current extraction** Lists of all pins connected to each net, $n_i$, are stored in a set, $P_i$: for the FC OTA, the pin lists are shown in Table I. The results of transient simulation from the schematic design phase are then used to collect information about the current flow of all pins.

**(3) Pin-to-pin current estimation** Next, the instantaneous pin-to-pin branch currents are estimated between all pin pairs in each net in the CF graph (Eq. (1)). These currents are mapped to the primitives, which form unit blocks for placement. The consolidated list of pin pairs of FC OTA is listed in Table II. When two or more pin pairs are merged, their currents are combined, e.g., when primitive M$_1$–M$_2$ merges the pin pairs of net $n_0$ into (M$_1$–M$_2$/S, M$_0$/D) the currents from (M$_0$/D, M$_1$/S) and (M$_0$/D, M$_2$/S) are added.

**(4) Charge flow calculation** The normalized pin-to-pin CF is computed using Eq. (2)–(3) for all the pin pairs of all nets. This value presents the relative importance of each pin-pair.

TABLE II
Connectivity of the FC OTA following primitive annotation.

| | | | |
|---|---|---|---|
| $n_1$ | (M$_1$–M$_2$/D1, M$_3$–M$_4$/D1)<br>(M$_1$–M$_2$/D1, M$_5$–M$_6$/S1)<br>(M$_5$–M$_6$/S1, M$_3$–M$_4$/D1) | $n_2$ | (M$_1$–M$_2$/D2, M$_3$–M$_4$/D2)<br>(M$_1$–M$_2$/D2, M$_5$–M$_6$/S2)<br>(M$_5$–M$_6$/S2, M$_3$–M$_4$/D2) |
| $n_3$ | (M$_7$–M$_8$/D1, M$_5$–M$_6$/D1) | $n_4$ | (M$_7$–M$_8$/D2, M$_5$–M$_6$/D2) |
| $n_5$ | (M$_9$–M$_{10}$/D1, M$_7$–M$_8$/S1) | $n_6$ | (M$_9$–M$_{10}$/D2, M$_7$–M$_8$/S2) |
| $n_0$ | (M$_1$–M$_2$/S, M$_0$/D) | | |

## V. Symmetry group detection using CF metrics

We now describe the CF-based approach to identify *symmetry groups* in a circuit hierarchically. A symmetry group is a set of blocks (transistors, passive components, or primitives) whose elements are placed along a common axis of symmetry.

Each block $b_i$ is associated with a feature set, $F_i = \{\rho_k\}$, defined by a multiset[2]. Each element of the multiset specifies a CF metric, $q_{i,j}$, between $b_i$ and another block $b_j$. We also maintain $\{v_i\}$, the set of all DC node voltages of all pins of $b_i$, and $k_i$, the type of primitive (or individual transistor).

We illustrate the approach using the high-speed comparator (Fig. 3). The analog layout generator that we use identifies the primitives M$_1$–M$_2$, M$_3$–M$_4$, and M$_5$–M$_6$ whose layouts are interleaved, and the transistor pairs M$_{11}$–M$_{13}$ and M$_{12}$–M$_{14}$ as inverter primitives. Transistors M$_7$ through M$_{10}$ are clock-connected transistors and are considered as single-transistor switch primitives. Thus, the set of transistor blocks is given by:

$$B = \{\mathrm{M}_0,\ \mathrm{M}_1\text{–}\mathrm{M}_2,\ \mathrm{M}_3\text{–}\mathrm{M}_4,\ \mathrm{M}_5\text{–}\mathrm{M}_6,\ \mathrm{M}_7,\ \mathrm{M}_8,\ \mathrm{M}_9,\ \mathrm{M}_{10},\ \mathrm{M}_{11}\text{–}\mathrm{M}_{13},\ \mathrm{M}_{12}\text{–}\mathrm{M}_{14}\}$$

Block M$_1$–M$_2$ has nonzero CF metrics with M$_0$, M$_3$–M$_4$, M$_9$, and M$_{10}$. The use of the multiset (instead of a set) helps to represent the two CF metrics M$_1$–M$_2$ has with M$_3$–M$_4$ at nodes $n_1$ and $n_2$ although the CF metrics are identical.

The approach builds symmetry group(s) by identifying potential symmetric placements (i.e., symmetric placement on either side of a common axis) and self-symmetric placements (i.e., placement of the block along the same axis as another block) of each block using the feature sets, $F_i$. The algorithm consists of several steps, listed below:

**(1) Group identical blocks** In this step, identical transistor blocks are grouped in a set and added to the set of candidate symmetry groups. Two or more blocks are identical if they are of the same type (identical primitive or individual transistor), have identical feature sets (i.e., they have an identical set of CF metrics), and identical node voltages at corresponding nodes. These blocks are candidates to be placed symmetrically around a common axis in the layout. For the comparator, the candidate symmetry groups are:

$$\{\mathrm{M}_7,\ \mathrm{M}_8\},\ \{\mathrm{M}_9,\ \mathrm{M}_{10}\},\ \{\mathrm{M}_{11}\text{–}\mathrm{M}_{13},\ \mathrm{M}_{12}\text{–}\mathrm{M}_{14}\}$$

Note that identical differential structures have the same charge flow since Eq. (2) uses the absolute value of current. Even for an AC differential signal, this absolute value is identical over an equal number of positive and negative half-cycles.

**(2) Find potential self-symmetric block pairs** In this step, we identify pair of blocks that are neighbors (i.e., blocks connected by one or more nets) for which some features, but not all, are identical: such blocks could share an axis of symmetry.

For the comparator, this step considers M$_1$–M$_2$ and M$_3$–M$_4$ as potential self-symmetric pairs as both share two CF metrics (features), corresponding to nets $n_1$ and $n_2$, that are identical as a consequence of sharing a differential path, but also have other CF metrics that are different (e.g., between M$_1$–M$_2$ and M$_0$). Similarly, M$_3$–M$_4$ and M$_5$–M$_6$

[2] A multiset is a set that allows multiple instances of the same elements (unlike a set where repeated entries appear just once).

are also potential self-symmetric pairs. The full set of groups is:

$$\{\text{M}_1\text{–M}_2,\ \text{M}_3\text{–M}_4\},\ \{\text{M}_3\text{–M}_4,\ \text{M}_5\text{–M}_6\} \qquad .$$

**(3) Post-process self-symmetric block pairs** The post-processing is done in two steps:

- For three or more blocks, if (i) all pairwise combinations are in the candidate self-symmetric set *and* (ii) any two of these blocks are neighbors, then these blocks are not considered for self-symmetry. This scenario is not seen in the comparator, and is typically activated in circuits with parallel structures, such as the FC OTA (Fig. 1(a)): placing $\text{M}_1$–$\text{M}_2$, $\text{M}_3$–$\text{M}_4$, and $\text{M}_5$–$\text{M}_6$ self-symmetrically is suboptimal; instead, placing $\text{M}_1$–$\text{M}_2$ and $\text{M}_5$–$\text{M}_6$ on either side of $\text{M}_3$–$\text{M}_4$ is preferable. By freeing these blocks from self-symmetric constraints, we permit the placer to find the optimal placement with lower parasitics. Since the CF metrics are identical, the placer positions these blocks symmetrically about the center block, as we will see in Fig. 8.
- If two or more potentially self-symmetric sets share a common transistor block, the sets are merged. For the comparator, this implies that sets $\{\text{M}_1\text{–M}_2,\ \text{M}_3\text{–M}_4\}$, $\{\text{M}_3\text{–M}_4,\ \text{M}_5\text{–M}_6\}$, which share $\text{M}_3$–$\text{M}_4$, are merged to $\{\text{M}_1\text{–M}_2,\ \text{M}_3\text{–M}_4,\ \text{M}_5\text{–M}_6\}$.

**(4) Add set(s) of identical blocks to symmetry group** This step finds if a block, $b_i$, can potentially share an axis of symmetry with an already-identified symmetric pair $\{b_m, b_n\}$. Block $b_i$ can be placed self-symmetrically to these blocks if its CF metrics with $b_m$ and $b_n$ are identical.

In the comparator, transistor pairs $\{\text{M}_9,\ \text{M}_{10}\}$ will have identical CF metrics with both $\text{M}_1$–$\text{M}_2$ and $\text{M}_3$–$\text{M}_4$ (which belong to the same symmetric group) due to the differential architecture. Similarly, $\{\text{M}_7,\ \text{M}_8\}$ and the inverters $\{\text{M}_{11}\text{–M}_{13},\ \text{M}_{12}\text{–M}_{14}\}$ will have identical CF metrics with $\text{M}_3$–$\text{M}_4$ and $\text{M}_5$–$\text{M}_6$ (also a symmetric pair). Hence, after this step, all identical blocks of the comparator are placed along the axis of symmetry of the self-symmetric structures. This leads to the following symmetries:

$$\{\text{M}_1\text{–M}_2,\ \text{M}_3\text{–M}_4,\ \text{M}_5\text{–M}_6,\ \{\text{M}_7,\ \text{M}_8\},$$
$$\{\text{M}_9,\ \text{M}_{10}\},\ \{\text{M}_{11}\text{–M}_{13},\ \text{M}_{12}\text{–M}_{14}\}\}$$

where the singleton transistor block sets are self-symmetric along an axis, and other sets are symmetric about this axis. Note that transistor $\text{M}_0$ does not have to be placed along this axis, but the connection point from primitive $\text{M}_1$–$\text{M}_2$ must be at its center when it connects to $\text{M}_0$.

This method allows the identification of more than one axis of symmetry, but this case is not activated for the comparator.

**(5) Identify symmetry for the remaining identical blocks** If, after repeated application of the previous step, there are still multiple identical blocks that have not been assigned to an axis, we place these blocks symmetrically about a new axis. This case is not seen for the comparator, but for the FIR equalizer in [8], this method distributes the 10 identical parallel structures evenly about an axis (details omitted due to space constraints).

## VI. Results

Our CF framework is implemented in Python. We use Spectre for circuit simulation, Calibre nmLVS for LVS, and Calibre xACT for extraction. All evaluations are carried out on a Linux server (Intel Xeon(R) 2.20GHz Silver 4114 CPU, 160GB memory) and all testcases are designed with a commercial 12nm PDK. We use an analog layout generator, with objective functions (4) and (6), that automatically detects primitives from a library; prepares layouts and assembles the building blocks at each level of hierarchy using a C++ simulated annealing placer based on [14]. We compare against layouts that maintain current path monotonicity, using manual layouts where needed.

Our approach is applied to a FC OTA, high-speed comparator, variable gain amplifier (VGA), double-tail sense amplifier (DTSA), two-stage OTA, and linear equalizer (LE). The maximum CPU time over all testcases is 4.6s. Table III lists specifications and performance for layouts generated with/without CF metrics, using "✓" if a specification is met and "✗" otherwise. Unlike competing methods, our CF flow meets all constraints.

Table IV compares the HPWL of the layouts generated for all testcases: HPWL values of all layouts for each testcase are normalized with the conventional automated layout generated using Eq. (4). Although conventional or current path-based placement could achieve smaller HPWL compared to CF-based placement, the smaller HPWL does not necessarily result in better performance or matching (Table III). Table V includes the placement runtime for the conventional and CF-driven cases, driven by objective functions (4) and (6), respectively. The use of CF causes negligible runtime increase ($< 6\%$). We compare the quality of symmetry group detection with CF metrics

TABLE III
PERFORMANCE COMPARISON OF THE LAYOUTS DEVELOPED WITH THE CONVENTIONAL OBJECTIVE FUNCTION (EQ. (4)), CURRENT PATH CONSTRAINTS, AND THE CF-BASED OBJECTIVE FUNCTION (EQ. (6))

| Circuit | Metrics | Spec. | Conventional | | Current path | | Charge flow | |
|---|---|---|---|---|---|---|---|---|
| FC OTA | DC gain (dB) | ≥20 | 17.09 | ✗ | 17.09 | ✗ | 25.87 | ✓ |
| | UGF (MHz) | ≥100 | 43.17 | ✗ | 43. 17 | ✗ | 385.57 | ✓ |
| | Phase margin (°) | ≥60 | 83.37 | ✓ | 83.37 | ✓ | 88.70 | ✓ |
| High-speed comparator | Response time (ps) | ≤100 | 100.49 | ✗ | 101.34 | ✗ | 97.61 | ✓ |
| | Offset (mV) | ≤3 | 3.30 | ✗ | 2.76 | ✓ | 2.51 | ✓ |
| VGA | Min Gain (dB) | ≥ −5 | −4.46 | ✓ | −3.53 | ✓ | −1.57 | ✓ |
| | Max Gain (dB) | ≥ 6 | 6.73 | ✓ | 7.12 | ✓ | 8.57 | ✓ |
| | UGF (GHz) | ≥ 30 | 21.50 | ✗ | 29.45 | ✗ | 30.79 | ✓ |
| | Phase margin (°) | ≥60 | 104.61 | ✓ | 100.48 | ✓ | 94.59 | ✓ |
| DTSA | Response time (ps) | ≤40 | 50.93 | ✗ | 39.89 | ✓ | 36.47 | ✓ |
| | Offset (mV) | ≤ 3 | 2.56 | ✓ | 1.17 | ✓ | 2.53 | ✓ |
| Two-stage OTA | DC gain (dB) | ≥45 | 48.48 | ✓ | 41.19 | ✗ | 49.16 | ✓ |
| | UGF (MHz) | ≥125 | 130.15 | ✓ | 119.15 | ✗ | 139.47 | ✓ |
| | Phase margin (°) | ≥60 | 63.46 | ✓ | 76.46 | ✓ | 62.27 | ✓ |
| LE | Gain (dB) | ≥0 | −0.08 | ✗ | 1.02 | ✓ | 1.14 | ✓ |
| | Bandwidth (GHz) | ≥ 10 | 14.15 | ✓ | 12.73 | ✓ | 13.66 | ✓ |

TABLE IV
HPWL OF THE LAYOUTS FOR THE TESTCASES, NORMALIZED TO THE HPWL OF THE CONVENTIONAL LAYOUT USING EQ. (4)

| Placement technique | FC OTA | High-speed comparator | VGA | DTSA | Two-stage OTA | LE |
|---|---|---|---|---|---|---|
| Current path | 1.00 | 1.02 | 1.12 | 1.25 | 1.10 | 1.14 |
| Charge flow | 1.08 | 1.07 | 1.17 | 1.15 | 1.04 | 1.05 |

TABLE V
RUNTIME COMPARISON OF THE LAYOUTS DEVELOPED WITH CONVENTIONAL (EQ. (4)) AND CF-BASED (EQ. (6)) OBJECTIVE FUNCTION

| Cost function | FC OTA | High-speed comparator | VGA | DTSA | Two-stage OTA | LE |
|---|---|---|---|---|---|---|
| Conventional | 25.22s | 39.93s | 47.47s | 38.94s | 22.30s | 49.18s |
| Charge flow | 25.58s<br>(+1.43%) | 40.76s<br>(+2.08%) | 49.25s<br>(+3.75%) | 41.12s<br>(+5.60%) | 22.63s<br>(+1.48%) | 50.75s<br>(+3.19%) |

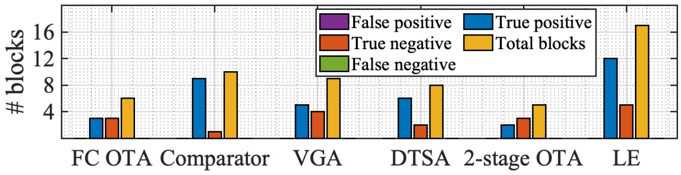
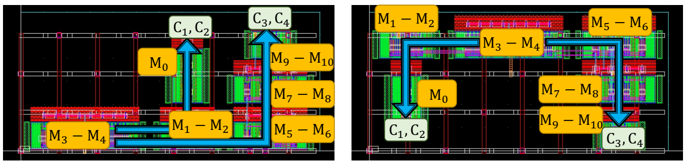


Fig. 7. Accuracy of symmetry group detection with CF metrics.



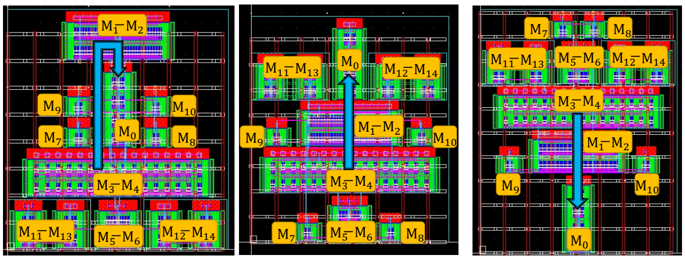
(a) (b)

Fig. 8. FC OTA (Fig. 1(a)) layouts under (a) conventional constraints, (b) the CF formulation. The areas for both layouts are equal: 6.07$\mu$m×13.07$\mu$m.

against designer annotation in Fig. 7. If a block belongs (does not belong) to a symmetry group, we consider it as a positive (negative) sample. A true sample implies that the CF-based annotation of a block, positive or negative sample, matches with the designer annotation. The data shows 100% accuracy (zero false positives/false negatives) on these testcases.

Figs. 8(a)–(b) show the layouts of the FC OTA of Fig. 1, along with the current paths using the conventional and the CF-based objective functions. Since the conventional layout satisfies the monotonic current path requirements, a manual layout is not required. Both placements use the symmetry constraints $\{M_5–M_6, M_7–M_8, M_9–M_{10}\}$ extracted by the CF-based method. As in the comparator, $M_0$ is not required to be on the axis of $M_1–M_2$ as long as $M_0$ is connected to the center of the pin of $M_1–M_2$. Unlike a conventional approach that reduces the HPWL for all nets connecting $M_1–M_2$, $M_3–M_4$, and $M_5–M_6$ together, the CF-based approach uses current directions to recognize that reducing net length between $\{M_1–M_2, M_3–M_4\}$ and $\{M_3–M_4, M_5–M_6\}$ are more important than between $\{M_1–M_2, M_5–M_6\}$. The HPWL metric results in the layout of Fig. 8(a) with a large net length (therefore a larger resistance) between $M_3–M_4$ and $M_5–M_6$. These parasitics push $M_5$ and $M_6$ out of the saturation region, causing significant performance drop (Table III). The CF-based layout in Fig. 8(b) has 8% higher HPWL, but biases these transistors in saturation because even this slightly larger capacitance is 0.29% of the load capacitance and has negligible effect on circuit performance.

For the high-speed comparator (Fig. 3), using the CF-based symmetry groups (Section V), Figs. 9(a), (b), and (c) show the layouts generated using the conventional objective functions, current path constraints, and the CF formulation, respectively.



(a) (b) (c)

Fig. 9. High-speed comparator layout (dimensions in parentheses) under: (a) conventional constraints (14.91$\mu$m×13.47$\mu$m), (b) current path constraints (14.91$\mu$m×13.07$\mu$m), (c) the CF formulation (16.49$\mu$m×13.47$\mu$m).

The conventional objective function (4) incentivizes HPWL reduction but creates a nonmonotonic current path (illustrated by the blue arrow in Fig. 9) for $M_3–M_4 \rightarrow M_1–M_2 \rightarrow M_0$, resulting in long interconnects between $M_3–M_4$ and $M_1–M_2$. The layouts generated with traditional current path constraints similar to [9]–[11] (Fig. 9(b)) and the CF formulation (Fig. 9(c)) overcome this issue. However, Fig. 9(b) has no assertions for gate-connected primitives at $n_3$ and $n_4$, $M_{11}–M_{13}$ and $M_{12}–M_{14}$. Unlike this layout, our CF-based methodology automatically places $M_{11}–M_{13}$ and $M_{12}–M_{14}$ close to the blocks that they charge/discharge through, resulting in the lowest offset and response time among the layouts, as shown in Table III.

## VII. Conclusion

A novel CF-based formulation, using ‘free” simulation data from schematic design, is shown to extract symmetry constraints and provide net importance metrics for AMS placement. The CF methodology is integrated into layout generation and its effectiveness is demonstrated on several AMS circuits.

## References

[1] D. Long, *et al.*, “Signal-Path Driven Partition and Placement for Analog Circuit,” in *Proc. ASP-DAC*, pp. 6–11, 2006.

[2] K. Zhu, *et al.*, “Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow,” in *Proc. ICCAD*, 2020.

[3] Y. Li, *et al.*, “A Customized Graph Neural Network Model for Guiding Analog IC Placement,” in *Proc. ICCAD*, 2020.

[4] M. Liu, *et al.*, “Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning,” in *Proc. DATE*, pp. 496–501, 2020.

[5] T. Dhar, *et al.*, “Fast and Efficient Constraint Evaluation of Analog Layout Using Machine Learning Models,” in *Proc. ASP-DAC*, pp. 158–163, 2021.

[6] E. Malavasi, *et al.*, “Automation of IC layout with analog constraints,” *IEEE T. Comput. Aid D.*, vol. 15, pp. 923–942, 1996.

[7] M. Eick, *et al.*, “Comprehensive Generation of Hierarchical Placement Rules for Analog Integrated Circuits,” *IEEE T. Comput. Aid D.*, vol. 30, pp. 180–193, 2011.

[8] K. Kunal, *et al.*, “A General Approach for Identifying Hierarchical Symmetry Constraints for Analog Circuit Layout,” in *Proc. ICCAD*, 2020.

[9] P.-H. Wu, *et al.*, “Performance-driven Analog Placement Considering Monotonic Current Paths,” in *Proc. ICCAD*, pp. 613–619, 2012.

[10] H.-C. Ou, *et al.*, “Simultaneous Analog Placement and Routing with Current Flow and Current Density Considerations,” in *Proc. DAC*, pp. 1–6, 2013.

[11] A. Patyal, *et al.*, “Analog Placement with Current Flow and Symmetry Constraints using PCP-SP,” in *Proc. DAC*, pp. 1–6, 2018.

[12] A. Hastings, *The Art of Analog Layout*. Upper Saddle River, NJ: Prentice-Hall, 2001.

[13] H. E. Graeb, *Analog Layout Synthesis*. New York, NY: Springer, 2011.

[14] Q. Ma and L. Xiao and Y.-C. Tam and E. F. Y. Young, “Simultaneous Handling of Symmetry, Common Centroid, and General Placement Constraints,” *IEEE T. Comput. Aid D.*, vol. 30, pp. 85–95, Jan. 2011.

[15] T. Massier, *et al.*, “The sizing rules method for CMOS and bipolar analog integrated circuit synthesis,” *IEEE T. Comput. Aid D.*, vol. 27, pp. 2209–2222, Dec. 2008.

[16] K. Kunal, *et al.*, “GANA: Graph Convolutional Network Based Automated Netlist Annotation for Analog Circuits,” in *Proc. DATE*, pp. 55–60, 2020.

[17] K. Kunal, *et al.*, “ALIGN: Open-source analog layout automation from the ground up,” in *Proc. DAC*, 2019.

[18] T. Dhar, *et al.*, “ALIGN: A System for Automating Analog Layout,” *IEEE Design & Test*, vol. 38, pp. 8–18, Apr. 2020.