CURRICULUM VITAE

Keshab K. Parhi
Email: parhi@umn.edu
http://ece.umn.edu/users/parhi

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EDUCATION

- Ph.D., Electrical Engineering and Computer Sciences, University of California, Berkeley, September 1988, Research Advisor: Prof. David G. Messerschmitt.
  THESIS: Algorithm and Architecture Designs for High-Speed Digital Signal Processing

- M.S.E.E., Univ. of Pennsylvania, Philadelphia, May 1984, Concentrated on signal processing and VLSI IC design. Research Advisor: (Late) Prof. Raymond S. Berkowitz.
  THESIS: Application of Importance Sampling for False Alarm Setting in Complex Multi-Dimensional Signal Processing Systems

- B.Tech. (Honors), Indian Institute of Technology, Kharagpur, India, May, 1982, Electrical Engineering.

INDUSTRIAL AND ACADEMIC EXPERIENCE

- Professor (Tenured), Department of Electrical Engineering, University of Minnesota, Minneapolis, MN, 55455 (starting July 1995). Edgar F. Johnson Professor (Starting July 1997). Distinguished McKnight University Professor (Starting July 2000). Associate Professor with Tenure (July 1992 - June 1995), Assistant Professor (Oct. 1988 - June 1992), Research efforts directed towards VLSI Architectures for Digital Signal Processing and machine learning systems, VLSI Digital Filters, Adaptive Filters and Beamformers, Video Compression, Error Control Coders, Cryptography, Computer Arithmetic, Low-Power Digital Systems, CAD for Low-Power, Digital IC Design and FPGA System Prototyping, DNA computing and DNA signal processing, and Hardware Security. Current research is also directed towards biomedical signal processing and signal classification, particularly with the use of machine learning techniques. Current applications include biomarkers for schizophrenia, epilepsy, and mental disorders from MEG, EEG, and functional MRI. Other applications include retinal image analysis from fundus images and OCT.

- Visiting Professor, Stanford University, 2018

- Visiting Professor, Fudan University, Shanghai, China, 2017

- Director of Graduate Studies of the Electrical Engineering Program, University of Minnesota, July 2008 - September 2011

- President, Leanics Corporation, 2005-2012
- Medtronic, Inc., Minneapolis, MN, 2006-2007, on Sabbatical Leave
- Broadcom Corp., Irvine, (2000-2002), Senior Principal Scientist and Technical Director - DSP Systems, Office of CTO (on Leave)
- Technical Advisory Board, Morphics, Inc. (2002-2003)
- Visiting Professor, Lund Univ., Sweden (April 1999)
- Visiting Researcher, NEC C&C Laboratories, Kanagawa, Japan (1996-97 Academic Year, on Leave as National Science Foundation Fellow)
- Visiting Professor, Delft Univ., The Netherlands (March - April, 1996)
- Visiting Researcher, NEC C&C Laboratories, Kanagawa, Japan (April 1992 - June 1992), Researched VLSI Architectures for Discrete Wavelet Transforms.
- Consultant to Dorsey and Whitney (2007), Theseus Logic (1996-1999), United Nations Development Program (1995), Top-Vu Technology, Inc. (1994) US West Advanced Technologies (1989), Bell Labs (1987 - 1988),
- Summer Job at AT&T Bell Laboratories, Holmdel, NJ during Summer 1987.
- Summer job at the IBM T.J. Watson Research Center, Yorktown Heights, NY, during Summer 1986.

AWARDS AND HONORS

- Fellow, American Association for Advancement of Science (2017)
- Fellow, IEEE (1996)
- IEEE Kiyo Tomiyasu Technical Field Award (2003)
- Mac Van Valkenburg Award, IEEE Circuits and Systems Society (2017)
- IEEE Charles A. Desoer Technical Achievement Award, IEEE Circuits and Systems Society (2012)
- Distinguished Alumnus Award, Indian Institute of Technology, Kharagpur (2013)
- Award for Outstanding Contributions to Postbaccalaureate, Graduate, and Professional Education, University of Minnesota (2013)
- Frederick Emmons Terman Award from American Society of Engineering Education (2004)
- IEEE Circuits and Systems Society Golden Jubilee Medal (2000)

- National Science Foundation Young Investigator Award, 1992-1997
- National Science Foundation Research Initiation Award, 1989
- IEEE Trans. VLSI Systems Prize Paper Award (2017)
- IEEE W.R.G. Baker Best Paper Award (2001)
- Darlington Best Paper Award of the IEEE Circuits and Systems Society, 1994
- Guillemin-Cauer Best paper Award of the IEEE Circuits and Systems Society, 1993
- IEEE Signal Processing Society Paper Award, 1991,
- IEEE Browder J. Thompson Memorial Prize paper Award, 1991
- Best Paper Award at the 2017 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED) (2017)
- Best Paper Award at the 2016 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED) (2016)
- Best (Student) Paper Award for the Design and Implementation of Signal Processing Systems (DISPS) Track at the IEEE ICASSP Conference (2015)
- Best (Student) Paper Award at the 6th IEEE Int. Conference on Neural Engineering (2013)
- Best (Third Place Student) Paper Award, 2012 Asilomar Conference on Signals, Systems and Computers (2012)
- Best (Student) Paper Award at the Asilomar Conference on Signals, Systems and Computers (2004)
- ACM Great Lakes Symp. Best Paper Award, 2004
- Best Paper Award at 33rd Design Automation Conference, June 1996
- Distinguished McKnight University Professorship (2000-)
- Judge, IEEE Fellow Selection Committee (1998-2000)
- IEEE Circuits and Systems Society Distinguished Lecturer (1996-1997)(2019-2020)
- McKnight - Land Grant Professorship at the Univ. of Minnesota, 1992 - 1994
- Eliahu Jury Award (for excellence in systems research), 1987, U.C. Berkeley
- Demetri Angelakos Award (for altruistic activities afforded fellow graduate students), 1987, U.C. Berkeley
- IBM Graduate Fellowship, 1987-88
- U.C. Regents Fellowship, 1986-87

Patents

1. R.A. Freking and K.K. Parhi, "Fast and Small Serial Variable Length Encoder with an Optimally High Rate for Encoding Including Huffman Encoding", U.S. Patent Number 6,271,689, August 7, 2001

2. R.A. Freking and K.K. Parhi, "Concurrent Method for Parallel Huffman Compression Coding and Other Variable Length Encoding and Decoding", U.S. Patent Number 6,304,197, October 16, 2001

3. R.A. Freking and K.K. Parhi, "Fast and Small Serial Huffman Decoder for Decoding at an Optimally High Rate", U.S. Patent Number 6,307,489, October 23, 2001

4. W. Freking and K.K. Parhi, "Fast Parallel cascaded Array Modular Multiplier", U.S. Patent Number 6,892,215, Issued May 10, 2005

5. K.K. Parhi, "System and Method for Generating Cyclic Codes for Error Control in Digital Communications", US Patent Number 6,895,545, Issued May 17, 2005

6. W. Freking and K.K. Parhi, "Systolic Cylindrical Array Modular Multiplier", US Patent Numbber 6,907,440, Issued June 14, 2005

7. K.K. Parhi, J.G. Chung, and K.J. Cho, "Low-Error Fixed-Width Modified Booth Multiplier", US Patent Number 6,978,426, Issued December 20, 2005

8. W. Freking and K.K. Parhi, "Systolic Ring Planarized Cylindrical Array Modular Multiplier", US Patent 7,010,561, Issued March 7, 2006

9. K.K. Parhi, "Pipelined Add-Compare-Select Circuits and Methods, and Applications there of", US Patent 7,020,831, Issued March 28, 2006

10. K.K. Parhi, J.-G. Chung and S.-M. Kim, "Low-Error Canonic-Signed-Digit Fixed-Width Multiplier, and Method for Designing Same", US Patent 7,080,115, Issued July 18, 2006

11. T. Zhang and K.K. Parhi, "LDPC Code and Encoder/Decoder Regarding Same", US Patent 7,120,856, Issued Oct. 10, 2006

12. Z. Wang and K.K. Parhi, "Area-Efficient Parallel Turbo Decoding", US Patent 7,200,799, Issued April 3, 2007

13. K.K. Parhi, "Pipelining of Multiplexor Loops in a Digital Circuit", US Patent 7,239,652, Issued July 3, 2007

14. K.K. Parhi and J. Kong, "Low-Latency Architectures for High-Throughput Viterbi Decoders", US Patent 7,308,640, Issued December 11, 2007

15. K.K. Parhi, "Pipelined Parallel Processing of Feedback Loops in a Digital Circuit", US Patent 7,333,580, Issued Feb. 19, 2008

16. K.K. Parhi, J.-G. Chung, K.-C. Lee, K.-J. Cho, "Low-Error Fixed-Width Modified Booth Multiplier," US Patent 7,334,200, Feb. 19, 2008

17. K.K. Parhi, "System and method for generating cyclic codes for error control in digital communications", US Patent 7,539,918, Issued May 26, 2009

18. K.K. Parhi and Y. Gu , "System and Method for MIMO Equalization for DSP Transceivers", US Patent 7,561,633, Issued July 14, 2009

19. A.E. Cohen and K.K. Parhi, "Low-Complexity Hybrid LDPC Code Encoder", US Patent 7,657,816, Issued Feb. 2, 2010

20. Y. Gu and K.K. Parhi, "Parallel Tomlinson Harashima Precoders", US Patent 7,693,233, Issued April 6, 2010

21. S.M. Kim, K.K. Parhi, and R. Liu, "System and Method for Designing RS Based LDPC Code Decoder", US Patent 7716553, Issued May 11, 2010

22. K.K. Parhi and Y. Gu, "High-Speed Precoders for Communications Systems", US Patent 7,769,099, Issued August 3, 2010

23. O.E. Agazzi, G. Ungerboeck, K.K. Parhi, C.A. Lutkemeyer, P. Vorenkamp, K.T. Chan, and M.H. Wakayama, "System and method for high speed communications using digital signal processing", Us Patent 7,933,341, Issued April 26, 2011

24. K.K. Parhi and Y. Gu, "System and Method for Low-Power Echo and NEXT Cancellers", US Patent 8,009,823, Issued August 30, 2011

25. A. Cohen and K.K. Parhi, "System for Secure Variable Data Rate Transmission", US Patent 8,416,948, Issued April 9, 2013

26. O.E. Agazzi, G. Ungerboeck, K.K. Parhi, C.A. Lutkemeyer, P. Vorenkamp, K.T. Chan, and M.H. Wakayama, "System and method for high speed communications using digital signal processing", US Patent 8,422,591, Issued April 16, 2013

27. J. Chen and K.K. Parhi "System for MIMO equalization of multi-channel transceivers with precoding," US Patent 8,498,343, Issued July 30, 2013

28. J. Chen and K.K. Parhi, "System for Low-Complexity Adaptive Echo and NEXT Cancellers", US Patent 8,600,039, Issued Dec. 3, 2013

29. J. Chen and K.K. Parhi, "System for FEXT Cancellation of Multi-Channel Transceivers with Precoding", US Patent 8,699,551, Issued April 15, 2014

30. Y. Lao, K.K. Parhi and C.H. Kim, "Robust Device Authentication," US Patent 10,235,517, Issued March 19, 2019

IEEE 802.3 Standards Presentations

1. K.K. Parhi, C. Lutkemeyer, A. Abnous and M. Hatamian, "Parallel Implementation of the DSP Functions of the PAM-5 10 Gb/s Transceiver", IEEE 802 Plenary meeting, March 2000, http://grouper.ieee.org/groups/802/3/ae/public/mar00/parhi_1_0300.pdf

2. O. Agazzi, V. Gopinathan, K. Parhi, K. Kota, A. Phanse, "DSP Based Equalization for Optical Channels", http://grouper.ieee.org/groups/802/3/ae/public/sep00/agazzi_1_0900.pdf

3. K.K. Parhi and Y. Gu, "Interleaved Trellis Coded Modulation and Decoding", http://grouper.ieee.org/groups/802/3/10GBT/public/jul03/parhi_1_0703.pdf

4. K.K. Parhi and Y. Gu, "Pipelining Tomlinson Harashima Precoders", http://grouper.ieee.org/groups/802/3/an/public/sep04/parhi_1_0904.pdf

Books

1. N.R. Shanbhag, and K.K. Parhi, *Pipelined Adaptive Digital Filters*, Kluwer Academic Publishers, 1994

2. R.I. Hartley, and K.K. Parhi, *Digit-Serial Computation*, Kluwer Academic Publishers, 1995

3. T. Nishitani and K.K. Parhi, ed., *VLSI Signal Processing VIII*, IEEE Press, 1995

4. J.-G. Chung and K.K. Parhi, *Pipelined Lattice and Wave Digital Recursive Filters*, Kluwer Academic Publishers, 1996

5. J. Fortes, C. Mongenet, K. Parhi, and V. Taylor, Ed., *Proceedings 1996 International Conference on Application Specific Systems, Architectures, and Processors*, IEEE Computer Society Press, 1996

6. K.K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley, NY 1999

7. K.K. Parhi and T. Nishitani, Ed., *Digital Signal processing for Multimedia Systems*, Marcel Dekker, NY, 1999

Book Chapters

1. K.K. Parhi, "Parallel Processing and Pipelining in Huffman Decoder", (Chapter 12) in *VLSI Implementations for Image Communications*, Series Advances in Image Communications (Edited by Peter Pirsch), **Vol. 2**, Elsevier Science Publisher, Amsterdam, 1993, pp. 365-395

2. K.K. Parhi, "VLSI For Signal Processing: Special Architectures", in *The Electrical Engineering Handbook*, edited by Richard C. Dorf, CRC Press, 1993, pp. 370-384 (Chapter 17, Section 17.1)

3. C.Y. Wang, and K.K. Parhi, "The MARS High-Level DSP Synthesis System", in *VLSI Design Methodologies for Digital Signal Processing Architectures*, edited by M. Bayoumi, pp. 169-205, Kluwer Academic Press, 1994

4. K.K. Parhi, "High-Level Transformations for DSP Synthesis", Chapter 8.1 in *Microsystems Technology for Multimedia Applications: An Introduction*, edited by B. Sheu *et al.*, IEEE ISCAS-95 Tutorial Book, pp. 575-587, IEEE Press, 1995

5. N.R. Shanbhag and K.K. Parhi, "Pipelined Adaptive Digital Filters", Chapter 8.2 in *Microsystems Technology for Multimedia Applications: An Introduction*, edited by B. Sheu *et al.*, IEEE ISCAS-95 Tutorial Book, pp. 589-601, IEEE Press, 1995

6. C.-Y. Wang and K.K. Parhi, "High-Level DSP Synthesis", Chapter 8.4 in *Microsystems Technology for Multimedia Applications: An Introduction*, edited by B. Sheu *et al.*, IEEE ISCAS-95 Tutorial Book, pp. 615-627, IEEE Press, 1995

7. K.K. Parhi and F. Catthoor, "Design of High-Performance DSP Systems", Chapter in *Emerging Technologies: Designing Low-Power Digital Systems*, Edited by R. Cavin and W. Liu, pp. 447-507, IEEE Press (ISCAS-96 Tutorial Book)

8. K.K. Parhi, "Low-Power Digital VLSI Approaches", Chapter in *Circuits and Systems in the Information Age*, Edited by Y. Huang and C. Wei, pp. 3-22, IEEE Press, June 1997 (ISCAS-97 Tutorial Book)

9. K.K. Parhi, "Video Compression", *Chapter 2 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 17-41, Marcel Dekker, New York, 1999

10. T.C. Denk and K.K. Parhi, "Wavelet VLSI Architectures", *Chapter 13 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 329-353, Marcel Dekker, New York, 1999

11. K.J. Raghunath and K.K. Parhi, "Pipelined RLS for VLSI: STAR-RLS Filters", *Chapter 19 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 519-550, Marcel Dekker, New York, 1999

12. H.R. Srinivas and K.K. Parhi, "Division and Square-Root", *Chapter 20 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 551-587, Marcel Dekker, New York, 1999

13. L. Song and K.K. Parhi, "Finite Field Arithmetic Architectures", *Chapter 21 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 589-621, Marcel Dekker, New York, 1999

14. J.H. Satyanarayana and K.K. Parhi, "Power Estimation Approaches", *Chapter 25 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 741-772, Marcel Dekker, New York, 1999

15. J.P. Ma and K.K. Parhi, "On Pipelined Implementations of QRD-RLS Adaptive Filters", *Chapter in QRD-RLS Adaptive Filters*, Edited by J.A. Apolinario, Jr., pp. 269-297, Springer-Verlag, 2009

16. K.K. Parhi and Y. Chen, "Signal Flow Graphs and Data Flow Graphs", *Handbook of Signal Processing Systems*, Vol. 4, Edited by S.S. Bhattacharyya, E.F. Deprettere, R. Leupers and J. Takala, pp. 791-816, Springer-Verlag, 2010

17. H.A. Patil, A.E. Cohen, and K.K. Parhi, "Speaker Identification over Narrowband VoIP Networks", *Chapter 6 in Advances in Forensic Speaker Recognition: Criminal Justice and Counterterrorism*, Edited by A. Neustein and H. Patil, Springer Science+Business Media LLC, 2011, pp. 125-151

18. V. Kulkarni, H. Jiang, E. Kharisov, N. Hovakimyan, M. Riedel, K. Parhi, "Synchronous Sequential Computations with Biomolecular Reactions," *Chapter 14 in Systems and Synthetic Biology Book*, Edited by V. Singh and P. K. Dhar, Springer Verlag, Netherlands, 2015, pp. 255-279

19. S. Roychowdhury, D. Koozekanani, M. Reinsbach and K.K. Parhi, "Automated OCT Segmentation for Images with DME," Chapter 4 in *Medical Image Analysis and Informatics: Computer-aided Diagnosis and Therapy*, edited by P.M. de Azevedo-Marques, A. Mencattini, M. Salmeri, and R. M. Rangayyan, CRC Press, pp. 85-102, 2017

Journal Publications

1. K.K. Parhi and D.G. Messerschmitt, "Concurrent Cellular VLSI Adaptive Filter Architectures", *IEEE Transactions on Circuits and Systems*, **Vol. CAS-34**, No. 10, October 1987, pp. 1141-1151

2. K.K. Parhi and R.S. Berkowitz, "On Optimizing Importance Sampling Simulations", *IEEE Transactions of Circuits and Systems*, **Vol. CAS-34**, No. 12, December 1987, pp. 1558-1563

3. K.K. Parhi, and D.G. Messerschmitt, "Concurrent Architectures for Two-Dimensional Recursive Digital Filtering", *IEEE Trans. on Circuits and Systems*, **Vol. CAS-36(6)**, June 1989, pp. 813-829

4. K.K. Parhi, and D.G. Messerschmitt, "Pipeline Interleaving and Parallelism in recursive Digital Filters, Part I: Pipelining using Scattered Look-Ahead and Decomposition", *IEEE Transactions on Acoustics, Speech, and Signal Processing*, **Vol. 37(7)**, July 1989, pp. 1099-1117

5. K.K. Parhi, and D.G. Messerschmitt, "Pipeline Interleaving and Parallelism in recursive Digital Filters, Part II: Pipelined Incremental Block Filtering", *IEEE Transactions on Acoustics, Speech, and Signal Processing*, **Vol. 37(7)**, July 1989, pp. 1118-1135

6. K.K. Parhi, "Algorithm Transformation Techniques for Concurrent Processors", *Proceedings of the IEEE*, Special Issue on Supercomputer Technology, **Vol. 77(12)**, December 1989, pp. 1879-1895

7. K.K. Parhi, and D.G. Messerschmitt, "Static Rate-Optimal Scheduling of Iterative Data Flow Programs via Optimum Unfolding", *IEEE Trans. on Computers*, **Vol. 40(2)**, February 1991, pp. 178-195

8. K.K. Parhi, "A Systematic Approach for Design of Digit-Serial Signal Processing Architectures", *IEEE Trans. on Circuits and Systems*, **Vol. 38**, No. 4, April 1991, pp. 358-375

9. K.K. Parhi, "Pipelining In Dynamic Programming Architectures", *IEEE Trans. on Signal Processing*, **Vol. 39**, No. 6, June 1991, pp. 1442-1450

10. K.K. Parhi, "Finite Word Effects in Pipelined Recursive Filters", *IEEE Trans. on Signal Processing*, **Vol. 39**, No. 6, June 1991, pp. 1450-1454

11. K.K. Parhi, "Pipelining in Algorithms with Quantizer Loops", *IEEE Trans. on Circuits and Systems*, **Vol. 38**, No. 7, July 1991, pp. 745-754

12. K.K. Parhi, "Technology for the 90s: VLSI Signal and Image Processing Systems", *IEEE Circuits and Devices Magazine* (special technology forecast issue), **7**(4), July 1991 (invited article), pp. 16-17

13. K.K. Parhi, "Research on VLSI For Digital Video Systems in Japan", *Asian Scientific Information Bulletin of the Office of Naval Research Office*, **16**(4), October - December 1991, pp. 93-98

14. K.K. Parhi, C.Y. Wang, A.P. Brown, "Synthesis of Control Circuits in Folded Pipelined DSP Architectures", *IEEE Journal of Solid State Circuits*, **Vol. 27**, No. 1, January 1992, pp. 29-43

15. M. Hatamian and K.K. Parhi, "An 85-MHz Fourth-Order Programmable IIR Digital Filter Chip", *IEEE Journal of Solid State Circuits*, **Vol. 27**, No. 2, February 1992, pp. 175-183

16. H.R. Srinivas, and K.K. Parhi, "High-Speed VLSI Arithmetic Processor Architectures Using Hybrid Number Representation", *Journal of VLSI Signal Processing*, **Vol. 4**, No. 2/3, 1992, pp. 177-198

17. H.R. Srinivas, and K.K. Parhi, "A Fast VLSI Adder Architecture", *IEEE Journal of Solid State Circuits*, **Vol. 27**, No. 5, May 1992, pp. 761-767

18. K.K. Parhi, "High-Speed VLSI Architectures for Huffman and Viterbi Decoders", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **Vol. 39**, No. 6, June 1992, pp. 385-391

19. K.K. Parhi, "Video Data Format Converters Using Minimum Number of Registers", *IEEE Transactions on Circuits and Systems For Video Technology*, **Vol. 2**, No. 2, June 1992, pp. 255-267

20. K.K. Parhi, "Systematic Synthesis of DSP Data Format Converters using Life-Time Analysis and Forward-Backward Register Allocation", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **Vol. 39**, No. 7, July 1992, pp. 423-440

21. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Differential Vector Quantizer for Low-Power Speech Coding Applications", *IEEE Transactions on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **40**(5), May 1993, pp. 347-349

22. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Lattice Filter Architecture", *IEEE Trans. on Signal Processing*, **41**(5), May 1993, pp. 1925-1939

23. K.J. Raghunath, and K.K. Parhi, "Parallel Adaptive Decision Feedback Equalizers", *IEEE Transactions on Signal Processing*, **41**(5), May 1993, pp. 1956-1961

24. K.K. Parhi, and T. Nishitani, "VLSI Architectures for Discrete Wavelet Transforms", *IEEE Trans. on VLSI Systems*, **1**(2), June 1993, pp. 191-202

25. L.E. Lucke, and K.K. Parhi, "Data-Flow Transformations for Critical Path Time Reduction For High-Level DSP Synthesis", *IEEE Transactions on Computer Aided Design of Integrated Circuits And Systems*, **12**(7), July 1993, pp. 1063-1068

26. N.R. Shanbhag, and K.K. Parhi, "Relaxed Look-Ahead Pipelined LMS Adaptive Filters and Their Application to ADPCM Coder", *IEEE Transactions on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **Vol. 40**(12), December 1993, pp. 753-766

27. K.K. Parhi, F.H. Wu, and K. Ganesan, "Sequential and Parallel Neural Network Vector Quantizers", *IEEE Transactions on Computers*, **43**(1), pp. 104-109, January 1994

28. J.-G. Chung, and K.K. Parhi, "Pipelining of Lattice IIR Digital Filters", *IEEE Transactions on Signal Processing*, **42**(4), pp. 751-761, April 1994

29. L.E. Lucke, and K.K. Parhi, "Parallel Processing Architectures for Rank-Order and Stack Filters", *IEEE Transactions on Signal Processing*, **42**(5), pp. 1178-1189, May 1994

30. N.R. Shanbhag, and K.K. Parhi, "Finite Precision Analysis of the ADPCM Coder", *IEEE Transactions on Circuits and Systems-Part II: Analog and Digital Signal Processing*, **41**(5), pp. 364-368, May 1994

31. K.K. Parhi, "Calculation of Minimum Number of Registers in Arbitrary Life Time Chart", *IEEE Circuits and Systems Transactions - Part II: Analog and Digital Signal Processing*, **41**(6), pp. 434-436, June 1994

32. N.R. Shanbhag, and K.K. Parhi, "Corrections to "Finite Precision Analysis of the ADPCM Coder"", *IEEE Transactions on Circuits and Systems-Part II: Analog and Digital Signal Processing*, **41**(7), pp. 493, July 1994

33. G.B. Adams III, E.J. Coyle, L. Lin, L.E. Lucke, and K.K. Parhi, "Input Compression and Efficient VLSI Architectures for Rank-Order and Stack Filters", *Signal Processing*, **38**, pp. 441-453, August 1994

34. H.R. Srinivas, B. Vinnakota, and K.K. Parhi, "A C-Testable Carry-Free Divider", *IEEE Trans. on VLSI Systems*, **2**(4), pp. 472-488, December 1994

35. K.K. Parhi, "High-Level Algorithm and Architecture Transformations for DSP Synthesis", *Journal of VLSI Signal Processing*, **9**(1), pp. 121-143, January 1995

36. C.-Y. Wang, and K.K. Parhi, "High-Level DSP Synthesis using Concurrent Transformations, Scheduling, and Allocation", *IEEE Transactions on Computer Aided Design*, **14**(3), pp. 274-295, March 1995

37. J.-G. Chung, and K.K. Parhi, "Scaled Normalized Lattice Digital Filters", *IEEE Transactions on Circuits and Systems - Part II: Analog and Digital Signal Processing*, **42**(4), pp. 278-282, April 1995

38. N.R. Shanbhag, and K.K. Parhi, "Pipelined Adaptive DFE Architectures using Relaxed Look-Ahead", *IEEE Trans. on Signal Processing*, **43(6)**, pp. 1368-1385, June 1995

39. H.R. Srinivas, and K.K. Parhi, "A Fast Radix-4 Division Algorithm", *IEEE Transactions on Computers*, **44**(6), pp. 826-831, June 1995

40. J.-G. Chung, H. Kim and K.K. Parhi, "Pipelined Lattice WDF Design for Wideband Filters", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **42**(9), pp. 616-618, September 1995

41. C.-Y. Wang, and K.K. Parhi, "Resource Constrained Loop List Scheduler for DSP Algorithms", *Journal of VLSI Signal Processing*, **11**(1/2), pp. 75-96, October 1995

42. K. Ito and K.K. Parhi, "Determining the Minimum Iteration Period of an Algorithm", *Journal of VLSI Signal Processing*, **11**(3), pp. 229-244, December 1995

43. T.C. Denk and K.K. Parhi, "Lower Bounds on Memory Requirements for Statically Scheduled DSP Programs", *Journal of VLSI Signal Processing*, **12**(3), pp. 247-264. June 1996

44. K.J. Raghunath, and K.K. Parhi, "Pipelined RLS Adaptive Filtering using Scaled Tangent Rotations (STAR)", *IEEE Transactions on Signal Processing*, **44**(10), pp. 2591-2604, October 1996

45. H.R. Srinivas, K.K. Parhi, and L. Montalvo, "Radix-2 Division with Over-Redundant Quotient Selection", *IEEE Trans. on Computers*, **46**(1), pp. 85-92, Jan. 1997

46. T.C. Denk and K.K. Parhi, "VLSI Architectures for Lattice Structure Based Orthonormal Discrete Wavelet Transforms", *IEEE Transactions on Circuits and Systems, Part - II: Analog and Digital Signal Processing*, **44**(2), pp. 129-132, Feb. 1997

47. B. Fu and K.K. Parhi, "Generalized Multiplication Free Arithmetic Codes", *IEEE Transactions on Communications*, **45**(5), pp. 497-501, May 1997

48. K.J. Raghunath and K.K. Parhi, "Finite Precision Error Analysis of QRD-RLS and STAR-RLS Adaptive Filters", *IEEE Transactions on Signal Processing*, **45**(5), pp. 1193-1209, May 1997

49. K. Ito and K.K. Parhi, "A Generalized Technique for Register Counting and its Application to Cost-Optimal DSP Architecture Synthesis", *Journal of VLSI Signal Processing*, **16**(1), pp. 57-72, May 1997

50. J.H. Satyanarayana and K.K. Parhi, "A Theoretical Approach to Estimation of Bounds on Power Consumption in Digital Multipliers", *IEEE Transactions on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **44**(6), pp. 473-481, June 1997

51. D.A. Parker and K.K. Parhi, "Low Area/Power Parallel FIR Digital Filter Implementations", *Journal of VLSI Signal Processing*, **17**(1), pp. 75-92, Sept. 1997

52. Y. Li and K.K. Parhi, "STAR Recursive Least Square Lattice Adaptive Filters", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **44**(12), pp. 1040-1054, December 1997

53. S. Jain, L. Song and K.K. Parhi, "Efficient Semi-Systolic VLSI Architectures for Finite Field Arithmetic", *IEEE Trans. on VLSI Systems*, **6**(1), pp. 101-113, March 1998

54. M. Majumdar and K.K. Parhi, "Synthesis of Low-Area Data Format Converters", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **45**(4), pp. 504-508, April 1998

55. L. Song and K.K. Parhi, "Low-Energy Digit-Serial/Parallel Finite Field Multipliers", *Journal of VLSI Signal Processing*, **19**(2), pp. 149-166, June 1998

56. T.C. Denk and K.K. Parhi, "Exhaustive Scheduling and Retiming of Digital Signal Processing Systems", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **45**(7), pp. 821-838, July 1998

57. Y.-N. Chang, C.Y. Wang, and K.K. Parhi, "Loop-List Allocation and Scheduling with using Heterogeneous Functional Units", *Journal of VLSI Signal Processing*, **19**(3), pp. 243-256, Aug. 1998

58. L. Montalvo, K.K. Parhi, and A. Guyot, "New Svoboda-Tung Division", *IEEE Trans. on Computers*, **47**(9), pp. 1014-1020, Sept. 1998

59. K. Ito, L.E. Lucke and K.K. Parhi, "ILP Based Cost-Optimal DSP Synthesis with Module Selection and Data Format Conversion", *IEEE Trans. on VLSI Systems*, **6**(4), pp. 582-594, Dec. 1998

60. T.C. Denk and K.K. Parhi, "Synthesis of Folded Pipelined Architectures for Multirate DSP Algorithms", *IEEE Trans. on VLSI Systems*, **6**(4), pp. 595-607, Dec. 1998

61. Y.-N. Chang, J.H. Satyanarayana and K.K. Parhi, "Systematic Design of High-Speed and Low-Power Digit-Serial Multipliers", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **45**(12), pp. 1585-1596, Dec. 1998

62. H.R. Srinivas and K.K. Parhi, "A Floating Point Radix 2 Shared Division/Square-Root Chip", *Journal of VLSI Signal Processing*, **21**(1), pp. 37-60, May 1999

63. T.C. Denk and K.K. Parhi, "Two-Dimensional Retiming", *IEEE Trans. on VLSI Systems*, **7**(2), pp. 198-211, June 1999

64. A.F. Shalash and K.K. Parhi, "Multi-Dimensional Carrierless AM/PM Systems for Digital Subscriber Loops", *IEEE Trans. on Communications*, **47**(11), pp. 1655-1667, Nov. 1999

65. K.K. Parhi, "Low-Energy CSMT Carry-Generators and Binary Adders", *IEEE Trans. on VLSI Systems*, **7**(4), pp. 450-462, Dec. 1999

66. J.H. Satyanarayana and K.K. Parhi, "Theoretical Analysis of Word-Level Switching Activity in the Presence of Glitching and Correlation", *IEEE Trans. on VLSI Systems*, **8**(2), pp. 148-159, Apr. 2000

67. L. Song, K.K. Parhi, I. Kuroda, T. Nishitani, "Hardware/Software Codesign of Finite Field Datapath for Low-Energy Reed-Solomon Codecs", *IEEE Trans. on VLSI Systems*, **8**(2), pp. 160-172, Apr. 2000

68. J. Satyanarayana and K.K. Parhi, "Power Estimation of Digital Datapaths using HEAT Tool", *IEEE Design and Test Magazine*, **17**(2), pp. 101-110, April-June 2000

69. Y.-N. Chang, H. Suzuki and K.K. Parhi, "A 2 Mb/s 256-State 10 mW Rate-1/3 Viterbi Decoder", *IEEE Journal of Solid State Circuits*, **Vol. 35**, No. 6, pp. 826-834, June 2000

70. J.G. Chung, H. Kim and K.K. Parhi, "Angle-Constrained IIR Filter Pipelining for Reduced Roundoff Errors", *IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing*, **47**(6), pp. 555-559, June 2000

71. Y.-N. Chang and K.K. Parhi, "High-Performance Digit-Serial Complex Multiplier", *IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing*, **47**(6), pp. 570-572, June 2000

72. A. Shalash and K.K. Parhi, "Power-Efficient Folding of Pipelined LMS Adaptive Filters with Applications to Wireline Digital Communications", *Journal of VLSI Signal Processing*, **25**(3), pp. 199-213, July 2000

73. J. Ma, K.K. Parhi and E.F. Deprettere, "Annihilation-Reordering Look-Ahead Pipelined CORDIC Based RLS Adaptive Filters and Their Application to Adaptive Beamforming", *IEEE Trans. on Signal Processing*, **48**(8), pp. 2414-2431, Aug. 2000

74. J. Ma, K.K. Parhi, G.J. Hekstra and E.F. Deprettere, "Efficient Implementations of Pipelined CORDIC Based IIR Digital Filters using Fast Orthonormal Micro-rotations", *IEEE Trans. on Signal Processing*, **48**(9), pp. 2712-2716, Sep. 2000

75. J. Ma, K.K. Parhi and E.F. Deprettere, "Pipelined CORDIC Based Cascade Orthogonal IIR Digital Filters", *IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing*, **47**(11), pp. 1238-1253, Nov. 2000

76. L. Gao and K.K. Parhi, "Hierarchical Pipelining and Folding of QRD-RLS Adaptive Filters and Its Application to Digital Beamforming", *IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing*, **47**(12), pp. 1503-1519, Dec. 2000

77. J. Ma, K.K. Parhi and E.F. Deprettere, "A Unified Algebraic Transformation Approach for Parallel Recursive and Adaptive Filtering and SVD Algorithms", *IEEE Trans. on Signal Processing*, **49**(2), pp. 424-437, Feb. 2001

78. M. Kuhlmann and K.K. Parhi, "A Novel Low-Power Shared Division and Square-Root using the GST Algorithm", *VLSI Design*, **12**(3), pp. 365-376, 2001

79. M.E. Zervakis, V. Sundararajan and K.K. Parhi, "Vector Processing of Wavelet Coefficients for Robust Image Denoising", *Journal of Image and Vision Computing*, Elsevier, **19**(7), pp. 435-450, May 2001

80. T. Zhang and K.K. Parhi, "A Novel Systematic Design Approach for Mastrovito Multipliers over GF(2^m)", *IEEE Trans. on Computers*, **50**(7), pp. 734-749, July 2001

81. Z. Chi, J. Ma and K.K. Parhi, "Hybrid Annihilation Transformation (HAT) for Pipelining QRD Based Least Square Adaptive Filters", *IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing*, **48**(7), pp. 661-674, July 2001

82. K.K. Parhi, "Approaches to Low-Power Implementation of DSP Systems", *IEEE Trans. on Circuits and Systems, Part-I: Fundamental Theory and Applications*, pp. 1214-1224, **48**(10), October 2001

83. Z. Wang, H. Suzuki and K.K. Parhi, "VLSI Implementation of Turbo/MAP Decoders", *Journal of VLSI Signal Processing Systems*, **29**(3), pp. 209-222, November 2001

84. W.L. Freking and K.K. Parhi, "Performance-Scalable Array Architectures for Modular Multiplication", *Journal of VLSI Signal Processing Systems*, **31**(2), pp. 101-116, April 2002

85. V. Sundararajan, S. Sapatnekar and K.K. Parhi, "Fast and Exact Transistor Sizing Based on Iterative Relaxation", *IEEE Trans. on CAD*, **21**(5), pp. 568-581, May 2002

86. M. Kuhlmann and K.K. Parhi, "P-CORDIC: A Precomputation Based CORDIC Algorithm for the Circular Mode", *Eurasip Journal on Applied Signal Processing*, Vol. **2002**, No. 9, pp. 436-443, 2002

87. J.G. Chung and K.K. Parhi, "Frequency spectrum based low-area low-power parallel FIR filter design", *Eurasip Journal on Applied Signal Processing*, Vol. **2002**, No. 9, pp. 444-453, 2002

88. J. Valls, M. Kuhlmann, K.K. Parhi, "Evaluation of CORDIC Algorithms for FPGA design", *Journal of VLSI Signal Processing*, Vol. **32**(3), pp. 207-222, Nov. 2002

89. X. Zhang and K.K. Parhi, "Hardware Implementation of Advanced Encryption Standard Algorithm", *IEEE CAS Magazine*, **2**(4), pp. 24-46, Dec. 2002

90. Z. Wang, Z. Chi and K.K. Parhi, "Area-Efficient High Speed Decoding Schemes for Turbo/MAP Decoders", *IEEE Trans. on VLSI Systems*, **10**(6), Dec. 2002

91. Z. Wang and K.K. Parhi, "On-Line Extraction of Soft Decoding Information and its Applications in VLSI Turbo Codes", *IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing*, **49**(12), pp. 760-769, Dec. 2002

92. I. Ben Dhaou, K.K. Parhi and H. Tenhunen, "Energy Efficient Signaling in DSM Technology", *VLSI Design: Special Issue on Timing Analysis and Optimization for Deep Sub-Micron ICs*, Vol. **15**(3), pp. 563-586, 2002

93. T. Sansaloni, J. Valls and K.K. Parhi, "Digit-Serial Complex Number Multipliers on FPGAs", *Journal of VLSI Signal Processing*, Vol. **33**(1), pp. 101-115, Jan. 2003

94. Z. Wang and K.K. Parhi, "Performance Improvement and Implementation Issues of Turbo/SOVA Decoders", *IEEE Trans. on Communications*, Vol. **51**(4), pp. 570-579, April 2003

95. T. Zhang and K.K. Parhi, "An FPGA Implementation of (3,6) Regular Low-Density Parity-Check Code Decoder", *Eurasip Journal on Applied Signal Processing*, **2003**(6), pp. 530-542, May 2003

96. V. Sundararajan and K.K. Parhi, "Synthesis of Minimum Area Folded Architectures for Multi-Dimensional Multirate DSP Systems", *IEEE Trans. on Signal Processing*, **51**(6), pp. 1954-1965, June 2003

97. Y.-N. Chang and K.K. Parhi, "An Efficient Pipelined FFT Implementation", *IEEE Trans. on Circuits and Systems: Part-II: Analog and Digital Signal Processing*, *Vol. 50*(6), pp. 322-325, June 2003

98. B. Sahoo and K.K. Parhi, "A Low Power Correlator for CDMA Wireless Systems", *Journal of VLSI Signal Processing*, **35**(1), pp. 105-112, August 2003

99. L. Gao, K.K. Parhi and J. Ma, "Relaxed Annihilation-Reordering Look-Ahead QRD-RLS Adaptive Filters", *Journal of VLSI Signal Processing*, *Vol. 35*(2), pp. 119-136, Sept. 2003

100. J. Kong and K.K. Parhi, "Interleaved Convolutional Code and its Viterbi Decoder Architecture", *EURASIP Journal on Applied Signal Processing*, *Vol. 2003*(13), pp. 1328-1324, 2003

101. Y. Chen and K.K. Parhi, "Reduced Complexity Decoding Algorithms for Space-Time Block Turbo Coded System", *EURASIP Journal on Applied Signal Processing*, *Vol. 2003*(13), pp. 1335-1345, 2003

102. S.-M. Kim, J.-G. Chung and K. K. Parhi, "Low error CSD Fixed-Width Multiplier with Efficient Sign Extension", *IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing*, **50**(3), pp. 984-993, December 2003

103. Z. Chi, L. Song and K.K. Parhi, "On the Performance, Complexity Tradeoffs of Block Turbo Decoder Design", *IEEE Communications Letters*, Vol. 52, No. 2, pp. 173-175, Feb. 2004

104. K.K. Parhi, "An Improved Pipelined MSB-First Add-Compare-Select Unit Structure for Viterbi Decoders", *IEEE Trans. on Circuits and Systems, Part-I: Regular Papers*, **51**(3), pp. 504-511, March 2004

105. K. K. Parhi, "Eliminating the Fanout Bottleneck in Parallel Long BCH Encoders", *IEEE Trans. on Circuits and Systems, Part-I: Regular Papers*, **51**(3), pp. 512-516, March 2004

106. T. Zhang and K.K. Parhi, "Joint (3,k)-regular LDPC Code and Decoder/Encoder Design", *IEEE Trans. Signal Processing*, **52**(4), pp. 1065-1079, April 2004

107. K.-J. Cho, K.-C. Lee, J.-G. Chung, and K.K. Parhi, "Design of Low-Error Fixed Width Modified Booth Multiplier", *IEEE Trans. on VLSI Systems*, **12**(5), pp. 522-531, May 2004

108. J. Kong and K.K. Parhi, "Low-Latency Architectures for High-Throughput Viterbi Decoders", *IEEE Trans. on VLSI Systems*, **12**(6), pp. 642-651, June 2004

109. Y. Chen and K.K. Parhi, "Small Area Parallel Chien search Architectures for Long BCH Codes", *IEEE Trans. on VLSI Systems*, **12**(5), pp. 545-549, May 2004

110. Y. Chen and K.K. Parhi, "Overlapped Message Passing of Quasi-Cyclic Low-Density Parity Check Codes", *IEEE Trans. on Circuits and Systems, Part-I: Regular Papers*, **51**(6), pp. 1106-1113, June 2004

111. J. Ma and K.K. Parhi, "Pipelined CORDIC Based State-Space Orthogonal Recursive Digital Filters using Matrix Look-Ahead", *IEEE Trans. Signal Processing*, **52**(7), pp. 2102-2119, July 2004

112. V. Sundararajan, S. Sapatnekar and K.K. Parhi, "A New Approach for Integration of Min-Area Retiming and Min-Delay Padding for Simultaneously Addressing Short Path and Long Path constraints. *ACM Trans. on TODAES*, **9**(3), pp. 273-289, July 2004

113. C. Cheng and K.K. Parhi, "Hardware Efficient Fast Parallel FIR Filter Structures Based on Iterated Short Convolution", *IEEE Trans. on Circuits and Systems, Part-I: Regular Papers*, **51**(8), pp. 1492-1500, Aug. 2004

114. X. Zhang and K.K. Parhi, "High-Speed VLSI Architectures for the AES Algorithm", *IEEE Trans. on VLSI Systems*, **12**(9), pp. 957-967, Sep. 2004

115. Y. Chen and K.K. Parhi, "On the Performance and Implementation Issues of Interleaved Single Parity Check Turbo Product Codes" *Journal of VLSI Signal Processing Systems*, **35**(1), Jan. 2005

116. Z. Chi, Z. Wang and K.K. Parhi, "On the Better Protection of Short Frame Turbo Codes", *IEEE Trans. on Communications*, **52**(9), pp. 1435-1439, Sept. 2004

117. X. Zhang and K.K. Parhi, "Fast Factorization Architecture in Soft-Decision Reed-Solomon Decoding", *IEEE Trans. on VLSI Systems*, **13**(4), pp. 413-426, Apr. 2005

118. K.K. Parhi, "Design of Multi-Gigabit Multiplexer Loop Based Decision Feedback Equalizers", *IEEE Trans. on VLSI Systems*, **13**(4), pp. 489-493, Apr. 2005

119. C. Cheng and K.K. Parhi, "A Novel Systolic Array Structure for DCT", *IEEE Trans. on Circuits and Systems, Part-II: Express Briefs*, **52**(5), pp. 366-369, July 2005

120. X. Zhang and K.K. Parhi, "High-Speed Architectures for Parallel Long BCH Encoders", *IEEE Trans. on VLSI Systems*, bf 13(7), pp. 872-877, July 2005

121. C. Cheng and K.K. Parhi, "Hardware Efficient Fast Computation of the Discrete Fourier Transform", *Springer Journal of VLSI Signal Processing*, pp. 159-172, **42**(2), Feb. 2006

122. Y. Gu and K.K. Parhi, "Interleaved Trellis Coded Modulation and Decoder Optimizations for 10 Gigabit Ethernet over Copper", *Journal of VLSI Signal Processing Systems*, **42**(3), pp. 211-221, March 2006

123. L. Gao and K.K. Parhi, "Models for Architectural Power and Power Grid Noise Analysis on Data Bus", *Journal of VLSI Signal Processing Systems*, **44**(2), pp. 25-46, August 2006

124. J.-H. Lin and K.K. Parhi, "Parallelization of Context Based Adaptive Binary Arithmetic Coders", *IEEE Trans. on Signal Processing*, **54**(10), pp. 3702-3711, Oct. 2006

125. X. Zhang and K.K. Parhi, "On the Optimum Constructions of Composite Field for the AES Algorithm", *IEEE Trans. Circuits and Systems-II: Express Briefs*, **53**(10), pp. 1153-1157, Oct. 2006

126. C. Cheng and K.K. Parhi, "High-Speed Parallel CRC Implementation Based on Unfolding, Pipelining and Retiming", *IEEE Trans. Circuits and Systems-II: Express Briefs*, **53**(10), pp. 1017-1021, Oct. 2006

127. C. Cheng and K.K. Parhi, "Hardware Efficient Fast DCT Based on Novel Cyclic Convolution Structures", *IEEE Trans. on Signal Processing*, **54**(11), Nov. 2006, pp. 4419-4434

128. K.-J. Cho, J.-S. Park, B.-K. Kim, J.-G. Chung and K.K. Parhi, "Design of a Sample Rate Converter from CD to DAT using Fractional Delay Allpass Filter", *IEEE Trans. on Circuits and Systems, Part-II: Express Briefs*, **54**(1), Jan. 2007, pp. 19-23

129. Y. Gu and K.K. Parhi, "Pipelined Parallel Decision Feedback Decoders (PDFDs) for High-Speed Ethernet over Copper", *IEEE Trans. on Signal Processing*, **55**(2), Feb. 2007, pp. 707-715

130. C. Cheng and K.K. Parhi, "Low Cost Parallel FIR Filter Structures with 2-Stage Parallelism", *IEEE Trans. Circuits and Systems-I: Regular Papers*, **54**(2), Feb. 2007, pp. 280-290

131. C. Cheng and K.K. Parhi, "Low-Cost Fast VLSI Algorithm for Discrete Fourier Transform", *IEEE Trans. Circuits and Systems-I: Regular Papers*, **54**(4), Apr. 2007, pp. 791-806

132. Y. Gu and K.K. Parhi, "High-Speed Architecture Design of Tomlinson-Harashima Precoders", *IEEE Trans. Circuits and Systems-I: Regular Papers*, **54**(9), pp. 1929-1937, Sep. 2007

133. C. Cheng and K.K. Parhi, "High-Throughput VLSI Architecture for FFT Computation", ¡I¿ IEEE Trans. Circuits and Systems-II: Express Briefs¡/I¿, **54**(10), pp. 863-867, Oct. 2007

134. C. Cheng and K.K. Parhi, "High-Speed VLSI Implementation of 2-D Discrete Wavelet Transform", *IEEE Trans. on Signal Processing*, **56**(1), Jan. 2008, pp. 393-403

135. Y. Gu and K.K. Parhi, "Design of Parallel Tomlinson-Harashima Precoders", *IEEE Trans. Circuits and Systems-II: Transactions Briefs*, **55**(5), pp. 447-451, May 2008

136. J. Chen, Y. Gu and K.K. Parhi, "Low Complexity ECHO And NEXT Cancellers for High-Speed Ethernet Transceivers", *IEEE Trans. Circuits and Systems-I: Regular Papers*, **55**(10), pp. 2827-2840, Oct. 2008

137. C. Cheng and K.K. Parhi, "Hardware Efficient Low-Latency Architecture for High Throughput Rate Viterbi Decoders", *IEEE Trans. Circuits and Systems-II: Transactions Briefs*, **55**(12), pp. 1254-1258, Dec. 2008

138. E. Saberinia, J. Tang, A.H. Tewfik, and K.K. Parhi, "Pulsed OFDM Modulation for Ultra Wideband Communications", *IEEE Trans. on Vehicular Technology*, **58**(2), pp. 720-726, Feb. 2009

139. S. Park, K.K. Parhi, and S.-C. Park, "Probabilistic Spherical Detection and VLSI Implementation for Multiple-Antenna Systems", *IEEE Trans. Circuits and Systems-I: Regular Papers*, **56**(3), pp. 685-698, March 2009

140. J. Chen, Y. Gu, and K.K. Parhi, "Novel FEXT Cancellation and Equalization for High Speed Ethernet Transmission", *IEEE Trans. Circuits and Systems-I: Regular Papers*, **56**(6), pp. 1272-1285, June 2009

141. D. Oh and K.K. Parhi, "Low Complexity Decoder Architecture for Low-density Parity-Check Codes", *Journal of VLSI Signal Processing Systems*, **56**, pp. 217-228, June 2009

142. R. Liu and K.K. Parhi, "Low-Latency Low-Complexity Architectures for Viterbi Decoders", *IEEE Trans. Circuits and Systems-I: Regular Papers*, **56**(10), pp. 2315-2324, Oct. 2009

143. A.E. Cohen and K.K. Parhi, "A Low-Complexity Hybrid LDPC Code Encoder for IEEE 802.3an (10GBase-T) Ethernet", *IEEE Trans. Signal Processing*, **57**(10), pp. 4085-4094, Oct. 2009

144. M. Garrido, K.K. Parhi, and J. Grajal, "A Pipelined FFT Architecture for Real-Valued Signals", *IEEE Trans. Circuits and Systems-I: Regular Papers*, **56**(12), pp. 2634-2643, Dec. 2009

145. D. Oh and K.K. Parhi, "Low Complexity Switch Networks for Reconfigurable LDPC Decoders", *IEEE Trans. VLSI Systems*, **18**(1), pp. 85-94, Jan. 2010

146. D. Oh and K.K. Parhi, "Min-Sum Decoder Architecture with Reduced Word-Length for LDPC Codes", *IEEE Trans. Circuits and Systems-I: Regular Papers*, **57**(1), pp. 105-115, Jan. 2010

147. Y. Liu, T. Zhang and K.K. Parhi, "Computation Error Analysis in Digital Signal Processing System with Overscaled Supply Voltage", *IEEE Trans. VLSI Systems*, **18**(4), pp. 517-526, Apr. 2010

148. A.E. Cohen and K.K. Parhi, "Fast Elliptic Curve Cryptography Accleration for GF(2^m) on 32-Bit Processors", *Springer Journal on Signal Processing Systems*, **60**(1), pp. 31-45, July 2010

149. A.E. Cohen and K.K. Parhi, "Secure Variable Data Rate Transmission", *IEEE Trans. Circuits and Systems-II: Transactions Briefs*, **58**(2), pp. 100-104, Feb. 2011

150. M. Ayinala and K.K. Parhi, "High-Speed Parallel VLSI Architectures for Linear Feedback Shift Registers", *IEEE Trans. Signal Processing*, **59**(9), pp. 4459-4469, Sept. 2011

151. Y. Park, L. Luo, K.K. Parhi and T. Netoff, "Seizure Prediction with Spectral Power of EEG Using Cost-Sensitive Support Vector Machines", *Epilepsia*, **52**(10), pp. 1761-1770, Oct. 2011

152. R. Liu and K.K. Parhi, "Power Reduction in Frequency-Selective FIR Filters under Voltage Overscaling", *IEEE J. of Emerging Technologies in Circuits and Systems (JETCAS)*, **1**(3), pp. 343-356, Sept. 2011

153. A.E. Cohen and K.K. Parhi, "Architectures for RSA Cryptosystems: A Tutorial", *IEEE Circuits and Systems Magazine*, **11**(4), Nov. 2011

154. A.E. Cohen, J. Lin and K.K. Parhi, "Variable Data Rate (VDR) Network Congestion Control", *Elsevier Computer Networks Journal*, **56**(4), pp. 1343-1356, March 2012

155. H. Jiang, M. Riedel, and K.K. Parhi, "Digital Signal Processing with Molecular Reactions", *IEEE Design and test Magazine*, **29**(3), May/June 2012

156. M. Ayinala, M.J. Brown and K.K. Parhi, "Pipelined Parallel FFT Architectures via Folding Transformation", *IEEE Trans. VLSI Systems*, **20**(6), pp. 1068-1081, June 2012

157. C. Zhang and K.K. Parhi, "A Network-Efficient Non-Binary QC-LDPC Decoder Architecture", *IEEE Trans. Circuits and Systems, Part-I: Regular Papers*, **59**(6), pp. 1359-1371, June 2012

158. T.-L. Kung, and K.K. Parhi, "Optimized Joint Timing Synchronization and Channel Estimation for OFDM Systems," *IEEE Wireless Communications Letters*, **1**(3), pp. 149-152, June 2012

159. H. Patil, and K.K. Parhi,"Static And Dynamic Iinformation Derived from Source and System Features for Person Recognition from Humming," *Springer Int. Journal of Speech Technology*, **15**(3), pp. 393-406, Sept. 2012

160. T.-L. Kung and K.K. Parhi, "Semiblind Frequency-Domain Timing Synchronization and Channel Estimation for OFDM Systems," *EURASIP Journal on Advances in Signal Processing*, **2013**(1), Jan. 2013

161. Y. Hu and K.K. Parhi, ""Design and Optimization of Multiplierless FIR Filters Using Sub-Threshold Circuits", *Springer Journal of Signal Processing Systems*, **70**(3), pp. 259-274, March 2013

162. T.-L. Kung and K.K. Parhi, "Performance Evaluation of Variable Transmission Rate OFDM Systems via Network Source Coding," *EURASIP Journal on Advances in Signal Processing*, **2013**(12), 2013

163. K.K. Parhi, "Comments on "Low-Energy CSMT Carry Generators and Binary Adders"" *IEEE Trans. VLSI Systems*, **21**(4), p. 791, April 2013

164. T. Xu, M. Stephane, and K.K. Parhi, "Multidimensional Analysis of Abnormal Neural Oscillations Associated with Lexical Processing in Schizophrenia," *Clinical EEG & Neuroscience*,**44**(2), pp. 135-143, April 2013

165. C. Zhang and K.K. Parhi, "Low-Latency Sequential and Overlapped Architectures for Successive Cancellation Polar Decoder," *IEEE Trans. Signal Processing*, **61**(10), pp. 2429-2441, May 15, 2013

166. H. Jiang, S.A. Salehi, M.D. Riedel, and K.K. Parhi "Discrete-Time Signal Processing with DNA," *ACS Synthtic Biology*, **2**(5), pp. 245-254, 2013

167. S.A. Salehi, R. Amirfattahi, and K.K. Parhi, "Pipelined Architectures for Real-Valued FFT and Hermitian-Symmetric IFFT with Real Datapaths," *IEEE Trans. Circuits and Systems, Part-II: Transactions Briefs*, **60**(8), pp. 507-511, Aug. 2013

168. M. Ayinala and K.K. Parhi, "FFT Architectures for Real-valued Signals based on Radix-2$\hat{3}$ and Radix-2$\hat{4}$ algorithms," *IEEE Trans. Circuits and Systems, Part-I: Regular Papers*, **60**(9), pp. 2422-2430, Sept. 2013

169. K.K. Parhi, "Hierarchical Folding and Synthesis of Iterative Data-Flow Graphs," *IEEE Trans. Circuits and Systems-II: Transactions Briefs*, **60**(9), pp. 597-601, Sept. 2013

170. T.-L. Kung and K.K. Parhi, "Optimized Joint Timing Synchronization and Channel Estimation for OFDM Systems with Multiple Transmit Antennas," *EURASIP Journal on Advances in Signal Processing*, bfVol. 2013(139), 2013

171. M. Ayinala, Y. Lao and K.K. Parhi, "An In-Place Architecture for Real-Valued Signals," *IEEE Trans. Circuits and Systems, Part-II: Transactions Briefs*, to appear **60**(10), pp. 652-656, Oct. 2013

172. K.K. Parhi, and M. Ayinala, "Low-Complexity Welch Power Spectral Density Computation," *IEEE Trans. Circuits and Systems, Part-I: Regular Papers*, **61**(1), pp. 172-182, Jan. 2014

173. R. Liu, T.-L. Kung, and K.K. Parhi, "Implulse Noise Correction in OFDM Systems," *Springer J. of Signal Processing Systems*, **74**, pp. 245-262, 2014

174. C. Zhang and K.K. Parhi, "Latency Analysis and Architecture Design of Simplified SC Polar Decoders," *IEEE Trans. Circuits and Systems, Part-II: Transactions Briefs*, **61**(2), pp. 115-119, 2014

175. B. Yuan and K.K. Parhi, "Low-Latency Successive-Cancellation Polar Decoder Architectures using 2-bit Decoding," *IEEE Trans. Circuits and Systems, Part-I: Regular Papers*, **61**(4), pp. 1241-1254, April 2014

176. Y. Lao and K.K. Parhi, "Statistical Analysis of MUX-based Physical Unclonable Functions," *IEEE Transactions on Computer Aided Design*," **33**(5), pp. 649-662, May 2014

177. S. Roychowdhury, D. Koozekanani and K.K. Parhi, DREAM: Diabetic Retinopathy Analysis using Machine Learning," *IEEE Journal of Biomedical and Health Informatics*, **18**(5), pp. 1717-1728, September 2014

178. Y. Wang, B. Yuan, K.K. Parhi and R. Victora, "Two-Dimensional Magnetic Recording using a Rotated Head Array and LDPC Code Decoding," *IEEE Trans. Magnetics*, **50**(11), November 2014

179. B. Yuan and K.K. Parhi, "Early Stopping Criteria for Low-Power Low-Latency Belief-Propagation Polar Code Decoders," *IEEE Trans. Signal Processing*, **62**(24), pp. 6496-6506, December 2014

180. Y. Lao and K.K. Parhi, "Obfuscating DSP Circuits via High-Level Transformations," *IEEE Transactions on VLSI Systems*, **23**(5), pp. 819-830, May 2015

181. S. Roychowdhury, D.D. Koozekanani, and K.K. Parhi, "Blood Vessel Segmentation of Fundus Images by Major Vessel Extraction and Sub-Image Classification," *IEEE Journal of Biomedical and Health Informatics*, **19**(3), pp. 1118-1128, May 2015

182. S. Roychowdhury, D.D. Koozekanani, and K.K. Parhi, "Iterative Vessel Segmentation of Fundus Images," *IEEE Trans. Biomedical Engineering*, **62**(7), pp. 1738-1749, July 2015

183. M. Bandarabadi, J. Rasekhi, C.A. Teixeira, T.I. Netoff and K.K. Parhi, and A. Dourado, "Early Seizure Detection using Neuronal Potential Similarity:A Generalized Low-Complexity and Robust Measure," *International Journal of Neural Systems (IJNS)*, **25**(5), pp. 1550019:1-18, May 2015

184. S.A. Salehi, H. Jiang, M.D. Riedel and K.K. Parhi, "Molecular Sensing and Computing Systems (Invited Paper)," *IEEE Transactions on Molecular, Biological, and Multi-Scale Communications*, **1**(3), pp. 249-264, Sept. 2015

185. B. Yuan and K.K. Parhi, "Low-Latency Successive-Cancellation List Decoders for Polar Codes with Multi-bit Decision," *IEEE Trans. VLSI Systems*, **23**(10), pp. 2268-2280, Oct. 2015

186. T. Xu, K.R. Cullen, B. Mueller, M.W. Schreiner, K.O. Lim, S.C. Schulz, "Network Analysis of Functional Brain Connectivity in Borderline Personality Disorder Using Resting-State fMRI," *NeuroImage: Clinical*, **11**, pp. 302-315, 2016

187. Y. Lao, Q. Tang, C.H. Kim and K.K. Parhi, "Beat Frequency Based True Random Number Generators: Statistical Modeling and Analysis," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, **13**(1), Articel 9, June 2016

188. Z. Zhang and K.K. Parhi, "Low-Complexity Seizure Prediction from iEEG/sEEG using Spectral Power and Ratios of Spectral Power," *IEEE Trans. Biomedical Circuits and Systems*, **10**(3), pp. 693-706, June 2016

189. Y. Liu and K.K. Parhi, "Architectures for Recursive Digital Filters Using Stochastic Computing," *IEEE Transactions on Signal Processing*, **64**(14), pp. 3705-3718, July 15, 2016

190. Y. Wang, B. Yuan and K.K. Parhi, "Improved BER Performance with Rotated Head Array and 2D Detector in Two-Dimensional Magnetic Recording," *IEEE Transactions on Magnetics*, **52**(7), July 2016

191. T. Xu, M. Stephane, and K.K. Parhi, "Abnormal Neural Oscillations in Schizophrenia Assessed by Spectral Power Ratio of MEG during Word Processing," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, **24**(11), pp. 1148-1158, Nov. 2016

192. S. Roychowdhury, D.D. Koozekanani, S.N. Kuchinka, and K.K. Parhi, "Optic Disc Boundary and Vessel Origin Segmentation of Fundus Images," *IEEE Journal of Biomedical and Health Informatics*, **20**(6), pp. 1562-1574, Nov. 2016

193. B. Yuan and K.K. Parhi, "LLR-based Successive-Cancellation List Decoder for Polar Codes with Multi-bit Decision," *IEEE Transactions on Circuits and Systems, Part-II: Transactions Briefs*, **64**(1), pp. 21-25, Jan. 2017

194. S.A. Salehi, K.K. Parhi, and M.D. Riedel, "Chemical Reaction Networks for Computing Polynomials," *ACS Synthtic Biology*, **6**(1), pp. 76-83, Jan. 2017

195. Y. Lao, B. Yuan, C.H. Kim, and K.K. Parhi, "Reliable PUF-based Local Authentication with Self-Correction," *IEEE Trans. Computer Aided Design of Integrated Circuits and Systems*, **36**(2), pp. 201-213, Feb. 2017

196. B. Yuan and K.K. Parhi, "VLSI Architectures for the Restricted Boltzmann Machine," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, **13**(3), Article 35, 2017

197. Y. Liu and K.K. Parhi, "Computing Polynomials using Unipolar Stochastic Logic," *ACM Journal of Emerging Technologies in Computing Systems (JETC)*, **3**(3), Article 42, 2017

198. K.K. Parhi, "Takao Nishitani: An Outstanding Researcher, Technical Leader and Mentor," *IEEE Solid-State Circuits Magazine*, **9**(2), pp. 35-37, Spring 2017

199. Y. Lao and K.K. Parhi, "Canonic FFT Flow-Graphs for Real-Valued Even/Odd Symmetric Inputs," *EURASIP Journal on Advances in Signal Processing*, **2017**(45), June 2017

200. A. Rashno, B. Nazari, D. D. Koozekanani, P.M. Drayna, S. Sadri, H. Rabbani and K.K. Parhi, "Fully-Automated 2D and 3D Segmentation of Fluid Regions in Exudative Age-Related Macular Degeneration Subjects: Kernel Graph Cut in Neutrosophic Domain," *to PLoS ONE*, **12**(10), e0186949, Oct. 2017

201. S. Koteshwara, C.H. Kim and K.K. Parhi, "Key-Based Dynamic Functional Obfuscation of Integrated Circuits using Sequentially-Triggered Mode-Based Design," *IEEE Trans. Information Forensics and Security*, **13**(1), pp. 79-93, Jan. 2018

202. S. Chu, K.K. Parhi and C. Lenglet, "Function-specific and Enhanced Brain Structural Connectivity Mapping via Joint Modeling of Diffusion and Functional MRI," *Nature Scientific Reports*, **8**, Article 4741, March 2018

203. A. Rashno, D.D. Koozekanani, P.M. Drayna, B. Nazari, S. Sadri, H. Rabbani and K.K. Parhi, "Fully-Automated Segmentation of Fluid/Cyst Regions in Optical Coherence Tomography Images with Diabetic Macular Edema using Neutrosophic Sets and Graph Algorithms," *IEEE Trans. on Biomedical Engineering*, **65**(5), pp. 989-1001, May 2018

204. S.A. Salehi, X. Liu, M.D. Riedel, and K.K. Parhi, "Computing Mathematical Functions using DNA via Fractional Coding," *Nature Scientific Reports*, **8**, Article 8312, May 2018

205. Y. Liu and K.K. Parhi, "Linear-Phase Lattice FIR Digital Filter Architectures using Stochastic Logic," *Springer Journal of Signal Processing Systems*, **90**(5), pp. 791-803, May 2018

206. Y. Lao and K.K. Parhi, "Canonic Composite Length Real-Valued FFT," *Springer Journal of Signal Processing Systems (JSPS)*, **90**(10), pp. 1401-1414, Oct. 2018

207. M. Garrido, N.K. Unnikrishnan, and K.K. Parhi, "A Serial Commutator Fast Fourier Transform for Real-Valued Signals," *IEEE Transactions on Circuits and Systems, Part-II: Transactions Briefs*, **65**(11), pp. 1693-1697, November 2018

208. K.K. Parhi, "Stochastic Logic Implementations of Polynomials with All Positive Coefficients by Expansion Methods," *IEEE Transactions on Circuits and Systems, Part-II: Transactions Briefs*, **65**(11), pp. 1698-1702, November 2018

209. S. Koteshwara and K.K. Parhi, "Incremental-Precision based Feature Computation and Multi-Level Classification for Low-Energy Internet-of-Things," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **8**(4), pp. 822-835, December 2018

210. K.K. Parhi and Y. Liu, "Computing Arithmetic Functions Using Stochastic Logic by Series Expansion," *IEEE Transactions on Emerging Topics in Computing (TETC)*, **7**(1), pp. 44-59, March 2019

211. S. Koteshwara, A. Das and K.K. Parhi, "Architecture Optimization and Performance Comparison of Nonce-Misuse Resistant Authenticated Encryption Algorithms," *IEEE Trans. VLSI Systems*, **27**(5), pp. 1053-1066, May 2019

212. B. Sen, S. Chu and K.K. Parhi, "Sub-Graph Entropy: Am approach for Ranking Regions, Edges and Classifying Tasks in Functional Brain Graphs," *Scientific Reports*, to appear

213. Z. Zhang and K.K. Parhi, "MUSE: Minimum Uncertainty and Sample Elimination Based Binary Feature Selection," *IEEE Transactions on Knowledge and Data Engineering*, to appear

214. Z. Zhang and K.K. Parhi, "M3U: Minimum Mean Minimum Uncertainty Feature Selection For Multiclass Classification," *Springer Journal of Signal Processing Systems (JSPS)*, to appear

215. H. Bogunovic, F. Venhuizen, S. Klimscha, S. Apostolopoulos, A. Bab-Hadiashar, U. Bagci, M. Faisal Beg, L. Bekalo, Q. Chen, C. Ciller, K. Gopinath, A.K. Gostar, K. Jeon, Z. Ji, S.-H. Kang, D.D. Koozekanani, D. Lu, D. Morley, K.K. Parhi, H.-S. Park, A. Rashno, M. Sarunic, S. Shaikh, J. Sivaswamy, R. Tennakoon, S. Yadav, S. De Zanet, S.M. Waldstein, B.S. Gerendas, C. Klaver, C.I. Sanchez, U. Schmidt-Erfurth, "RETOUCH - The Retinal OCT Fluid Detection and Segmentation Benchmark and Challenge," *IEEE Transactions on Medical Imaging*, to appear

216. K.K. Parhi and Z. Zhang, "Discriminative Ratio of Spectral Power and Relative Power Features Derived via Frequency-Domain Model Ratio (FDMR) with Application to Seizure Prediction," *IEEE Trans. Biomedical Circuits and Systems*, to appear

Refereed Conference Publications

1. K.K. Parhi and R.S. Berkowitz, "False Alarm Threshold Setting in Complex Multi-Variate Systems using Importance Sampling Technique", *Proceedings of the 29th Midwest Symposium on Circuits and Systems*, Lincoln, Nebraska, August 1986, pp. 227-230

2. K.K. Parhi and D.G. Messerschmitt, "A Bit Parallel Bit Level Recursive Filter Architecture", *Proceedings of the IEEE International Conference on Computer Design*, October 6-9, 1986, Rye Town, Rye, NY, pp. 284-289

3. K.K. Parhi and D.G. Messerschmitt, "Look-Ahead Computation: Improving Iteration Bound in Linear Recursions", *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, Dallas, April 1987, pp. 1855-1858

4. K.K. Parhi and D.G. Messerschmitt, "Block Digital Filtering via Incremental Block-State Structure", *Proceedings of the IEEE International Symposium on Circuits and Systems*, Philadelphia, May 1987, pp. 645-648

5. K.K. Parhi, W.L. Chen, and D.G. Messerschmitt, "Architecture Considerations for High Speed Recursive Filtering", *Proceedings of the 1987 IEEE International Symposium on Circuits and Systems*, Philadelphia, May 1987, pp. 374-377

6. K.K. Parhi and D.G. Messerschmitt, "Area-Efficient High-Speed VLSI Adaptive Filter Architectures", *Proceedings of the IEEE International Conference on Communications*, Seattle, June 1987, *invited talk*

7. K.K. Parhi, and D.G. Messerschmitt, "Pipelined VLSI Recursive Filter Architectures using Scattered Look-Ahead and Decomposition", *Proceedings of the IEEE International Conference ef Acoustics, Speech, and Signal Processing*, April 1988, pp. 2120-2123

8. K.K. Parhi, and D.G. Messerschmitt, "Two-Dimensional Recursive Digital Filtering: Pipelining, One- and Two-Dimensional Block Processing", *IEEE International Symposium on Circuits and Systems*, Helsinki, June 1988, pp. 1521-1524

9. K.K. Parhi, and M. Hatamian, "A High Sample Rate Recursive Filter Chip", in *VLSI Signal Processing III*, Chapter 1, IEEE Press, *Proc. of the Third IEEE VLSI Signal Processing Workshop*, Monterey, CA, Nov. 1988, pp. 3-14

10. R. Ramaswami, and K.K. Parhi, "Distributed Scheduling of Broadcasts in a Radio Network", *Proceedings of the 1989 IEEE Infocom*, April 1989, Ottawa

11. K.K. Parhi, and D.G. Messerschmitt, "Rate-Optimal Fully-Static Multiprocessor Scheduling of Data-Flow Signal Processing Programs", *IEEE International Symposium on Circuits and Systems*, Oregon, May 1989, pp. 1923-1928

12. K.K. Parhi, "Look-Ahead in Dynamic Programming and Quantizer Loops", *IEEE International Symposium on Circuits and Systems*, Oregon, May 1989, (*invited talk*), pp. 1382-1387

13. K.K. Parhi, "Nibble-Serial Arithmetic Processor Designs via Unfolding", *IEEE ISCAS 1989* (*invited talk*), pp. 635-640

14. K.K. Parhi and D.G. Messerschmitt, "Fully-Static Rate-Optimal Scheduling of Iterative Data-Flow Programs via Optimum Unfolding", *Proc. of the 1989 International Conference on Parallel Processing*, August 1989, pp. I:209-216, St. Charles (Illinois)

15. K.K. Parhi, "High-Speed Architectures for Dynamic Programming Problems", in *Proc. of 1990 IEEE International Conference on Acoustics, Speech, and Signal Processing*, April 1990, Albuquerque, pp. 1041-1044

16. K. K. Parhi, G.S. Munson, and L.Q. Pham, "Quantization Effects in High-Speed Pipelined Recursive Filters", in *Proc. of IEEE International Conference on Acoustics, Speech, and Signal Processing*, April 1990, Albuquerque, pp. 1743-1746

17. K.K. Parhi, "High-Speed Architectures for Algorithms with Quantizer Loops", in *Proc. of the IEEE International Symposium on Circuits and Systems*, May 1990, New Orleans (*invited talk*), pp. 2357-2360

18. K.K. Parhi, and C.Y. Wang, "Digit-Serial DSP Architectures", *Proceedings of the Third Conference on Application-Specific Array Processors*, September 1990, Princeton, IEEE Computer Society Press, pp. 341-351

19. C.Y. Wang, and K.K. Parhi, "Automatic Generation of Control Circuits in Pipelined DSP Architectures", in *Proceedings of the IEEE International Conference on Computer Design*, September 1990, Cambridge (MA), pp. 324-327

20. C.-Y. Wang, and K.K. Parhi, "Dedicated DSP Architecture Synthesis using the MARS Design System", *Proc. of the 1991 IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, pp. 1253-1256, Toronto, May 1991

21. K.K. Parhi, and J.-S. Lee, "Register Allocation for Design of Data Converters", *Proc. of the 1991 IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, pp. 1133-1136, Toronto, May 1991

22. F.H. Wu, K.K. Parhi, and K. Ganesan, "Neural Network Vector Quantizer Design using Sequential and Parallel Learning Techniques", *Proc. of the 1991 IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, pp. 637-640, Toronto, May 1991

23. L.E. Lucke, A.P. Brown, and K.K. Parhi, "Unfolding and Retiming for High-Level Synthesis", in *Proc. of 1991 IEEE International Symposium on Circuits and Systems*, June 1991, Singapore (*invited talk*), pp. 2351-2354

24. K.K. Parhi, "Register Minimization in DSP Data Format Converters", in *Proc. of 1991 IEEE International Symposium on Circuits and Systems*, June 1991, Singapore (*invited talk*), pp. 2367-2370

25. H.R. Srinivas, and K.K. Parhi, "High-Speed VLSI Arithmetic Processor Architectures Using Hybrid Number Representation", in *Proc. of the 1991 IEEE Int. Conf. on Computer Design*, October 1991, Cambridge, Massachusetts, pp. 564-571

26. K.K. Parhi, "High-Speed Huffman Decoder Architectures", in *Proc. of Twenty-Fifth Annual Asilomar Conference on Signals, Systems, and Computers*, Nov. 4-6, 1991, Pacific Grove (CA), pp. 64-68

27. N.R. Shanbhag, and K.K. Parhi, "A Pipelined LMS Adaptive Filter Architecture", in *Proc. of Twenty-Fifth Annual Asilomar Conference on Signals, Systems, and Computers*, Nov. 4-6, 1991, Pacific Grove (CA), pp. 668-672

28. J-G. Chung, and K.K. Parhi, "Design of Pipelined Lattice IIR Digital Filters", in *Proc. of Twenty-Fifth Annual Asilomar Conference on Signals, Systems, and Computers*, Nov. 4-6, 1991, Pacific Grove (CA), pp. 1021-1025

29. L.E. Lucke, and K.K. Parhi, "Parallel Structures For Rank-Order and Stack Filters", in *Proc. of the 1992 IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, March 1992 (San Francisco), pp. V-645-648

30. K.J. Raghunath, and K.K. Parhi, "Parallel Adaptive DFE Algorithms", in *Proc. of the 1992 IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, March 1992 (San Francisco), pp. IV-353-356

31. L.E. Lucke, and K.K. Parhi, "A New VLSI Architecture for Rank-Order and Stack Filters", in *Proc. of the IEEE International Symposium on Circuits and Systems*, San Diego, May 1992, pp. 101-104

32. C.-Y. Wang, and K.K. Parhi, "High-Level DSP Synthesis using Mars System", in *Proc. of the IEEE International Symposium on Circuits and Systems*, San Diego, May 1992 (*invited talk*), pp. 164-167

33. N.R. Shanbhag, and K.K. Parhi, "A High-Speed Architecture for ADPCM Coder and Decoder", in *Proc. of the IEEE International Symposium on Circuits and Systems*, San Diego, May 1992, pp. 1499-1502

34. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Lattice Filter Architecture", in *Proc. of the IEEE International Symposium on Circuits and Systems*, San Diego, May 1992, pp. 2196-2199

35. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Lattice Filter Architecture", *Proc. of the 1992 European Signal Processing Conference*, August 24-28, 1992, Brussels (Belgium), pp. 1057-1060

36. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Differential Vector Quantizer for Real-Time Video Compression", *Proc. of the IEEE Workshop on Visual Signal Processing and Communications*, September 1992, Raleigh, North Carolina, pp. 9-14

37. K.K. Parhi, and G. Shrimali, "A Concurrent Loss-Less Coder for Video Compression", in *VLSI Signal Processing V*, IEEE Press, Oct. 1992 (Proc. of the Fifth IEEE VLSI Signal Processing Workshop, Napa Valley, CA), pp. 257-266

38. K.K. Parhi, "Impact of Architecture Choices on DSP Circuits", *Proc. of the IEEE TENCON: Region 10 Int. Conference on Computers, Communications, and Automation*, Nov. 9-13, 1992, Melbourne, Australia, pp. 784-788 (*invited talk*)

39. L.E. Lucke, and K.K. Parhi, "VLSI Structures for Weighted Order Statistics Filters", in *Proc. of IEEE Winter Workshop on Nonlinear Digital Signal Processing*, Tampere, Finland, January 17-20, 1993, pp. 5.2.2.1-5.2.2.5

40. G. Shrimali, and K.K. Parhi, "Fast Arithmetic Decoder Architectures", *Proceedings of Sixth SIAM Conference on Parallel Processing for Scientific Computing*, March 22-24, 1993, Norfolk, VA, pp. 1025-1032

41. L.E. Lucke, and K.K. Parhi, "Block Processing for Rank-Order Filtering using the Rank-Order State Machine Architecture", in *Proc. of the 1993 IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, April 1993, Minneapolis (MN), pp. I-357-360

42. G. Shrimali, and K.K. Parhi, "Fast Arithmetic Coder Architectures", in *Proc. of the 1993 IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, April 1993, Minneapolis (MN), pp. I-361-364

43. T.C. Denk, K.K. Parhi, and V. Cherkassky, "Combining Neural Network and the Wavelet Transform for Image Compression", in *Proc. of the 1993 IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, April 1993, Minneapolis (MN), pp. I-637-640

44. J.-G. Chung, and K.K. Parhi, "The Scaled Normalized Lattice Digital Filter", *Proc. of the 1993 IEEE Int. Symp. on Circuits and Systems*, May 1993, Chicago, pp. 483-486

45. N.R. Shanbhag, and K.K. Parhi, "Roundoff Error Analysis of the Pipelined ADPCM Coder", *Proc. of the 1993 IEEE Int. Symp. on Circuits and Systems*, May 1993, Chicago, pp. 886-889

46. C.-Y. Wang, and K.K. Parhi, "Loop List Scheduler for DSP Algorithms under Resource Constraints", *Proc. of the 1993 IEEE Int. Symp. on Circuits and Systems*, May 1993, Chicago, pp. 1662-1665

47. K.K. Parhi, and T. Nishitani, "Folded VLSI Architectures for Discrete Wavelet Transforms", *Proc. of the 1993 IEEE Int. Symp. on Circuits and Systems*, May 1993, Chicago, pp. 1734-1737

48. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Differential Vector Quantizer for Low-Power Speech Compression", *Proc. of the 1993 IEEE Int. Symp. on Circuits and Systems*, May 1993, Chicago, pp. 1956-1958

49. K.J. Raghunath, and K.K. Parhi, "High-Speed RLS using Scaled Tangent Rotation (STAR)", *Proc. of the 1993 IEEE Int. Symp. on Circuits and Systems*, May 1993, Chicago, pp. 1959-1962

50. L.E. Lucke, and K.K. Parhi, "Generalized ILP Scheduling and Allocation for High-Level DSP Synthesis", in *Proc. of IEEE Custom Integrated Circuit Conference*, May 9-12, 1993, San Diego, CA, pp. 5.4.1-5.4.4

51. G. Shrimali, and K.K. Parhi, "High-Speed Arithmetic Decoder Architectures", in *Proc. of the IEEE Int. Conference on Communications*, May 23-26, 1993, Geneva (Switzerland), pp. 222-226

52. K.K. Parhi, "Algorithms and Architectures for High-Speed or Low-Power Digital Signal Processing", *Proceedings of the 4th International Conference on Advances in Communications and Control (COMCON 4)*, Rhodes, Greece, June 14-18, 1993, pp. 259-270

53. K.J. Raghunath, and K.K. Parhi, "Pipelined Implementation of High Speed STAR-RLS Adaptive Filters", *Proc. of the SPIE Advanced Signal Processing Algorithms, Architectures, and Implementations IV, 1993 Int. Symp. on Optical Appl. Sci. and Eng.*, Vol. 2027, July 11-16, 1993, San Diego (CA), pp. 122-133

54. N.R. Shanbhag, and K.K. Parhi, "Pipelined Adaptive DFE Architectures", *Proc. of the SPIE Advanced Signal Processing Algorithms, Architectures, and Implementations IV, 1993 Int. Symp. on Optical Appl. Sci. and Eng.*, Vol. 2027, July 11-16, 1993, San Diego (CA), pp. 134-145

55. N.R. Shanbhag, and K.K. Parhi, "Pipelined Adaptive Quantizers using Relaxed Look-Ahead", in *Proc. of the 1993 IEEE Workshop on VLSI in Communications*, Sept. 15-17, 1993, Stanford Sierra Camp, Lake Tahoe, California

56. H.R. Srinivas, B. Vinnakota, and K.K. Parhi, "A C-Testable Carry-Free Divider", *Proceedings of the 1993 IEEE Int. Conf. on Computer Design*, October 3-6, 1993, Cambridge, MA, pp. 206-213

57. N.R. Shanbhag, and K.K. Parhi, "VLSI Implementation of a 100 MHz Pipelined ADPCM Codec Chip", in *VLSI Signal Processing VI*, IEEE Press, *Proc. of the sixth IEEE VLSI Signal Processing Workshop*, Veldhoven, Netherlands, pp. 114-122, Oct. 1993

58. L.E. Lucke, and K.K. Parhi, "Parallel Processing Architectures for Rank-Order and Stack Filters", *Proc. of the 1993 Int. Conf. on Application Specific Array Processors*, Oct. 1993, Venice (Italy), pp. 65-76

59. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Kalman Filter Architecture", *Proc. of the 27th Annual Asilomar Conf. on Signals, Systems, and Computers*, Nov. 1-3, 1993, Pacific Grove (CA), pp. 1225-1229

60. J.-G. Chung, and K.K. Parhi, "Pipelining of Orthogonal Double-Rotation Digital Lattice Filters", *Proc. of the 27th Annual Asilomar Conf. on Signals, Systems, and Computers*, Nov. 1-3, 1993, Pacific Grove (CA), pp. 1613-1617

61. K.K. Parhi, "Calculation of Minimum Number of Registers in Arbitrary Life Time Chart", *Proc. of the Seventh Int. Conf. on VLSI Design*, IEEE Computer Society Press, pp. 83-86, Calcutta, India, January 5-8, 1994

62. K.J. Raghunath, and K.K. Parhi, "Fixed and Floating Point Error Analysis of QRD-RLS and STAR-RLS Adaptive Filters", *Proc. of the 1994 IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, pp. III-81-III-84, April 19-22, 1994, Adelaide, Australia

63. T.C. Denk, and K.K. Parhi, "Calculation of Minimum Number of Registers in 2-D Discrete Wavelet Transforms using Lapped Block Processing", *Proc. of 1994 IEEE Int. Symp. on Circuits and Systems*, pp. 3.77-3.80, May 30 - June 2, 1994, London

64. H.R. Srinivas, and K.K. Parhi, "A Fast Radix-4 Division Algorithm", *Proc. of 1994 IEEE Int. Symp. on Circuits and Systems*, pp. 4.311-4.314, May 30 - June 2, 1994, London

65. K.K. Parhi and T.C. Denk, "VLSI Discrete Wavelet Transform Architectures", in *Proc. of the 1st ARPA RASSP Conference*, pp. 154-170, Aug. 15-18, 1994, Arlington (VA)

66. T.C. Denk, and K.K. Parhi, "Architectures for Lattice Structure Based Orthonormal Discrete Wavelet Transforms", *Proc. of the 1994 Int. Conf. on Application Specific Array Processors*, pp. 259-270, San Francisco, August 1994

67. J.-G. Chung and K.K. Parhi, "Pipelined Wave Digital Filter Design for Narrow-Band Sharp-Transition Digital Filters", in *VLSI Signal Processing VII*, pp. 501-510, IEEE Press, *Proc. of the Seventh IEEE VLSI Signal Processing Workshop*, La Jolla, CA, Oct. 1994

68. S. Jain and K.K. Parhi, "Efficient Power Based Galois Field Arithmetic Architectures", in *VLSI Signal Processing VII*, pp. 306-315, IEEE Press, *Proc. of the Seventh IEEE VLSI Signal Processing Workshop*, La Jolla, CA, Oct. 1994

69. H.R. Srinivas and K.K. Parhi, "Computer Arithmetic Architectures with Redundant Number System", *Proc. of the 28th Asilomar Conf. on Signals, Systems, and Computers*, pp. 182-186, Oct. 31 - Nov. 2, 1994, Pacific Grove, CA (*Invited Talk*)

70. K.K. Parhi, "VLSI Digital Signal Processing Education", *Proc. of the 28th Asilomar Conf. on Signals, Systems, and Computers*, pp. 1303-1308, Oct. 31 - Nov. 2, 1994, Pacific Grove, CA (*Invited Talk*)

71. K. Ito, L.E. Lucke and K.K. Parhi, "Module Selection and Data Format Conversion for Cost-Optimal DSP Synthesis", *Proc. of the IEEE/ACM Int. Conf. on Computer Aided Design*, pp. 322-329, Nov. 6-10, 1994, San Jose (CA)

72. K. Ito and K.K. Parhi, "Determining the Iteration Bound of Data-Flow Graphs", *Proc. of the IEEE Asia-Pacific Conference on Circuits and Systems*, pp. 163-168, Dec. 5-8, 1994, Grand Hotel, Taipei

73. W. Amendola, Jr., H.R. Srinivas, and K.K. Parhi, "A 16-Bit X 16-Bit 1.2 Micron CMOS Multiplier Chip with Low Latency Vector Merging", *Proc. of the 8th Int. Conf. on VLSI Design*, IEEE Computer Society Press, pp. 398-402, Jan. 4-7, 1995, New Delhi, India

74. J.-G. Chung and K.K. Parhi, "Synthesis and Pipelining of Ladder Wave Digital Filters in Digital Domain", in *Proc. of the 1995 IEEE Int. Symp. on Circuits and Systems*, pp. 77-80, Seattle, May 1995

75. D. Pearson and K.K. Parhi, "Low-Power FIR Digital Filter Architectures", in *Proc. of the 1995 IEEE Int. Symp. on Circuits and Systems*, pp. 231-234, Seattle, May 1995

76. B. Fu and K.K. Parhi, "Generalized Multiplication Free Arithmetic Codes", in *Proc. of the 1995 IEEE Int. Symp. on Circuits and Systems*, pp. 437-440, Seattle, May 1995

77. B. Fu and K.K. Parhi, "Two VLSI Design Advances in Arithmetic Coding", in *Proc. of the 1995 IEEE Int. Symp. on Circuits and Systems*, pp. 1440-1443, Seattle, May 1995

78. S. Jain and K.K. Parhi, "A Low-Latency Standard Basis GF(2^m) Multiplier", in *Proc. of the 1995 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 2747-2750, May 1995, Detroit (MI)

79. K.J. Raghunath and K.K. Parhi, "A 100 MHz RLS Adaptive Filter Chip", in *Proc. of the 1995 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 3187-3190, May 1995, Detroit (MI)

80. K.K. Parhi, "Trading off Concurrency for Low-Power in Linear and Nonlinear Computations", in *Proc. of 1995 IEEE Workshop on Nonlinear Signal Processing*, June 1995, pp. 895-898, Thessaloniki, Greece

81. H.R. Srinivas and K.K. Parhi, "A Floating Point Radix 2 Shared Division/Square Root Chip", *Proc. of the 1995 IEEE Int. Conf. on Computer Design*, pp. 472-478, October 1995, Austin

82. T.C. Denk and K.K. Parhi,"Systematic Design of Architectures for M-ary Tree-Structured Filter Banks", pp. 157-166, in *VLSI Signal Processing VIII*, IEEE Press, *Proc. of the 1995 IEEE Workshop on VLSI Signal Processing*, Sakai, Japan, Oct. 1995

83. K. Ito and K.K. Parhi,"Register Minimization in Cost-Optimal Synthesis of DSP Architectures", pp. 207-216, in *VLSI Signal Processing VIII*, IEEE Press, *Proc. of the 1995 IEEE Workshop on VLSI Signal Processing*, Sakai, Japan, October 1995

84. C.-Y. Wang and K.K. Parhi, "MARS: A High-Level DSP Synthesis Tool Integrated within the Mentor Graphics Environment", in *Proc. of Mentor Graphics Users' Group Annual Conference*, October 22-27, 1995, Portland

85. Y.N. Chang, C.Y. Wang and K.K. Parhi, "High-Level DSP Synthesis with Heterogeneous Functional Units using the MARS-II System", *Proc. of the 1995 Asilomar Conf. on Signals, Systems and Computers*, pp. 109-116, Pacific Grove (CA), November 1995 (*invited talk*)

86. Y.-N. Chang, C.Y. Wang, and K.K. Parhi, "Loop List Scheduling for Heterogeneous Functional Units", *Proc. of Sixth Great Lakes Symp. on VLSI*, pp. 2-7, March 1996, Ames (Iowa)

87. S.K. Jain and K.K. Parhi, "Efficient Standard Basis Reed-Solomon Encoder", *in Proc. of 1996 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 3287-3290, May 1996, Atlanta

88. T.C. Denk, M. Majumdar and K.K. Parhi, "Two-Dimensional Retiming with Low Memory Requirements", *in Proc. of 1996 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 3330-3333, May 1996, Atlanta

89. J. Satyanarayana and K.K. Parhi, "A Hierarchical Approach to Transistor Level Power Estimation of Arithmetic Units", *in Proc. of 1996 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 3338-3341, May 1996, Atlanta

90. Y. Li and K.K. Parhi, "STAR RLS Lattice Adaptive Filters", *in Proc. of 1996 IEEE Int. Symp. on Circuits and Systems*, pp. II: 389-392, May 1996, Atlanta

91. A. Shalash and K.K. Parhi, "Comparison of Discrete Multitone and Carrierless AM/PM Techniques for Line Equalization", *in Proc. of 1996 IEEE Int. Symp. on Circuits and Systems*, pp. II: 560-563, May 1996, Atlanta

92. L. Montalvo and K.K. Parhi, "Radix-2 Over-Redundant Digit-Set Converters", *in Proc. of 1996 IEEE Int. Symp. on Circuits and Systems*, pp. 81-84, May 1996, Atlanta

93. M. Majumdar and K.K. Parhi, "Synthesis of Low-Area Data Format Converters", *Proc. of 1996 IEEE Int. Symp. on Circuits and Systems*, pp. 145-148, May 1996, Atlanta

94. T.C. Denk and K.K. Parhi, "A Unified Framework for Characterizing Retiming and Scheduling Solutions", *in Proc. of 1996 IEEE Int. Symp. on Circuits and Systems*, pp. 568-571, May 1996, Atlanta

95. J. Satyanarayana and K.K. Parhi, "HEAT: Hierarchical Energy Analysis Tool", *Proc. of ACM IEEE Design Automation Conference*, Las Vegas, pp. 9-14, June 3-7, 1996

96. L.L. Song and K.K. Parhi, "Efficient Finite Field Serial/Parallel Multiplication", *Proc. of the 1996 Int. Conf. on Applications-specific Systems, Architectures, and Processors*, pp. 72-82, Chicago, August 1996

97. D.A. Parker and K.K. Parhi, "Low Area/Power Parallel FIR Digital Filters", *Proc. of the 1996 Int. Conf. on Applications-specific Systems, Architectures, and Processors*, pp. 93-111, Chicago, August 1996

98. J.H. Satyanarayana, K.K. Parhi, L.L. Song and Y.N. Chang "Systematic Analysis of Bounds on Power Consumption in Pipelined and Non-pipelined Multipliers", *Proc. of 1996 IEEE Int. Conf. on Computer Design*, pp. 492-499, October 1996, Austin (Texas)

99. L. Montalvo, K.K. Parhi, and J.H. Satyanarayana, "Estimation of Average Energy Consumption of Ripple-Carry Adder Based on Maximum Average Carry Chains", in *VLSI Signal Processing IX*, pp. 189-198, IEEE Press, *Proc. of the 1996 IEEE Workshop on VLSI Signal Processing*, San Francisco, Oct. 1996

100. C. Xu, C.-Y. Wang and K.K. Parhi, "Order-Configurable Programmable Power Efficient FIR Filters", *Proc. of 3rd Int. Workshop on Image and Signal Processing*, pp. 535-538, November 1996, UMIST (UK) (*Invited Talk*)

101. L. Montalvo and K.K. Parhi, "Estimation of Average Energy Consumption of Ripple Carry Adder Based on Average Length Carry Chains", *Proc. of 1996 Design of Integrated Circuits and Systems Conf. (DCIS)*, pp. 11-16, Barcelona (Spain), Nov. 1996

102. J.P. Ma, K.K. Parhi, and E.F. Deprettere, "Pipelining of Cordic Based IIR Digital Filters", *Proc. of ProRISC/IEEE Workshop*, Mierlo, The Netherlands, Nov. 1996

103. C. Xu, C.-Y. Wang and K.K. Parhi, "Order-Configurable Programmable Power Efficient FIR Filters", *Proc. of Int. Conf. on High Performance Computing*, pp. 357-361, Trivandrum (India), December 1996 (*Invited Talk*)

104. J.P. Ma, K.K. Parhi and E.F. Deprettere, "Pipelining of Cordic Based IIR Digital Filters", *Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 643-646, Munich, April 1997

105. L. Song and K.K. Parhi, "Low-Area Dual-Basis Divider Over $GF(2^M)$", *Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 627-530, Munich, April 1997

106. A. Shalash and K.K. Parhi, "Three-Dimensional Carrierless AM/PM Line Code for Unshielded Twisted Pair Cables", *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. 2136-2139, Hong Kong, June 1997 (*Invited Talk*)

107. Y.N. Chang, J. Satyanarayana and K.K. Parhi, "Low-Power Digit-Serial Architectures", *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. 2164-2167, Hong Kong, June 1997 (*Invited Talk*)

108. H. Kim, J.-G. Chung and K.K. Parhi, "Low-Noise Implementation Technique for Pipelined Filters with Crowded Poles", *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. 2196-2199, Hong Kong, June 1997

109. T.T. Vu, P.C. Nguyen,L.T. Vu, C.H. Nguyen, M.D. Bui, A.C. Nguyen, J.N.C. Vu, R. Harjani, L.L. Kinney, K.K. Parhi, D.L. Polla, R. Schaumann, P.J. Schiller and M.S. Shur, "Microsensors Fabricated in Gallium Arsenide", *Proc. of Technology 1997 (NASA Tech Briefs, Federal Laboratory Consortium, and Technology Utilization Foundation)*, Sept. 22-24, 1997, Boston, MA

110. V. Sundararajan, M.E. Zervakis and K.K. Parhi, "Area/Power Efficient Implementation of a Wavelet Domain Robust Image Denoising System", *Proc. of IEEE Workshop on Non-Linear Signal Processing*, Michigan, September 1997

111. L. Song, K.K. Parhi, I. Kuroda and T. Nishitani, "Heterogeneous Digit-Serial Finite Field Multipliers and Low-Energy Reed-Solomon Codecs", *Proc. of 35th Annual Allerton Conference on Communication, Control, and Computing*, Illinois, Sept. 29 - Oct. 1, 1997 *Invited Talk*

112. Y.-N. Chang, J.H. Satyanarayana, and K.K. Parhi, "Design and Implementation of Low-Power Digit-Serial Multipliers", *Proc. of IEEE Conf. on Computer Design*, pp. 186-195, Austin, October 12-15, 1997

113. K.K. Parhi, "Fast Low-Energy VLSI Binary Addition", *Proc. of IEEE Conf. on Computer Design*, pp. 676-684, Austin, October 12-15, 1997

114. K.K. Parhi, "Low-Power Multimedia DSP Systems", *Proc. of 1997 Int. Conf. on VLSI and CAD (ICVC)*, pp. 10-17, Seoul, Korea, Oct. 13-15, 1997, *Plenary Talk*

115. M.E. Zervakis, V. Sundararajan and K.K. Parhi, "A Wavelet-Domain Algorithm for Denoising in the Presence of Noise Outliers", *Proc. of IEEE Int. Conf. on Image Processing*, pp. I-632-I-635, Santa Barbara, October 26-29, 1997

116. W. Freking and K.K. Parhi, "Low-Power Digital Filters using Residue Arithmetic", *Proc. of 1997 Asilomar Conf. on Signals, Systems and Computers*, pp. 739-743, November 1997 *Invited Talk*

117. J. Ma, E.F. Deprettere and K.K. Parhi, "Pipelined Cordic Based QRD-RLS Adaptive Filtering Using Matrix Look-Ahead" *Proc. of 1997 IEEE Workshop on Signal Processing Systems: Design and Implementation*, pp. 131-140, Leicester, U.K., Nov. 1997

118. K.K. Parhi, "Fast VLSI Binary Addition", *Proc. of 1997 IEEE Workshop on Signal Processing Systems: Design and Implementation*, pp. 232-241, Leicester, U.K., Nov. 1997

119. L. Song and K.K. Parhi, "Optimum Primitive Polynominals for Low Area and Low Power Finite Field Semi-Systolic Multipliers", *Proc. of 1997 IEEE Workshop on Signal Processing Systems: Design and Implementation*, pp. 375-384, Leicester, U.K., Nov. 1997

120. T.T. Vu, P.C. Nguyen, L.T. Vu, C.H. Nguyen, M.D. Bui, A.C. Nguyen, J.N.C. Vu, R. Harjani, K.K. Parhi, D.L. Polla, R. Schaumann, P.J. Schiller and M.S. Shur, "Gallium Arsenide Based Microsensor Systems", *Proc. of Government Microcircuit Applications Conference*, March 16-19, 1998, Arlington, Virginia

121. J. Ma, K.K. Parhi, and E.F. Deprettere, "Pipelined Cordic Based QRD-MVDR Adaptive Beamforming", *in Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 3025-3028, May 1998, Seattle

122. L. Song, K.K. Parhi, I. Kuroda, and T. Nishitani, "Low-energy Heterogeneous Digit-Serial Reed-Solomon Codecs", *in Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 3049-3052, May 1998, Seattle

123. V. Sundararajan and K.K. Parhi, "Synthesis of Folded, Pipelined Architectures for Multi-Dimensional Multirate Systems", *in Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 3089-3092, May 1998, Seattle

124. L. Song, K.K. Parhi, I. Kuroda and T. Nishitani, "Low-Energy Programmable Finite Field Datapath Architectures", *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. II-406-II-409, Monterey, May 31 - June 3, 1998

125. J. Ma, K.K. Parhi, and E.F. Deprettere, "High-Speed Cordic Based Parallel Weight Extraction For QRD-RLS Adaptive Filtering", *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. V-245-V-248, Monterey, May 31 - June 3, 1998

126. V. Sundararajan and K.K. Parhi, "Synthesis of Folded Multi-Dimensional DSP Systems", *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. II-433-II-436, Monterey, May 31 - June 3, 1998

127. R. Freking and K.K. Parhi, "Theoretical Estimation of Power Consumption in Binary Adders", *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. II-453-II-457, Monterey, May 31 - June 3, 1998

128. J.-G. Chung, Y.-B. Kim, H.-J. Jeong, and K.K. Parhi, "Efficient Parallel FIR Filter Implementations using Frequency Spectrum Characteristics", *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. V-354-V-358, Monterey, May 31 - June 3, 1998

129. A. Shalash and K.K. Parhi, "Three-Dimensional Equalization for the 3-D QAM System with Strength Reduction", *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. IV-453-IV-456, Monterey, May 31 - June 3, 1998

130. M. Kuhlmann and K.K. Parhi, "Power Comparison of SRT and NST Dividers", *Proc. of the SPIE Advanced Signal Processing Algorithms, Architectures, and Implementations VIII, 1998 Int. Symp. on Optical Sci., Eng. and Instrumentation*, July 19-24, 1998, San Diego (CA)

131. J. Ma, K.K. Parhi, G.J. Hekstra, and E.F. Deprettere, "Efficient implementations of Cordic-based IIR digital filters using fast orthonormal micro-rotations, *Proc. of the SPIE Advanced Signal Processing Algorithms, Architectures, and Implementations VIII, 1998 Int. Symp. on Optical Sci., Eng. and Instrumentation*, July 19-24, 1998, San Diego (CA)

132. L. Song and K.K. Parhi, "Scheduling Strategies for Low-Energy Programmable Digit-Serial Reed-Solomon Codecs", *Proc. of 1998 IEEE Workshop on Signal Processing Systems: Design and Implementations (SiPS)*, pp. 275-284, Oct. 8-10, 1998, Boston

133. J. Ma, K.K. Parhi, and E.F. Deprettere, "Pipelined implementation of Cordic-based QRD-MVDR adaptive beamforming", *Proc. of the 4th Int. conf. on Signal Processing (ICSP)*, Vol. 1, pp. 514-517, 1998

134. J. Ma and K.K. Parhi, "High-Speed VLSI State-Space Orthogonal IIR Digital Filters Using Matrix Lookahead", *Proc. of 1998 IEEE Workshop on Signal Processing Systems: Design and Implementations (SiPS)*, pp. 417-426, Oct. 8-10, 1998, Boston

135. A. Karandikar and K.K. Parhi, "Low-Power SRAM Design Using Hierarchical Divided Bit-Line Approach", *Proc. of 1998 IEEE Int. Conf. on Computer Design*, pp. 82-88, Austin, Oct. 1998

136. M. Kuhlmann and K.K. Parhi, "Fast Low-Power Shared Division and Sqaure-Root Architecture", *Proc. of 1998 IEEE Int. Conf. on Computer Design*, pp. 128-135, Austin, Oct. 1998

137. Y.N. Chang and K.K. Parhi, "High-Performance Digit-Serial Complex-Number Multiplier-Accumulator", *Proc. of 1998 IEEE Int. Conf. on Computer Design*, pp. 211-213, Austin, Oct. 1998

138. A. Shalash and K.K. Parhi, "Power Efficient FIR Folding Transformation for Wireline Digital Communications", *Proc. of 1998 Asilomar Conf. on Signals, Systems and Computers*, pp. 1816-1820, Nov. 1-4, 1998, Pacific Grove (CA)

139. M. Kuhlmann and K.K. Parhi, "Power Comparison of Flow-Graph and Distributed Arithmetic Based DCTs", *Proc. of 1998 Asilomar Conf. on Signals, Systems and Computers*, pp. 1214-1219, Nov. 1-4, 1998, Pacific Grove (CA)

140. T.C. Denk and K.K. Parhi, Systolic VLSI Architectures for 1-D Discrete Wavelet Transforms", *Proc. of 1998 Asilomar Conf. on Signals, Systems and Computers*, pp. 1220-1224, Nov. 1-4, 1998, Pacific Grove (CA)

141. H. Suzuki, Y.N. Chang and K.K. Parhi, "Performance Tradeoffs in Digit-Serial DSP Systems", *Proc. of 1998 Asilomar Conf. on Signals, Systems and Computers*, pp. 1225-1229, Nov. 1-4, 1998, Pacific Grove (CA)

142. J.H. Satyanarayana and K.K. Parhi, "Theoretical Analysis of Word-Level Switching Activity in the Presence of Glitching and Correlation", *Proc. of 9th Great Lakes Symp. on VLSI*, March 1999, Ann Arbor, MI

143. V. Sundararajan and K.K. Parhi, "Low-Power Gate Resizing of Combinational Circuits by Buffer Redistribution", *Proc. of 1999 Advanced Research on Conference on VLSI*, pp. 170-184, March 1999

144. H. Suzuki, Y.N. Chang and K.K. Parhi, "Low-Power Bit-Serial Viterbi Decoder for Next Generation Wide-Band CDMA Systems", *Proc. of 1999 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Phoenix, pp. 1913-1916, March 1999

145. R.A. Freking and K.K. Parhi, "An Unrestrictedly Parallel Scheme for Ultra-High-Rate Reprogrammable Huffman Coding", *Proc. of 1999 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 1937-1940, Phoenix, March 1999

146. H. Suzuki, Y.N Chang and K.K. Parhi, "256 States Low-Power Bit-Serial Viterbi Decoder for Next Generation Wireless Applications", *Proc. of 1999 IEEE Customs Integrated Circuits (CICC) Conference*, pp. 589-592, San Diego, May 1999

147. L. Song and K.K. Parhi, "Low-Energy Software Reed-Solomon Codecs Using Specialized Finite Field Datapath and Division-Free Berlekamp-Massey Algorithm", *Proc. of 1999 IEEE Int. Symp. on Circuits and Systems*, pp. I:84-89, Orlando, June 1999

148. W.L. Freking and K.K. Parhi, "Parallel Modular Multiplication with Application to VLSI RSA Implementation", *Proc. of 1999 IEEE Int. Symp. on Circuits and Systems*, pp. I:490-495, Orlando, June 1999

149. L. Song and K.K. Parhi, "Low-Complexity Modified Mastrovito Multipliers over Finite Fields GF(2^m)", *Proc. of 1999 IEEE Int. Symp. on Circuits and Systems*, pp. I:508-512, Orlando, June 1999

150. Z. Chi, J. Ma and K.K. Parhi, "Pipelined QR Decomposition Based Multi-Channel Least Square Lattice Adaptive Filter Architectures", *Proc. of 1999 IEEE Int. Symp. on Circuits and Systems*, pp. III:49-53, Orlando, June 1999

151. S. Summerfield, Z. Wang and K.K. Parhi, "Area-Power-Time Efficient Pipeline-Interleaved Architectures for Wave Digital Filters", *Proc. of 1999 IEEE Int. Symp. on Circuits and Systems*, pp. III:343-346, Orlando, June 1999

152. J. Ma, K.K. Parhi and E.F. Deprettere, "Derivation of Parallel and Pipelined Orthogonal Filter Architectures via Algorithm Transformations", *Proc. of 1999 IEEE Int. Symp. on Circuits and Systems*, pp. III:347-350, Orlando, June 1999

153. A. Shalash and K.K. Parhi, "Multiple Access Over Wireline Channels Using Orthogonal Signaling", *Proc. of 1999 IEEE Int. Symp. on Circuits and Systems*, pp. IV:580-583, Orlando, June 1999

154. V. Sundararajan and K.K. Parhi, "Synthesis of Low Power CMOS VLSI Circuits using Dual Supply Voltages", *Prof. of 1999 ACM IEEE Design Automation Conference*, pp. 72-75, New Orleans, June 1999

155. A. Shalash and K.K. Parhi, "Orthogonality Division Multiple Access LTI Transmit Filters for ISI Channels", *Proc. of 1999 IEEE Int. Conf. on Communications*, Vol. 1, pp. 246-250, Vancouver, BC, June 1999

156. V. Sundararajan and K.K. Parhi, "Low Power Synthesis of Dual Threshold Voltage CMOS VLSI Circuits" *Proc. of 1999 IEEE Int. Symp. on Low-Power Electronics and Design*, pp. 139-144, San Diego, Aug. 1999

157. W. Freking and K.K. Parhi, "A Unified Method for Iterative Computation of Modular Multiplication and Reduction Operations", *Proc. of 1999 IEEE Int. Conf. on Computer Design*, pp. 80-87, Austin, TX, Oct. 1999

158. M. Kuhlmann, S. Sapatnekar and K.K. Parhi, "Efficient Crosstalk Estimation", *Proc. of 1999 IEEE Int. Conf. on Computer Design*, pp. 266-272, Austin, TX, Oct. 1999

159. Z. Wang, H. Suzuki and K.K. Parhi, "VLSI Implementation Issues of Turbo Decoder Design for Wireless Applications", *Proc. of 1999 IEEE Workshop on Signal Processing Systems: Design and Implementation*, pp. 503-512, Taipei, Oct. 1999

160. Y.-N. Chang and K.K. Parhi, "Efficient FFT Implementation using Digit-Serial Arithmetic", *Proc. of 1999 IEEE Workshop on Signal Processing Systems: Design and Implementation*, pp. 645-653, Taipei, Oct. 1999

161. M. Kuhlmann and K.K. Parhi, "A High-Speed CORDIC Algorithm and Architecture for Digital Signal Processing Applications", *Proc. of 1999 IEEE Workshop on Signal Processing Systems: Design and Implementation*, pp. 732-741, Taipei, Oct. 1999

162. D. Kumar and K.K. Parhi, "Performance Trade-off of DCT Architectures in Xilinx FPGAs", *Proc. of 1999 Asilomar Conf. on Signals, Systems and Computers*, Vol. 1, pp. 579-583, Pacific Grove, CA, Oct. 24-27, 1999

163. W. Freking and K.K. Parhi, "Montgomery Multiplication and Exponentiation in the Residue Number System", *Proc. of 1999 Asilomar Conf. on Signals, Systems and Computers*, Pacific Grove, Vol. 2, pp. 1312-1316, CA, Oct. 24-27, 1999

164. M. Kuhlmann and K.K. Parhi, "A New CORDIC Rotation Method for Generalized Coordinate Systems", *Proc. of 1999 Asilomar Conf. on Signals, Systems and Computers*, Vol. 2, pp. 1361-1367, Pacific Grove, CA, Oct. 24-27, 1999

165. J. Ma and K.K. Parhi, "An Algorithm Transformation Approach to CORDIC Based Parallel Singular Value Decomposition Architectures", *Proc. of 1999 Asilomar Conf. on Signals, Systems and Computers*, Vol. 2, pp. 1401-1405, Pacific Grove, CA, Oct. 24-27, 1999

166. V. Sundararajan, S. Sapatnekar, and K.K. Parhi, "MARSH: Min-Area Retiming with Setup and Hold Constraints", *Proc. of 1999 IEEE Int. Conf. on Computer Aided Design*, Santa Clara, pp. 2-6, Nov. 1999

167. V. Sundararajan and K.K. Parhi, "Synthesis of Low Power Folded Programmable Coefficient FIR Digital Filters", *Proc. of 2000 IEEE Asia Pacific Design Automation Conference (ASP-DAC)*, pp. 153-156, Yokohama, Jan. 2000

168. V. Sundararajan and K.K. Parhi, "Data Transmission over a Bus with Peak-Limited Transition Activity", *Proc. of 2000 IEEE Asia Pacific Design Automation Conference (ASP-DAC)*, pp. 221-224, Yokohama, Jan. 2000

169. V. Sundararajan and K.K. Parhi, "Reducing Bus Transition Activity by Limited Weight Coding with Codeword Slimming", *Proc. of 2000 Great Lakes Symposium on VLSI*, pp. 13-16, Chicago, IL, March 2000

170. B. Sahoo, M. Kuhlmann and K.K. Parhi, "A Low-Power Correlator", *Proc. of 2000 Great Lakes Symposium on VLSI*, pp. 153-155, Chicago, IL, March 2000

171. T. Sansaloni, J. Valls, and K.K. Parhi, "Digit-Serial Fixed-Coefficient Complex Number Multiplier Accumulator on FPGAs", *Proc. of 2000 IEEE Int. Symp. on Circuits and Systems*, Vol. **4**, pp. 585-588, Geneva, May 2000

172. Z. Wang, H. Suzuki and K.K. Parhi, "Efficient Approaches to Improving Performance of VLSI SOVA-based Turbo Decoders", *Proc. of 2000 IEEE Int. Symp. on Circuits and Systems*, Vol. **1**, pp. 287-290, Geneva, May 2000

173. H. Suzuki, Z. Wang and K.K. Parhi, " A K=3 2 Mbps Low Power Turbo Decoder for 3rd Generation W-CDMA Systems", *Proc. of 2000 IEEE Customs Integrated Circuits Conference*, pp. 39-42, Orlando, May 2000

174. Z. Chi, Z. Wang and K.K. Parhi, "High-Throughput, Low-Energy FEC/ARQ Technique for Short Frame Turbo Codes", *Proc. of 2000 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. **5**, pp. 2653-2656, Istanbul, June 2000

175. V. Sundararajan and K.K. Parhi, "A Novel Multiply Multiple Accumulator Component for Low Power PDSP Design", *Proc. of 2000 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. **6**, pp. 3247-3250, Istanbul, June 2000

176. Y. Wang and K.K. Parhi, "Explicit Cook-Toom Algorithm for Linear Convolution", *Proc. of 2000 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. **6**, pp. 3279-3282, Istanbul, June 2000

177. L. Gao, and K.K. Parhi, "Hierarchical Pipelining and Folding of QRD-RLS Adaptive Filters", *Proc. of 2000 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. **6**, pp. 3283-3286, Istanbul, June 2000

178. Z. Wang and K.K. Parhi, "Decoding Metrics and Their Applications in VLSI Turbo Decoders", *Proc. of 2000 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. **6**, pp. 3370-3373, Istanbul, June 2000

179. V. Sundararajan, S.S. Sapatnekar and K.K. Parhi, "MINFLOTRANSIT: Min-Cost Flow Based Transistor Sizing Tool", *Prof. of 2000 ACM/IEEE Design Automation Conference*, pp. 649-654, Los Angeles, June 2000

180. W.L. Freking and K.K. Parhi, "Performance-Scalable Array Architectures for Modular Multiplication", *Proc. of 2000 Applications-specific Systems, Architectures and Processors (ASAP) Conference*, pp. 149-160, Boston, July 2000

181. L. Gao and K.K. Parhi, "Block-Update Parallel Processing QRD-RLS Algorithm for Throughput Improvement with Low-Power Consumption", *Proc. of 2000 Applications-specific Systems, Architectures and Processors (ASAP) Conference*, pp. 225-234, Boston, July 2000

182. T. Sansaloni, J. Valls and K.K. Parhi, "Digit-Serial Fixed Coefficient Complex Number Multiplier-Accumulator on FPGAs", *Proc. of IEEE ASIC/SOC Conference*, pp. 236-240, Sept. 2000

183. J. Valls, M. Kuhlmann and K.K. Parhi, "Efficient mapping of CORDIC algorithms on FPGA", *Proc. of the 2000 IEEE Workshop on Signal Processing Systems (SiPS): Design and Implementation*, pp. 336-345, Lafayette, LA, Oct. 2000

184. Z. Chi and K.K. Parhi, "High Speed Least Square Adaptive Filter Design Using ART and HAT", *Proc. of the 2000 IEEE Workshop on Signal Processing Systems (SiPS): Design and Implementation*, pp. 427-436, Lafayette, LA, Oct. 2000

185. W. Freking and K.K. Parhi, "Ring-Planarized Cylindrical Arrays with Application to Modular Multiplication", *Proc. of the 2000 IEEE Workshop on Signal Processing Systems (SiPS): Design and Implementation*, pp. 497-506, Lafayette, LA, Oct. 2000

186. T. Zhang and K.K. Parhi, "A Novel Systematic Design Approach of Mastrovito Multipliers over GF(2^m)", *Proc. of the 2000 IEEE Workshop on Signal Processing Systems (SiPS): Design and Implementation*, pp. 507-516, Lafayette, LA, Oct. 2000

187. R.A. Freking and K.K. Parhi, "Highly Parallel Arithmetic Coding", *Proc. of 9th IEEE DSP Workshop*, Hunt, Texas, Oct. 2000

188. Z. Chi, Z. Wang and K.K. Parhi, "Iterative Decoding of Space-Time Trellis Codes and Related Implementation Issues", *Proc. of 2000 Asilomar Conference on Signals, Systems and Computers*, pp. 562-566, Nov. 2000

189. R.A. Freking and K.K. Parhi, "Low-Memory, Fixed-Latency Huffman Encoder for Unbounded Codelength Codes", *Proc. of 2000 Asilomar Conference on Signals, Systems and Computers*, pp. 1031-1034, Nov. 2000

190. W. Freking and K.K. Parhi, "Modular Multiplication in the Residue Number System with Application to Massively-Parallel Public-Key Cryptography Systems" *Proc. of 2000 Asilomar Conference on Signals, Systems and Computers*, pp. 1339-1343, Nov. 2000

191. Y. Wang and K.K. Parhi, "Low-Power Binary Adders", *Proc. of 2000 Asilomar Conference on Signals, Systems and Computers*, pp. 1707-1712, Nov. 2000

192. L. Gao and K.K. Parhi, "Models for Power Consumption and Power Grid Noise Due to Datapath Transition Activity ", *Proc. of 2001 Great Lakes Symposium on VLSI*, VLSI (GLSVLSI), West Lafayette, IN, March 22-23, 2001, pp.121-126.

193. I. Ben Dhaou, V. Sundararajan, H. Tenhunen and K.K. Parhi, "Energy Efficient Signaling in Deep Sub-Micron Technology", *Proc. of 2001 International Symposium on Quality of Electronic Design (ISQED 2001)*, pp. 319-324, March 26-28, 2001, San Jose

194. I. Ben Dhaou, V. Sundararajan, H. Tenhunen, and K.K. Parhi, "Energy Efficient Signaling in Deep Submicron CMOS Technology", *Proc. of 2001 IEEE Int. Symp. on Circuits and Systems*, pp. 411-414, Sydney, May 2001

195. L. Gao and K.K. Parhi, "Custom VLSI Design of Efficient Low Latency and Low Power Finite Field Multiplier for Reed-Solomon Codec", *Proc. of 2001 IEEE Int. Symp. on Circuits and Systems*, pp. 574-577, Sydney, May 2001

196. Z. Chi, L. Song and K.K. Parhi, "A Study On The Performance, Complexity Tradeoffs Of Block Turbo Decoder Design", *Proc. of 2001 IEEE Int. Symp. on Circuits and Systems*, pp. 65-68, Sydney, May 2001

197. T. Zhang, Z. Wang and K.K. Parhi, "On Finite Precision Implementation of Low Density Parity Check Codes Decoder", *Proc. of 2001 IEEE Int. Symp. on Circuits and Systems*, pp. 202-205, Sydney, May 2001

198. Z. Wang, Z. Chi and K.K. Parhi, "Area-Efficient High Speed Decoding Schemes for Turbo/MAP Decoders", *Proc. of 2001 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. 4, pp. 2633-2636, Salt Lake City, Utah, May 2001

199. Z. Chi and K.K. Parhi, "A Study on the Performance, Power Consumption Tradeoffs of Short Frame Turbo Decoder Design", *Proc. of 2001 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. 4, pp. 2637-2640, Salt Lake City, Utah, May 2001

200. T. Zhang and K.K. Parhi, "A Class of Efficient-Encoding Generalized Low-Density Parity-Check Codes", *Proc. of 2001 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. 4, pp. 2477-2480, Salt Lake City, Utah, May 2001

201. T. Zhang and K.K. Parhi, "VLSI implementation-oriented (3,k)-regular low-density parity-check codes", *Proc. of 2001 IEEE Workshop on Signal Processing Systems*, pp. 25-36, Antwerp, Belgium, Sept. 26-28, 2001

202. J.-G. Chung, S.-M. Kim, and K.K. Parhi, "Sign Extension Reduction by Look-Ahead Carry Computation", *Proc. of 2001 Asilomar Conf. on Signals, Systems and Computers*, Nov. 2001

203. Y. Wang and K.K. Parhi, "A Unified Adder Design", *Proc. of 2001 Asilomar Conf. on Signals, Systems and Computers*, Nov. 2001

204. T. Zhang and K.K. Parhi, "Joint Code and Decoder Design for Implementation Oriented (3,k)-Regular LDPC Codes", *Proc. of 2001 Asilomar Conf. on Signals, Systems and Computers*, Vol. 2, pp. 1232-1236, Nov. 2001

205. K. Prasad and K.K. Parhi, "Low-Power 4-2 and 5-2 Compressors", *Proc. of 2001 Asilomar Conf. on Signals, Systems and Computers*, Vol. 1, pp. 129-133, Nov. 2001

206. Y. Chen and K.K. Parhi, "A Very Low Complexity Block Turbo Decoder Composed of Extended Hamming Codes", *Proc. of 2001 IEEE Globecom Conference*, Vol. 1, pp. 171-175, Nov. 2001, San Antonio, Texas

207. T. Zhang and K.K. Parhi, "High-Performance Decoding of Generalized Low-Density Parity-Check Codes", *Proc. of 2001 IEEE Globecom Conference*, Vol. 1, pp. 181-185, Nov. 2001, San Antonio, Texas

208. T. Zhang and K.K. Parhi, "On the High-Speed VLSI Implementation of Errors-and-Erasures Correct ing Reed-Solomon Decoders", *Proc. of 2002 Great Lakes Symp. on VLSI*, pp. 95-100, Binghamton, NY, April 2002

209. Y. Chen and K.K. Parhi, "A very low complexity soft decoding of space-time block codes", *Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 2693-2696, May 2002, Florida

210. Z. Chi and K.K. Parhi, "High Speed Algorithm and VLSI Architecture Design for Decoding BCH Product Codes", *Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, pp. 3089-3092, May 2002, Florida

211. S.-M. Kim, J.-G. Chung and K.K. Parhi, "Design of Low Error CSD Fixed-Width Multiplier", *Proc. of 2002 IEEE Int. Symp. on Circuits and Systems*, Vol. 1, pp. 69-72, Scottsdale, AZ, May 2002

212. G. Jung, J. Kim, G.E. Sobelman and K.K. Parhi, "High-Speed Add-Compare-Select Units using Locally Self-Resetting CMOS", *Proc. of 2002 IEEE Int. Symp. on Circuits and Systems*, Vol. 1, pp. 889-892, Scottsdale, AZ, May 2002

213. Z. Chi and K.K. Parhi, "High-Speed VLSI Architecture Design for Block Turbo Decoder", *Proc. of 2002 IEEE Int. Symp. on Circuits and Systems*, Vol. 1, pp. 901-904, Scottsdale, AZ, May 2002

214. Y. Chen and K.K. Parhi, "Parallel Decoding of Interleaved Single Parity Check Turbo Product Codes", *Proc. of 2002 IEEE Signal Processing Systems Workshop*, pp. 27-32, San Diego, Oct. 2002

215. K.J. Cho, K.C. Lee, J.G. Chung, K.K. Parhi, "Low Error Fixed-Width Modified Booth Multiplier", *Proc. of 2002 IEEE Signal Processing Systems Workshop*, pp. 45-50, San Diego, Oct. 2002

216. T. Zhang and K.K. Parhi, "A 54 Mbps (3,6)-Regular FPGA LDPC Decoder", *Proc. of 2002 IEEE Signal Processing Systems Workshop*, pp. 127-132, San Diego, Oct. 2002

217. Y. Chen and K.K. Parhi, "On the Performance and Implementation Implementation of Block Turbo Codes with Antenna Diversity", *Proc. of 2002 Asilomar Conf. on Signals, Systems and Computers*, Vol. 1, pp. 604-608, Nov. 2002

218. J. Kong and K.K. Parhi, "Viterbi Decoder Architecture for Interleaved Convolutional Code", *Proc. of 2002 Asilomar Conf. on Signals, Systems and Computers*, Vol. 2, pp. 1934-1937, Nov. 2002

219. J.S. Park, J.-G. Chung, and K.K. Parhi, "An Asynchronous Sample-Rate Converter From CD To DAT", *Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. 2, pp. 509-512, Hong Kong, April 2003

220. Z. Wang and K.K. Parhi, "Efficient Interleaver Memory Architectures For Serial Turbo Decoding", *Proc. of IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. 2, pp. 629-632, Hong Kong, April 2003

221. Y. Chen and K.K. Parhi, "High Throughput Overlapped Message Passing for Low Density Parity Check Codes", *Proc. of ACM/IEEE Great Lakes Symp. on VLSI*, pp. 245-248, April 2003

222. J.-S. Park, J.-G. Chung and K.K. Parhi, "High-Speed Tunable Fractional-Delay Allpass Filter Structure", *Proc. 2003 IEEE Int. Symp. on Circuits and Systems*, pp. IV-165-IV-168, Bangkok, May 2003

223. J. Kong and K.K. Parhi, "Low-Latency K-Nested Layered Look-Ahead Method and Architectures for High Throughput Rate Viterbi Decoder", *Proc. of 2003 IEEE Workshop on Signal Processing Systems*, pp. 99-104, Seoul, Korea, August 2003

224. J. Kong and K.K. Parhi, "Interleaved Cyclic Redundancy Check (CRC) Code", *Proc. of 2003 Asilomar Conf. on Signals, Systems and Computers*, **Vol. 2**, pp. 2137-2141, Pacific Grove, CA, Nov. 2003

225. J. Tang and K.K. Parhi, "On the Power Spectrum density and Parameter Choice of Multicarrier UWB Communications" *Proc. of 2003 Asilomar Conf. on Signals, Systems and Computers*, **Vol. 2**, pp. 1230-1234, Pacific Grove, CA, Nov. 2003

226. X. Zhang and K.K. Parhi, "High-Speed Architectures for Long BCH Encoders", *Proc. of 2004 ACM Great Lakes Symp. on VLSI*, pp. 1-6, Boston, April 2004

227. K.K. Parhi, "Novel Pipelining of MSB-First Add-Compare-Select Unit Structure for Viterbi Decoders", *Proc. of 2004 IEEE Int. Symp. on Circuits and Systems*, **Vol. II**, pp. 501-504, Vancouver, May 2004

228. Y. Zhang and K.K. Parhi, "Parallel Turbo Decoding", *Proc. of 2004 IEEE Int. Symp. on Circuits and Systems*, bf Vol. II, pp. 510-512, Vancouver, May 2004

229. C. Cheng and K.K. Parhi, "Hardware Efficient Fast Parallel FIR Filter Structures Based On Iterated Short Convolution", *Proc. of 2004 IEEE Int. Symp. on Circuits and Systems*, bf Vol. III, pp. 361-364, Vancouver, May 2004

230. A. Saberinia, J. Tang, A.H. Tewfik, and K.K. Parhi, "Pulsed OFDM modulation for Ultra wideband Communications", *Proc. of 2004 IEEE Int. Symp. on Circuits and Systems*, bf Vol. V, pp. 369-372, Vancouver, May 2004

231. J. Tang, A.H. Tewfik and K.K. Parhi, "High Performance Solution for Interfering UWB Piconets with Reduced Complexity Sphere Decoding", *Proc. of 2004 IEEE Int. Symp. on Circuits and Systems*, **Vol. V**, pp. 377-380, Vancouver, May 2004

232. K.K. Parhi, "Pipelining of Parallel Multiplexer Loops and Decision Feedback Equalizers", *Proc. of the 2004 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, **Vol. V**, pp. 21-24, Montreal, May 2004

233. Y. Gu and K.K. Parhi, "Interleaved Trellis Coded Modulation and Decoding for 10 Gigabit Ethernet Over Copper," *Proc. of the 2004 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, bf Vol. V, pp. 25-28, Montreal, May 2004

234. Z. Wang, Y. Chen, and K.K. Parhi, "Area-Efficient Decoding of Quasi-Cyclic Low-Density Parity Check Codes," *Proc. of the 2004 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, **Vol. V**, pp. 49-52, Montreal, May 2004

235. Y. Chen and K.K. Parhi, "Area-Efficient Parallel Decoder Architecture for Long BCH Codes", *Proc. of the 2004 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, **Vol. V**, pp. 73-76, Montreal, May 2004

236. A. Saberinia, J. Tang, A.H. Tewfik, and K.K. Parhi, "Design and Implementation of Multiband Pulsed-OFDM System for Wireless Personal Area Networks, *Proc. of 2004 IEEE Int. Conf. on communications*, **Vol. 2**, pp. 862-866, Paris, June 2004

237. K.K. Parhi, "Eliminating the Fanout Bottleneck in Parallel Long BCH Encoders", *Proc. of 2004 IEEE Int. Conf. on communications*, **Vol. 5**, pp. 2611-2615, Paris, June 2004

238. J. Tang, A.H. Tewfik and K.K. Parhi, "Reduced Complexity Sphere Decoding and Application to Interfering IEEE 802.15.3a Piconets" *Proc. of 2004 IEEE Int. Conf. on communications*, **Vol. 5**, pp. 2864-2868, Paris, June 2004

239. Y. Gu and K.K. Parhi, "Parallel Design for Parallel Decision Feedback Decoders for 10GBASE-T", *Proc. of 2004 IEEE Midwest Symp. on Circuits and Systems*, pp. II-229-II-232, Hiroshima, Japan, July 2004

240. X. Zhang and K.K. Parhi, "Fast Factorization Architecture in Soft-Decision Reed-Solomon Decoding", *Proc. of 2004 IEEE Workshop on Signal Processing Systems*, pp. 101-106, Sept. 2004, Austin (TX)

241. S.-M. Kim and K.K. Parhi, "Overlapped Decoding for a Class of Quasi-Cyclic LDPC Codes", *Proc. of 2004 IEEE Workshop on Signal Processing Systems*, pp. 113-117, Sept. 2004, Austin (TX)

242. Y. Gu and K.K. Parhi, "Complexity Reduction of the Decoders for Interleaved Trellis Coded Modulation Schemes for 10 Gigabit Ethernet over Copper", *Proc. of 2004 IEEE Workshop on Signal Processing Systems*, pp. 130-135, Sept. 2004, Austin (TX)

243. X. Zhang and K.K. Parhi, "An Efficient 21.5 Gbps AES Implementation on FPGA", *Proc. of 38th Asilomar Conference on Signals, Systems, and Computers*, Vol. 1, pp. 465-470, Nov. 2004, Pacific Grove (CA)

244. A. E. Cohen and K.K. Parhi, "Implementation of Elliptic Curve Cryptosystem Crypto-Accelerators for GF(2m̂)", *Proc. of 38th Asilomar Conference on Signals, Systems, and Computers*, Vol. 1, pp. 471-477, Nov. 2004, Pacific Grove (CA)

245. Y. Zhang, Z. Wang and K.K. Parhi, "Efficient High-Speed Quasi-Cyclic LDPC Decoder Architecture", *Proc. of 38th Asilomar Conference on Signals, Systems, and Computers*, Vol. 1, pp. 540-544, Nov. 2004, Pacific Grove (CA)

246. J. Kong and K.K. Parhi, "Quantum Convolutional Codes Design and their Encoder Architecture", *Proc. of 38th Asilomar Conference on Signals, Systems, and Computers*, Vol. 1, pp. 1131-1135, Nov. 2004, Pacific Grove (CA)

247. J. Tang and K.K. Parhi, "Viterbi Decoder for High-Speed Ultra-Wideband Communication Systems", *Proc. 2005 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. 5, pp. 37-40, Philadelphia, March 2005

248. A.E. Cohen and K.K. Parhi, "A New Reconfigurable Bit-Serial Systolic Divider for GF(2^m) and GF(p)", *Proc. 2005 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. 5, 105-108, Philadelphia, March 2005

249. Y. Gu and K.K. Parhi, "Pipelined Parallel Decision Feedback Decoders (PDFDs) for High-Speed Ethernet over Copper", *Proc. 2005 IEEE Int. Conf. on Acoustics, Speech and Signal Processing*, Vol. 5, 121-124, Philadelphia, March 2005

250. S.-M. Kim, J. Tang and K.K. Parhi, "Quasi-Cyclic Low-Density Parity-Check Coded Multiband-OFDM UWB Systems", *Proc. of 2005 IEEE Int. Symposium on Circuits and Systems*, pp. 65-68, Kobe (Japan), May 2005

251. Y. Gu and K.K. Parhi, "Pipelining Tomlinson-Harashima Precoders", *Proc. of 2005 IEEE Int. Symposium on Circuits and Systems*, pp. 408-411, Kobe (Japan), May 2005

252. C. Cheng and K.K. Parhi, "Further Complexity Reduction of Parallel FIR Filters", *Proc. of 2005 IEEE Int. Symposium on Circuits and Systems*, pp. 1835-1838, Kobe (Japan), May 2005

253. J. Lin and K.K. Parhi, "VLSI Architectures for Stereoscopic Video, Disparity Matching and Object Extraction", *Proc. of 2005 IEEE Int. Symposium on Circuits and Systems*, pp. 2373-2376, Kobe (Japan), May 2005

254. C. Cheng and K.K. Parhi, "Low-Cost Parallel Adaptive Filter Structures", *Proc. of 39th Asilomar Conference on Signals, Systems, and Computers*, pp. 354-358, Nov. 2005, Pacific Grove, CA

255. M. Yadav and K.K. Parhi, "Design and Implementation of LDPC Codes for DVB-S2", *Proc. of 39th Asilomar Conference on Signals, Systems, and Computers*, pp. 723-728, Pacific Grove, CA, Oct. 2005

256. J. Chen, Y. Gu and K.K. Parhi, "MIMO Equalization and Cancellation for 10Gbase-T", *Proc. of 2006 IEEE Int. Conf. Acoustics, Speech and Signal Processing*, pp. IV-637-IV-640, Toulouse (France), May 2006

257. J. Lee, S. Park, Y. Zhang, K.K. Parhi, and S.-C. Park, "Implementation Issues of a List Sphere Decoder", *Proc. of 2006 IEEE Int. Conf. Acoustics, Speech and Signal Processing*, pp. III-996-III-999, Toulouse (France), May 2006

258. S. Park, K. Lee, Y. Zhang, K.K. Parhi, J. Lee, S.-C. Park, "Probabilistic List Sphere Decoding for LDPC-Coded MIMO-OFDM Systems", *Proc. of 2006 IEEE Int. Conf. Acoustics, Speech and Signal Processing*, pp. III-912-III-915, Toulouse (France), May 2006

259. Z. Wang, Y. Zhang and K.K. Parhi, "Study of Early Stopping Criteria for Turbo Decoding and Their Applications in WCDMA Systems", *Proc. of 2006 IEEE Int. Conf. Acoustics, Speech and Signal Processing*, pp. III-1016-III-1019, Toulouse (France), May 2006

260. A.E. Cohen and K.K. Parhi, "Faster elliptic curve point multiplication based on a novel greedy base-2,3 method", *Proc. of 2006 IEEE Int. Symp. on Circuits and Systems*, pp. 3374-3377, Kos (Greece), May 2006

261. J. Lin and K.K. Parhi, "Low-Complexity Block Turbo Equalization", *Proc. of 2006 IEEE Int. Symp. on Circuits and Systems*, pp. 5091-5094, Kos (Greece), May 2006

262. J. Tang, T. Bhatt, V. Sundaramurthy, "Reconfigurable Shuffle Network Design in LDPC Decoders", *Proc. of 2006 IEEE Conf. on Applications-Specific Architectures, Systems, and Processors*, pp. 81-86, Steamboat Springs (CO), Sept. 2006

263. D. Oh and K.K. Parhi, "Low Complexity Design of High-Speed Parallel Decision Feedback Equalizers", *Proc. of 2006 IEEE Conf. on Applications-Specific Architectures, Systems, and Processors*, pp. 118-122, Steamboat Springs (CO), Sept. 2006

264. Y. Zhang, J. Tang and K.K. Parhi, "Low-Complexity List Updating Circuits for List Sphere Decoders", *Proc. 2006 IEEE Workshop on Signal Processing Systems*, pp. 28-33, Banff, canada, Oct. 2006

265. J. Lin and K.K. Parhi, "Low Complexity Iterative Joint Detection, Decoding, and Channel Estimation for Wireless MIMO System", *Proc. 2006 IEEE Workshop on Signal Processing Systems*, pp. 45-50, Banff, canada, Oct. 2006

266. J. Chen and K.K. Parhi, "Adaptive Tap Management in Multi-Gigabit Echo and NEXT Cancellers", *Proc. 2006 IEEE Workshop on Signal Processing Systems*, pp. 415-419, Banff, canada, Oct. 2006

267. D. Oh and K.K. Parhi, "Low-Complexity Implementations of Sum-Product Algorithm for Decoding Low-Density Parity Check Codes", *Proc. 2006 IEEE Workshop on Signal Processing Systems*, pp. 262-267, Banff, canada, Oct. 2006

268. J. Lin and K.K. Parhi, "High-Speed Error Resilient Stereoscopic Video Coder", *Proc. of 40th Asilomar Conf. on Signals, Systems and Computers*, Oct. 2006, pp. 1054-1058, Pacific Grove, CA

269. A.E. Cohen and K.K. Parhi, "New Side Channel Resistant Scalar Point Multiplication Method for Binary Elliptic Curves", *Proc. of 40th Asilomar Conf. on Signals, Systems and Computers*, Oct. 2006, pp. 1205-1209, Pacific Grove, CA

270. Y. Zhang and K.K. Parhi, "High-Throughput Radix-4 LogMAP Turbo Decoder Architecture", *Proc. of 40th Asilomar Conf. on Signals, Systems and Computers*, Oct. 2006, pp. 1711-1715, Pacific Grove, CA

271. Y. Zhang, J. Tang and K.K. Parhi, "Low Complexity Radius Reduction Method for List Sphere Decoders", *Proc. of 40th Asilomar Conf. on Signals, Systems and Computers*, Oct. 2006, pp. 2200-2203, Pacific Grove, CA

272. J. Chen and K.K. Parhi, "Fast Computation of MIMO Equalizers and Cancellers in 10GBASE-T Channels", *IEEE Int. Conf. Acoustics, Speech and Signal Processing*, pp. III-201-III-204, April 2007, Hawaii

273. A.E. Cohen and K.K. Parhi "Side channel resistance quantification and verification", *Proc. of 2007 IEEE Int. Conf. Electro/Information Technology*, pp. 130-134, May 2007

274. D. Oh and K.K. Parhi, "Efficient Highly-Parallel Decoder Architecture For Quasi-Cyclic Low-Density Parity-Check Codes", *2007 IEEE Int. Symp. on Circuits and Systems*, pp. 1855-1858, New Orleans, May 2007

275. D. Oh and K.K. Parhi, "Performance of Quantized Min-Sum Decoding Algorithms for Irregular LDPC Codes", *2007 IEEE Int. Symp. on Circuits and Systems*, pp. 2758-2761, New Orleans, May 2007

276. Y. Zhang and K.K. Parhi, "Parallel Processing for List Sphere Decoders", *2007 IEEE Int. Symp. on Circuits and Systems*, pp. 2096-2099, New Orleans, May 2007

277. D. Oh and K.K. Parhi, "Area Efficient Controller Design of Barrel Shifters for Reconfigurable LDPC Decoders", *Proc. of 2008 IEEE Int. Symp. on Circuits and Systems*, pp. 240-243, Seattle, May 2008

278. D. Oh and K.K. Parhi, "Nonuniformly Quantized Min-Sum Decoder Architecture for Low-Density Parity-Check Codes", *Proceedings of the ACM 2008 Great Lakes Symposium on VLSI*, May 2008

279. R. Liu and K.K. Parhi, "Fast Composite Field S-Box Architectures for Advanced Encryption Standard", *Proceedings of the ACM 2008 Great Lakes Symposium on VLSI*, May 2008

280. J. Chen and K.K. Parhi, "Further Cost Reduction of Adaptive and NEXT Cancellers for High-Speed Ethernet Transceivers", *Proc. of 2008 IEEE Workshop on Signal Processing Systems*, pp. 227-232, Washington, D.C., Oct. 2008

281. R. Liu and K.K. Parhi, "Minimal Complexity Low-Latency Architectures for Viterbi Decoders", *Proc. of 2008 IEEE Workshop on Signal Processing Systems*, Washington, D.C., pp. 140-145, Oct. 2008

282. C. Cheng and K.K. Parhi, "High-Speed Implementation of Smith-Waterman Algorithm for DNA Sequence Scanning in VLSI", *Proc. 2008 Asilomar Conf. on Signals, Systems and Computers*, pp. 1528-1533, Pacific Groves, CA, Oct. 2008

283. J. Chen and K.K. Parhi, "New Stable IIR Modeling of Long FIR filters with Low Complexity", *Proc. 2008 Asilomar Conf. on Signals, Systems and Computers*, pp. 1649-1653, Pacific Groves, CA, Oct. 2008

284. D. Oh and K.K. Parhi, "Optimally Quantized Offset Min-Sum Algorithm for Flexible LDPC Decoder", *Proc. 2008 Asilomar Conf. on Signals, Systems and Computers*, pp. 1886-1891, Pacific Groves, CA, Oct. 2008

285. Y. Liu, T. Zhang and K.K. Parhi, "Analysis of Voltage Overscaled Computer Arithmetics in Low Power Signal Processing Systems", *Proc. 2008 Asilomar Conf. on Signals, Systems and Computers*, pp. 2093-2097, Pacific Groves, CA, Oct. 2008

286. J. Chen and K.K. Parhi, "Further Cost Reduction of Adaptive and NEXT Cancellers for High-Speed Ethernet Transceivers", Proc. of 2008 IEEE Workshop on Signal Processing Systems, pp. 227-232, Washington, D.C., Oct. 2008

287. R. Liu and K.K. Parhi, "Low-Power Frequency-Selective Filtering", *Proc. of 2009 IEEE Int. Symp. on Circuits and Systems*, pp. 245-248, May 2009, Taipei

288. R. Liu and K.K. Parhi, "Noise-reduction for Low-Power Broadband Filtering", *Proc. of 2009 IEEE Int. Symp. on Circuits and Systems*, pp. 1012-1015, May 2009, Taipei

289. X. Zhu, K.K. Parhi and W. Warwick, "Detecting Changes in Respiratory Patterns in High Frequency Chest Compression Therapy by Single-Channel Blind Source Separation", *Proc. of 2009 IEEE Engineering in Medicine and Biology Society Conference*, pp. 2523-2526, Sept. 2009, Minneapolis, MN

290. T. Netoff, Y. Park and K.K. Parhi, "Seizure Prediction using Cost-Sensitive Support Vector Machine", *Proc. of 2009 IEEE Engineering in Medicine and Biology Society Conference*, pp. 3322-3325, Sept. 2009, Minneapolis, MN

291. J. Lee, Y.W. Lee, G. O'Clock, X. Zhu, K. Parhi, W. Warwick, "Induced Respiratory System Modeling by High Frequency Chest Compression Using Lumped System Identification Method", *Proc. of 2009 IEEE Engineering in Medicine and Biology Society Conference*, pp. 5486-5489, Sept. 2009, Minneapolis, MN

292. R. Liu and K.K. Parhi, "Sparse Severe Error Removal in OFDM Demodulators for Erasure Channels", *Proc. of 2009 IEEE Workshop on Signal Processing Systems*, pp. 1-6, Tampere, Finland, Oct. 2009

293. Y. Sun, J. Chen and K.K. Parhi, "Multi-delay Block Frequency Domain Adaptive Filters with Sparse Partial Subblock Update", *Proc. 2009 Asilomar Conf. on Signals, Systems and Computers*, Pacific Groves, CA, Nov. 2009

294. X. Zhu, K.K. Parhi and W. Warwick, "Blind Source Separation with Low Frequency Compensation for Convolutive Mixtures", *Proc. 2009 Asilomar Conf. on Signals, Systems and Computers*, Pacific Groves, CA, Nov. 2009

295. C. Cheng and K.K. Parhi, "High Speed VLSI Architecture for General Linear Feedback Shift Register (LFSR) Structures", *Proc. 2009 Asilomar Conf. on Signals, Systems and Computers*, Pacific Groves, CA, Nov. 2009

296. A. Shea, B. Fett, M. Riedel and K. Parhi, "Synthesizing Sequential Register-Based Computation with Biochemistry", *Proc. of 2009 IEEE Int. Conf. on Computer Aided Design*, pp. 136-143, Nov. 2009

297. H. Patil and K.K. Parhi, "Variable Length Teager Energy Based Mel Cepstral Features for Identification of Twins", *Proc. of 3rd Int. Conf. on Pattern Recognition and Machine Intelligence*, Dec. 2009, New Delhi (India)

298. J. Yang, X. Zhu, G.E. Sobelman and K.K. Parhi, "Sparseness-Controlled Adaptive Tap Algorithms for Partial Update Adaptive Filters", *Proc. of 7th Int. Conf. Informations, Communications and Signal Processing (ICICS)*, Dec. 2009, Hong Kong

299. A. Shea, B. Fett, M.D. Riedel, and K. Parhi, "Writing and Compiling Code into Biochemistry", *Proc. 2010, Pacific symposium on Biocomputing (PSB)*, Vol. 15, pp. 456-464, Jan. 2010

300. X. Zhu and K.K. Parhi, "Underdetermined Blind Source Separation Based on Continuous Density", *Proc. 2010 IEEE Int. Conf. on Acoustics, Speech and Signal Processing (ICASSP)*, pp. 4126-4129, March 2010, Dallas

301. H. Patil and K.K. Parhi, "Novel Variable Length Teager Energy Based Features for Person Recognition from their Hum", *Proc. 2010 IEEE Int. Conf. on Acoustics, Speech and Signal Processing (ICASSP)*, pp. 4526-4529, March 2010, Dallas

302. Y. Park, T. Netoff and K.K. Parhi, "Seizure Prediction with Spectral Power of timespace-differential EEG signals using cost-sensitive support vector machine", *Proc. 2010 IEEE Int. Conf. on Acoustics, Speech and Signal Processing (ICASSP)*, pp. 5450-5453, March 2010, Dallas

303. H.A. Patil and K.K. Parhi, "Development of TEO Phase for Speaker Recognition", *International Conference on Signal Processing and Communications - 2010 (SPCOM 2010)*, pp.1-5, Bangalore, July 2010

304. A.E. Cohen and K.K. Parhi, "GPU Accelerated Elliptic Curve Cryptography in GF(2^m)", *Proc. 2010 Midwest Symp. on Circuits and Systems*, pp. 57-60, Aug. 2010, Seattle, Washington

305. M. Ayinala and K.K. Parhi, "Efficient Parallel VLSI Architecture for Linear Feedback Shift Registers", *Proc. of 2010 IEEE Workshop on Signal Processing Systems*, pp. 52-57, Fremont, CA, Oct. 2010

306. H. Jiang, M. Riedel, and K.K. Parhi, "Digital Signal Processing with Biomolecular Reactions", *Proc. of 2010 IEEE Workshop on Signal Processing Systems*, pp. 237-242, Fremont, CA, Oct. 2010

307. H. Jiang, A. Kharam, M. Riedel and K.K. Parhi, "A Synthesis Flow for Digital Signal Processing with Biomolecular Reactions", *Proc. of 2010 IEEE Int. Conf. on Computer Aided Design*, pp. 417-424, Nov. 2010

308. P. Metkar, A.E. Cohen and K.K. Parhi, "Improved Approach for Calculating Model Parameters in Speaker Recognition Using Gaussian Mixture Models", *Proc. 2010 Asilomar Conf. on Signals, Systems and Computers*, pp. 567-570, Pacific Grove, CA, Nov. 2010

309. M. Ayinala and K.K. Parhi, "Parallel - Pipelined Radix-2^2 FFT Architecture for Real Valued Signals", *Proc. 2010 Asilomar Conf. on Signals, Systems and Computers*, pp. 1274-1278, Pacific Grove, CA, Nov. 2010

310. A. Kharam, H. Jiang, M. Riedel, and K.K. Parhi, "Binary Counting with Chemical Reactions", *Proc. of 2011 Pacific Symp. on Biocomputing*, Vol. 16, pp. 302-313, Jan. 2011, Hawaii

311. Y. Lao and K.K. Parhi, "Novel Reconfigurable Silicon Physical Unclonable Functions", *Proc. of 2011 Workshop on the Foundations of Dependable and Secure Cyber-Physical Systems (FDSCPS-11)*, pp. 30-36, April 2011, Chicago

312. Y. Lao and K.K. Parhi, "Reconfigurable Architectures for Silicon Physical Unclonable Functions", *2011 IEEE International Conference on Electro Information Technology*, Mankato, May 2011

313. T. Kung and K.K. Parhi, "Frequency Domain Symbol Synchronization for OFDM Systems", *2011 IEEE International Conference on Electro Information Technology*, Mankato, May 2011

314. H. Jiang, M.D. Riedel and K.K. Parhi, "Synchronous Sequential Computation with Molecular Reactions", *Proc. of ACM IEEE Design Automation Conference*, pp. 836-841, San Diego, CA, June 2011

315. H.A. Patil, M.C. Madhavi, and K.K. Parhi, "Combining Evidence from Spectral and Source-like Features for Person Recognition from Humming", *Proc. of 12th International Speech Communication Association (Interspeech)*, Florence, Italy, Aug. 2011

316. M.J. Brown, T. Netoff and K.K. Parhi, "A Low-Complexity Seizure Prediction Algorithm", *Proc. of 33rd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'11)*, pp. 1640-1643, Boston, Aug. 2011

317. H. Jiang, M.D. Reidel, and K.K. Parhi, "Asynchronous Computations with Molecular Reactions", *Proc. 2011 Asilomar Conf. on Signals, Systems and Computers*, pp. 493-497, Pacific Grove, CA, Nov. 2011

318. M. Ayinala and K.K. Parhi, "Parallel Pipelined FFT Architectures with Reduced Number of Delays," *Proc. of ACM Great Lakes Symp. on VLSI*, pp. 63-66, Salt Lake City, Utah, May 2012

319. S.A. Salehi, R. Amirfattahi, and K.K. Parhi, "Efficient Folded VLSI Architectures for Linear Prediction Error Filters," *Proc. of ACM Great Lakes Symp. on VLSI*, pp. 357-362, Salt Lake City, Utah, May 2012

320. C. Zhang, B. Yuan, and K.K. Parhi, "Reduced-Latency SC Polar Decoder Architectures," *Proc. of IEEE Int. Conf. Communications*, pp. 3520-3524, Ottawa, June 2012

321. M. Ayinala and K.K. Parhi, "Low complexity algorithm for seizure prediction using Adaboost," *IEEE Int. conference on Engineering in Medicine and Biology Society*, pp. 1061-1064, San Diego, August 2012

322. T. Xu, M. Stephane and K.K. Parhi, "Selection of Abnormal Neural Oscillation Patterns Associated with Language Disorder in Schizophrenia," *IEEE Int. conference on Engineering in Medicine and Biology Society*, pp. 4293-4296, San Diego, August 2012

323. Y.-S. Park, T. Netoff, X. Yang, and K.K. Parhi, "Seizure Detection On/Off System using Rats' ECoG," *IEEE Int. conference on Engineering in Medicine and Biology Society*, pp. 4688-4691, San Diego, August 2012

324. K.K. Parhi, "Verifying Equivalence of Digital Signal Processing Circuits," *Proc. of 2012 Asilomar Conf. on Signals, Systems and Computers*, pp. 99-103, Pacific Grove, CA, Nov. 2012 (Invited talk)

325. Y.S. Park, T. Netoff and K.K. Parhi, "Reducing the Number of Features for Seizure Prediction of Spectral Power in Intracranial EEG," *Proc. of 2012 Asilomar Conf. on Signals, Systems and Computers*, pp. 770-774, Pacific Grove, CA, Nov. 2012

326. S. Roychowdhury, D. Koozekanani, and K.K. Parhi, "Screening Fundus Images for Diabetic Retinopathy," *Proc. of 2012 Asilomar Conf. on Signals, Systems and Computers*, pp. 1641-1645, Pacific Grove, CA, Nov. 2012

327. B. Yuan and K.K. Parhi, "Architecture Optimizations for BP Polar decoders," *Proc. of 2013 IEEE International Conference on Acoustics, Speech and Signal Processing*, pp. 2654-2658, Vancouver, May 2013

328. Y.-N. Chang and K.K. Parhi, "Architectures for Digital Filters using Stochastic Computing," *Proc. of 2013 IEEE International Conference on Acoustics, Speech and Signal Processing*, pp. 2697-2701, Vancouver, May 2013

329. S. Roychowdhury, D. Koozekanani, S. Radwan, and K.K. Parhi, "Automated Localization of Cysts in Diabetic Macular Edema using Optical Coherence Tomography Images," *Proc. of 2013 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 1426-1429, Osaka, July 2013

330. M. Bandarabadi, A. Dourado, C. Teixeira, T. Netoff, and K.K. Parhi, "Seizure Prediction with Bipolar Spectral Power Features using Adaboost and SVM Classifiers," *Proc. of 2013 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 6305-6308, Osaka, July 2013

331. H. Jiang, M.D. Riedel, and K.K. Parhi, "Digital Logic with Molecular Reactions," *Proc. of 2013 IEEE International Conference on Computer Aided Design (ICCAD)*, pp. 721-727, San Jose, CA, Nov. 2013

332. T. Xu, M. Stephane and K.K. Parhi, "Classification of Single-Trial MEG during Sentence Processing for Automated Schizophrenia Screening," *Proc. of 6th International IEEE EMBS Conference on Neural Engineering*, pp. 363-366, San Diego, Nov. 2013

333. S. Roychowdhury, D. Koozekanani and K.K. Parhi, "Automated Denoising and Segmentation of Optical Coherence Tomography Images," *Proc. 2013 Asilomar Conference on Signals, Systems and Computers*, pp. 258-262, Pacific Grove, CA, November 2013

334. T. Xu, M. Stephane and K.K. Parhi, "Classification of Single-Trial MEG during Sentence Processing for Automated Schizophrenia Screening," *Proc. 2013 Asilomar Conference on Signals, Systems and Computers*, pp. 354-357, Pacific Grove, CA, November 2013

335. M. Ayinala and K.K. Parhi, "Low-Energy Architectures for Support Vector Machine Computation," *Proc. 2013 Asilomar Conference on Signals, Systems and Computers*, pp. 2167-2171, Pacific Grove, CA, November 2013

336. K.K. Parhi, "VLSI Systems for Neurocomputing and Health Informatics," *Keynote Talk at 2014 ACM Great Lakes Symposium on VLSI*, pp. 1-2, Houston, May 2014

337. B. Yuan and K.K. Parhi, "Architectures for Polar BP Decoders Using Folding," *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 205-208, Melbourne, Australia, June 2014

338. K.K. Parhi and Y. Liu, "Architectures for IIR Digital Filters Using Stochastic Computing," *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 373-376, Melbourne, Australia, June 2014

339. C. Zhang and K.K. Parhi, "Interleaved Successive Cancellation Polar Decoders," *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 401-404, Melbourne, Australia, June 2014

340. Y. Lao and K.K. Parhi, "Protecting DSP Circuits Through Obfuscation," *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 798-801, Melbourne, Australia, June 2014

341. Z. Zhang and K.K. Parhi, "Seizure Detection using Wavelet Decomposition of the Prediction Error Signal from a Single Channel of Intra-Cranial EEG," *Proc. of 2014 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 4443-4446, Aug. 2014, Chicago, IL

342. M. Bandarabadi, C. Teixeira, T. Netoff, K.K. Parhi, and A. Dourado, "Robust and Low Complexity Algorithms for Seizure Detection," *Proc. of 2014 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 4447-4450, Aug. 2014, Chicago, IL

343. T. Xu, K.R. Cullen, A. Houri, K.O. Lim, S.C. Schulz, and K.K. Parhi, "Classification of Borderline Personality Disorder based on Spectral Power of Resting-State fMRI," *Proc. of 2014 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 5036-5039, Aug. 2014, Chicago, IL

344. Q. Tang, B. Kim, Y. Lao, K.K. Parhi and C. Kim, "True Random Number Generator Circuits Based on Single- and Multi-Phase Beat Frequency Detection," *Proc. of 2014 IEEE Customs Integrated Circuits Conference*, September 2014, San Jose, CA

345. B. Yuan and K.K. Parhi, "Successive Cancellation List Polar Decoder using Log-likelihood Ratios," *Proc. 2014 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 2014

346. M. Parhi, Y. Lao and K.K. Parhi, "Canonic Real Valued FFT Structures," *Proc. 2014 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 2014

347. S.A. Salehi, M.D. Riedel, and K.K. Parhi, "Asynchronous Discrete-time Signal Processing with Molecular Reactions," *Proc. 2014 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 2014

348. B. Yuan and K.K. Parhi, "Algorithm and Architecture for Hybrid Decoding of Polar Codes," *Proc. 2014 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 2014

349. S. Chu, C. Lenglet and K.K. Parhi, "Brain connectivity from diffusion and functional MRI using a network flow model," *Proc. of 2015 SPIE Medical Imaging Conference*, Feb. 2015, Orlando, FL

350. Y. Liu and K.K. Parhi, "Lattice FIR Digital Filters using Stochastic Computing," *Proc. of 2015 IEEE Int. Conf. Acoustics, Speech and Signal Processing (ICASSP)*, pp. 1027-1031, Brisbane, Australia, April 2015

351. G.N.C. Shanmugam, Y. Lao and K.K. Parhi, "An Obfuscated Radix-2 Real FFT Architecture," *Proc. of 2015 IEEE Int. Conf. Acoustics, Speech and Signal Processing (ICASSP)*, pp. 1056-1060, Brisbane, Australia, April 2015

352. A. Chinnapalanichamy and K.K. Parhi, "Serial and Interleaved Architectures for Computing Real FFT," *Proc. of 2015 IEEE Int. Conf. Acoustics, Speech and Signal Processing (ICASSP)*, pp. 1066-1070, Brisbane, Australia, April 2015

353. B. Yuan and K.K. Parhi, "Successive Cancellation Decoding of Polar Codes Using Stochastic Computing," *Proc. of 2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, May 2015

354. R. Parhi, C.H. Kim,and K.K. Parhi, "Fault-Tolerant Ripple-Carry Binary Adder Using Partial Triple Modular Redundancy (PTMR)," *Proc. of 2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, May 2015

355. B. Yuan and K.K. Parhi, ""Reduced-latency LLR-based SC List Decoder for Polar Codes," *Proc. of 2015 ACM Great Lakes Symposium on VLSI*, pp. 107-110, Pittsburgh, May 2015

356. M. Parhi, M.D. Riedel, and K.K. Parhi, "Effect of Bit-Level Correlation in Stochastic Computing," *Proc. 2015 IEEE International Conference on Digital Signal Processing (DSP)*, pp. 463-467, Singapore, July 2015

357. S.A. Salehi, M.D. Riedel, and K.K. Parhi, "Markov Chain Computations using Molecular Reactions," *Proc. 2015 IEEE International Conference on Digital Signal Processing (DSP)*, pp. 689-693, Singapore, July 2015

358. S. Roychowdhury, D.D. Koozekanani, M. Reinsbach, K.K. Parhi, "3-D Localization of Diabetic Macular Edema using OCT Thickness Maps," *Proc. of 2015 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 4334-4337, Milan, Italy, August 2015

359. Z. Zhang and K.K. Parhi, "Seizure Prediction using Polynomial SVM Classification," *Proc. of 2015 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 5748-5751, Milan, Italy, August 2015

360. Z. Zhang and K.K. Parhi, "Seizure Detection using Regression Tree Based Feature Selection and Polynomial SVM Classification," *Proc. of 2015 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 6578-6581, Milan, Italy, August 2015

361. Y. Lao and K.K. Parhi, "Canonic Real-Valued Radix-2n̂ FFT Computations," *Proc. 2015 Asilomar Conference on Signals, Systems and Computers*, pp. 441-446, Pacific Grove, CA, Nov. 2015

362. Z. Zhang, T.R. Henry and K.K. Parhi, "Seizure Prediction using Cross-Correlation and Classification," *Proc. 2015 Asilomar Conference on Signals, Systems and Computers*, pp. 775-779, Pacific Grove, CA, Nov. 2015

363. Y. Liu and K.K. Parhi, "Architectures for Stochastic Normalized and Modified Lattice IIR Filters," *Proc. 2015 Asilomar Conference on Signals, Systems and Computers*, pp. 1351-1358, Pacific Grove, CA, Nov. 2015 *Invited Talk*

364. S. Koteshwara, C.H. Kim and K.K. Parhi, "Mode-based Obfuscation using Control-Flow Modifications," *Proc. of Third Workshop on Cryptography and Security in Computing Systems (CS2)*, pp. 19-24, Prague, Jan. 20, 2016

365. S.V.S. Avvaru, C. Zhou, S. Satapathy, Y. Lao, C. Kim and K.K. Parhi, "Estimating Delay Differences of Arbiter PUFs Using Silicon Data," *Proc. of 2016 Design, Automation, Test in Europe (DATE)*, pp. 543-546, March 2016, Dresden

366. B. Yuan and K.K. Parhi, "Belief Propagation Decoding of Polar Codes using Stochastic Computing," *Proc. of 2016 Int. Symp. on Circuits and Systems*, Montreal, May 2016

367. Y. Liu and K.K. Parhi, "Computing Complex Functions using Factorization in Unipolar Stochastic Logic," *Proc. of 2016 ACM Great Lakes Symposium on VLSI*, Boston, MA, May 2016

368. C. Zhou, S. Satapathy, Y. Lao, K.K. Parhi and C.H. Kim, "oft Response Generation and Thresholding Strategies for Linear and Feed-Forward MUX PUFs," *Proc. of 2016 ACM/IEEE International Symposium on Low Power Electronics and Design*, pp. 124-129, San Francisco, Aug. 2016

369. S. Roychowdhury, D.D. Koozekanani, and K.K. Parhi, "Automated Detection of Neovascularization for Proliferative Diabetic Retinopathy Screening," *Proc. of 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp. 1300-1303, Orlando, FL, August 2016

370. V. Vijayakumar, D.D. Koozekanani, S. Roychowdhury and K.K. Parhi, "Artery/Vein Classification of Retinal Blood Vessels using Feature Selection," *Proc. of 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp. 1320-1323, Orlando, FL, August 2016

371. B. Sen, G. Bernstein, T. Xu, B. Mueller, M.W. Schreiner, K.R. Cullen, K.K. Parhi, "Classification of Obsessive-Compulsive Disorder from Resting-State fMRI," *Proc. of 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp. 3606-3609, Orlando, FL, August 2016

372. Y. Liu, H. Venkataraman, Z. Zhang and K.K. Parhi, "Machine Learning Classifiers using Stochastic Logic," *Proc. 2016 IEEE Int. Conf. on Computer Design*, pp. 408-411, Phoenix, AZ, Oct. 2016

373. Y. Lao and K.K. Parhi, "Data-Canonic Real FFT Flow-Graphs for Composite Lengths," *Proc. 2016 IEEE Workshop on Signal Processing Systems*, pp. 189-194, Dallas, Oct. 2016

374. Y. Liu and K.K. Parhi, "Computing RBF Kernel for SVM Classification using Stochastic Logic," *Proc. 2016 IEEE Workshop on Signal Processing Systems*, pp. 327-332, Dallas, Oct. 2016

375. Y. Liu, M. Parhi and K.K. Parhi, "Synthesis of Correlated Bit Streams for Stochastic Computing," *Proc. 2016 Asilomar Conference on Signals, Systems and Computers*, pp. 167-174, Pacific Grove, CA, Nov. 2016

376. Z. Zhang and K.K. Parhi, "Seizure Prediction using Long-Term Fragmented Intracranial Canine and Human EEG Recordings," *Proc. 2016 Asilomar Conference on Signals, Systems and Computers*, pp. 361-365, Pacific Grove, CA, Nov. 2016

377. Y. Liu and K.K. Parhi, "Computing Hyperbolic Tangent and Sigmoid Functions using Stochastic Logic," *Proc. 2016 Asilomar Conference on Signals, Systems and Computers*, pp. 1580-1585, Pacific Grove, CA, Nov. 2016

378. S.A. Salehi, K.K. Parhi, M.D. Riedel, "Computing Polynomials by Chemical Reaction Networks," *Proc. 2016 IEEE Globecom Symposium*, Washington, D.C., Dec. 2016

379. B. Sen and K.K. Parhi, "Extraction of Common Task Signals and Spatial Maps from Group fMRI using a PARAFAC-Based Tensor Decomposition Technique," *Proc. 2017 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, New Orleans, Louisiana, pp. 1113-1117, March 2017

380. Q. Tang, C. Zhou, W. Choi, G. Kang, J. Park, K. Parhi, and C.H. Kim, "A DRAM based Physical Unclonable Function Capable of Generating $> 10^{32}$ Challenge Response Pairs per 1Kbit Array for Secure Chip Authentication," *Proc. 2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, Texas, April 30-May 3, 2017

381. S.A. Salehi, Y. Liu, M.D. Riedel and K.K. Parhi, "Computing Polynomials with Positive Coefficients using Stochastic Logic by Double-NAND Expansion," *Proc. 2017 ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 471-474, Banff, Canada, May 2017

382. K.K. Parhi, "Analysis of Stochastic Logic Circuits in Unipolar, Bipolar and Hybrid Formats," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017

383. S. Koteshwara, A. Das and K.K. Parhi, "FPGA Implementation and Comparison of AES-GCM and Deoxys Authenticated Encryption Schemes," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017

384. S. Koteshwara, C.H. Kim, and K.K. Parhi, "Hierarchical Functional Obfuscation of Integrated Circuits Using a Mode-Based Approach," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017

385. A. Koyily, C. Zhou, C.H. Kim, and K.K. Parhi, "An Entropy Test for Determining Whether a Mux PUF Is Linear or Nonlinear," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017

386. C. Zhou, K.K. Parhi, and C.H. Kim, "Secure and Reliable XOR Arbiter PUF Design: An Experimental Study based on 1 Trillion Challenge Response Pair Measurements," *Proc. 2017 Design Automation Conference (DAC)*, Austin, Texas, June 2017

387. M. Liu, C. Zhou, Q. Tang, K.K. Parhi and C.H. Kim, "A Data Remanence based Approach to Generate 100% Stable Keys from an SRAM Physical Unclonable Function," *Proc. of 2017 IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, Taipei, Taiwan, July 2017

388. S.V. Sandeep Avvaru, C. Zhou, C.H. Kim and K.K. Parhi, "Predicting Hard and Soft-Responses and Identifying Stable Challenges of Mux PUFs Using ANN," *Proc. of 2017 IEEE Midwest Symp. on Circuits and Systems*, pp. 934-937, Boston, August 2017

389. S.A. Salehi, M.D. Riedel, and K.K. Parhi, "Molecular Computation of Complex Markov Chains with Self-Loop State Transitions," *Proc. 2017 Asilomar Conference on Signals, Systems and Computers*, pp. 478-483, Pacific Grove, CA, Oct. 29-Nov. 1, 2017

390. S. Koteshwara, C.H. Kim, and K.K. Parhi, "Functional Encryption of Integrated Circuits by Key-Based Dynamic Hybrid Obfuscation," *Proc. 2017 Asilomar Conference on Signals, Systems and Computers*, pp. 484-488, Pacific Grove, CA, Oct. 29-Nov. 1, 2017

391. S. Koteshwara, A. Das and K.K. Parhi, "Performance Comparison of AES-GCM-SIV and AES-GCM Algorithms for Authenticated Encryption on FPGA Platforms," *Proc. 2017 Asilomar Conference on Signals, Systems and Computers*, pp. 1331-1336, Pacific Grove, CA, Oct. 29-Nov. 1, 2017

392. A. Koyily, S.V.S. Avvaru, C. Zhou, C.H. Kim and K. K. Parhi, "Effect of Aging on Linear and Nonlinear MUX PUFs by Statistical Modeling," *Proc. of 23rd Asia and South Pacific Design Automation Conference*, pp. 76-83, Jeju Island, Korea, Jan. 2018

393. A. Koyily, C. Zhou, C.H. Kim and K.K. Parhi, "Predicting Soft-Response of Mux PUFs via Logistic Regression of Total Delay Difference," *Proc. of 2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018

394. Q. Tang, W.H. Choi, L. Everson, K.K. Parhi and C.H. Kim, "A Physical Unclonable Function Based on Capacitor Mismatch in a Charge-Redistribution SAR-ADC," *Proc. of 2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018

395. S. Koteshwara and K.K. Parhi, "Low-Energy Architectures of Linear Classifiers for IoT Applications using Incremental Precision and Multi-Level Classification," *Proc. 2018 ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 291-296, Chicago, May 2018

396. S. Chu, C. Lenglet, M.W. Schreiner, B. Klimes-Dougan, K.R. Cullen and K.K. Parhi, "Classifying Treated vs. Untreated MDD Adolescents from Anatomical Connectivity using Nonlinear SVM," *Proc. of 2018 IEEE Engineering in Medicine and Biology Conference (EMBC)*, pp. 1-4, July 2018, Hawaii

397. S. Chu, C. Lenglet, M.W. Schreiner, B. Klimes-Dougan, K.R. Cullen and K.K. Parhi, "Biomarkers for Adolescent MDD from Anatomical Connectivity and Network Topology Using Diffusion MRI," *Proc. of 2018 IEEE Engineering in Medicine and Biology Conference (EMBC)*, pp. 1152-1155, July 2018, Hawaii

398. S. Chu, C. Lenglet, M.W. Schreiner, B. Klimes-Dougan, K.R. Cullen and K.K. Parhi, "Anatomical Biomarkers for Adolescent Major Depressive Disorder from Diffusion Weighted Imaging using SVM Classifier," *Proc. of 2018 IEEE Engineering in Medicine and Biology Conference (EMBC)*, pp. 2740-2743, July 2018, Hawaii

399. A. Rashno, D.D. Koozekanani, and K.K. Parhi, "Segmentation of Various Types of Fluids with Graph Shortest Path and Convolutional Neural Network," *Proc. of 2018 IEEE Engineering in Medicine and Biology Conference (EMBC)*, pp. 3426-3429, July 2018, Hawaii

400. C. Deng, S. Liao, Y. Xie, K.K. Parhi, X. Qian, and B. Yuan, "PermDNN: Efficient Compressed Deep Neural Network Architecture with Permuted Diagonal Matrices," *Proc. 51st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 189-202, Fukuoka, Japan, Oct. 20-24, 2018

401. S. Chu, C. Lenglet, M.W. Schreiner, B. Klimes-Dougan, K.R. Cullen, and K.K. Parhi, "Altered Structural Connection Between Hippocampus and Insula in Adolescent Major Depressive Disorder using DTI," *Proc. 2018 Asilomar Conference on Signals, Systems and Computers*, pp. 1182-1186, Pacific Grove, CA, Oct. 28-Oct. 31, 2018

402. S. Chu, C. Lenglet, M.W. Schreiner, B. Klimes-Dougan, K.R. Cullen, and K.K. Parhi, "Classifying Adolescent Major Depressive Disorder using Linear SVM with Anatomical Features from Diffusion Weighted Imaging," *Proc. 2018 Asilomar Conference on Signals, Systems and Computers*, pp. 1197-1201, Pacific Grove, CA, Oct. 28-Oct. 31, 2018

403. B. Sen and K.K. Parhi, "Constrained Tensor Decomposition Optimization with Applications to fMRI Data Analysis," *Proc. 2018 Asilomar Conference on Signals, Systems and Computers*, pp. 1923-1928, Pacific Grove, CA, Oct. 28-Oct. 31, 2018

404. S.V.S. Avvaru and K.K. Parhi, "Feed-Forward XOR PUFs: Reliability and Attack-Resistance Analysis," *Proc. 2019 ACM Great Lakes Symposium on VLSI*, Washington, D.C., May 2019

405. N.K. Unnikrishnan, M. Garrido, and K.K. Parhi, "Effect of Finite Word-Length on SQNR, Area and Power for Real-Valued Serial FFT," *Proc. 2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, May 2019

406. X. Liu and K.K. Parhi, "Computing Radial Basis Function Support Vector Machine using DNA via Fractional Coding," *Proc. 2019 ACM/IEEE Design Automation Conference*, Las Vegas, June 2019

407. A. Ayling, S.V.S. Avvaru, and K.K. Parhi, "Not All Feed-Forward MUX PUFs Generate Unique Signatures," *Proc. 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Miami, July 2019

408. S.V.S. Avvaru and K.K. Parhi, "Effect of Loop Positions on Reliability and Attack Resistance of Feed-Forward PUFs," *Proc. 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Miami, July 2019

409. B. Sen and K.K. Parhi, "Predicting Male vs. Female from Task-fMRI Brain Connectivity," *Proc. of 2019 IEEE Engineering and Medicine in Biology Conference (EMBC)*, Berlin, July 2019

410. B. Sen, B. Mueller, B. Klimes-Dougan, K. Cullen and K.K. Parhi, "Classification of Major Depressive Disorder from Resting-State fMRI," *Proc. of 2019 IEEE Engineering and Medicine in Biology Conference (EMBC)*, Berlin, July 2019

Conference Abstracts Without Proceedings

1. A. Shea, B. Fett, M. Riedel, and K.K. Parhi, "Synthesizing Sequential Register-Based Computation with Biochemistry," *Proc. of IEEE/ACM International Workshop on Logic Synthesis*, 2009

2. H. Jiang, M. Riedel, and K. Parhi, "Signal Processing Functions with Biomolecular Reactions," *International Workshop on Bio-Design Automation*, Anaheim, CA, 2010

3. H. Jiang, M. Riedel, and K. Parhi, "Iterative Computation with Biomolecular Reactions," *Annual Institute of Biological Engineering Conference*, Boston, MA, 2010

4. H. Jiang, M. Riedel, and K. Parhi, "Digital Signal processing with DNA," *International Conference on DNA Computing*, Pasadena, CA, 2011

5. H. Jiang, M. Riedel, and K. Parhi, "Asynchronous Sequential Computation with Molecular Reactions," *International Workshop on Bio-Design Automation*, San Diego, CA, 2011

6. S. Roychowdhury, K.K. Parhi, M.G. Lawrence, and D.D. Koozekanani, "Automated Screening System for Detecting Diabetic Retinopathy: A Classification Approach," Poster presented at 2012 *Association for Research in Vision and Opthalmology (ARVO) annual meeting*, Fort Lauderdale, May 2012

7. S. Radwan, S. Roychowdhury, J. Tokarev, H.F. Roemhild, K.K. Parhi, and D.D. Koozekanani, "Optical Coherence Tomography Predictors of Visual Outcome in Macular Edema," Poster presented at 2013 *Association for Research in Vision and Opthalmology (ARVO) Annual Meeting*, Seattle, May 2013

8. S. Roychowdhury, D.D. Koozekanani, S. Radwan, and K.K. Parhi, "Automated Detection and Location Analysis of Diabetic Cysts in Retinal OCT Images: An Iterative Filtering Approach," Poster presented at 2013 *Association for Research in Vision and Opthalmology (ARVO) Annual Meeting*, Fort Lauderdale, May 2013

9. K.K. Parhi and Z. Zhang, "Seizure Prediction using Ratio of Spectral Power from Single EEG Electrode," *Proc. of 6th International Workshop on Seizure Prediction (IWSP6)*, p. 39, Nov. 2013, San Diego

10. S. Roychowdhury, K.K. Parhi, M. Reinsbach, and D.D. Koozekanani, "Automated Intra-Retinal Layer Thickness Profile Analysis in Optical Coherence Tomography Images by Iterative High-Pass Filtering," Poster presented at 2014 *Association for Research in Vision and Opthalmology (ARVO) Annual Meeting*, Orlando, FL, May 2014

11. Y. Wang, B. Yuan, K.K. Parhi and R. Victora, "Two-Dimensional Magnetic Recording using a Rotated Head Array and LDPC Code Decoding," *2014 IEEE International Magnetics Conference (INTERMAG) Digest*, Dresden, Germany, May 2014

12. S. Chu, C. Lenglet and K.K. Parhi, "Joint Brain Connectivity Estimation from Diffusion and Functional MRI Using a Network Flow Model," Poster presented at 2014 *IEEE EMBS BRAIN Grand Challenges Conference*, Nov. 2014, Washington, D.C.

13. K.K. Parhi, "Simple Features and Simple Classifiers for Cyber-Physical Systems: Applications to Seizure Detection and Prediction," Talk presented at *Workshop on Big Data Analytics in CPS: Enabling the Move from IoT to Real-Time Control*, April 2015, Seattle, Washington

14. S. Chu, K.K. Parhi and C. Lenglet, "Joint Brain Connectivity Estimation from Diffusion and Functional MRI Using a Network Flow Model," Poster presented at the *24th Annual Meeting of the International Society for Magnetic Resonance in Medicine (ISMRM)*, May 30-June 5, 2015, Toronto, Canada

15. Z. Zhang and K.K. Parhi, "Seizure Prediction using Polynomial Support Vector Machine Classification," Poster presented at the 7th *International Workshop on Seizure Prediction*, August 3-6, 2015, Melbourne, Australia

16. S.A. Salehi, K.K. Parhi and M.D. Riedel, "Markov Chain Computations using Molecular Reactions," Poster Presented at the 21st *International Conference on DNA Computing and Molecular Programming (DNA21)*, August 17-21, 2015, Cambridge, MA

17. Y. Wang, B. Yuan, K.K. Parhi, and B. Kumar, "Increased Data Throughput and BER Performance with Rotated Head Array in the Two Dimensional Magnetic Recording," *2016 joint MMM-IEEE International Magnetics Conference (INTERMAG)*, San Diego, Jan. 2016

18. K.K. Parhi, "Network Analysis of Functional Brain Connectivity in Borderline Personality Disorder Using Resting-State fMRI," *2016 Information Theory and Applications (ITA)*, San Diego, Jan. 2016 *(Invited Talk)*

19. A. Rashno, K.K. Parhi, B. Nazari, S. Sadri, H. Rabbani, P. Drayna, and D.D. Koozekanani, "Automated Intra-Retinal, Sub-Retinal and Sub-RPE Cyst Regions Segmentation in Age-Related Macular Degenration (AMD) Subjects," *Annual Meeting of the Association for Research in Vision and Ophthalmology (ARVO)*, Baltimore, MD, May 2017

20. J. Kohler, A. Rashno, K.K. Parhi, P. Drayna, S. Radwan, and D.D. Koozekanani, "Correlation Between Initial Vision and Vision Improvement with Automatically Calculated Retinal Cyst Volume in Treated DME after Resolution," *Annual Meeting of the Association for Research in Vision and Ophthalmology (ARVO)*, Baltimore, MD, May 2017

21. K.K. Parhi, A. Rashno, B. Nazari, S. Sadri, H. Rabbani, P. Drayna, and D.D. Koozekanani, "Automated Fluid/Cyst Segmentation: A Quantitative Assessment of Diabetic Macular Edema," *Annual Meeting of the Association for Research in Vision and Ophthalmology (ARVO)*, Baltimore, MD, May 2017

22. S. Chu, B. Klimes-Dougan, K.K. Parhi, M.W. Schreiner, K. Cullen, "Brain Connectivity Correlates with Antidepressant Treatment Response in Adolescents with Major Depressive Disorder," *Society for Research on Adolescence (SRA) Biennial Meeting*, Minneapolis, April 2018

University Sponsored Research Grants

1. "Dedicated VLSI DSPs", *Graduate School Grant-in-Aid*, $33.6k (Sept. 1988 - June 1990)

2. "Equipment for VLSI and Image Processing Laboratory", *Graduate School Grant-in-Aid*, $22.5k (Sept. 1990 - June 1991)

3. "McKnight Land Grant Professorship", *Graduate School*, $39.2k, (July 1992 - June 1994)

4. "Edgar F. Johnson Professorship", *College of Science and Engineering*, $15K per year (July 1997 - present)

5. "Distinguished McKnight University Professorship", *Univ. of Minnesota*, $100k research support, Permanent University title, July 2000

6. "Seizure Prediction Classifier Algorithms and Architectures", IEM, $50K (Jan. 1, 2010 - Jan. 31, 2011) (Co-PI: T. Netoff)

7. "Automated Screening System for Diabetic Retinopathy using Fundus Images", Grant-in-Aid, Graduate School, $31,153, Jan. 1, 2011 - June 30, 2012

8. K.K. Parhi, "Redesigning Signal Processing Education, OIT Faculty Fellowship," $10k (2012-2013)

9. K.K. Parhi, "Graduate/Professional Teaching Award," $15k (2013)

10. K.K. Parhi, D. Koozekanani, "Automated Screening for Hypertensive Retinopathy and Stroke from Fundus Images," IEM, $25k, Jan. 2014-Jan. 2015

Externally Funded Research Grants

1. "VLSI Architecture Designs for High-Speed Signal and Image Processing", **National Science Foundation**, Research Initiation Award, $70k (June 1989 - Jan. 1992)

2. "CAD of Real-Time DSP ICs", **Texas Instruments**, $42k, (July 1989 - June 1992)

3. "Vector Quantizers using Neural Networks", **US West Advanced Technologies**, $8k (Aug. 1989)

4. "Concurrent Architectures for VLSI Signal and Image Processing", **Army Research Office**, $233.6k (March 1990 - Feb. 1993)

5. "Design of Dedicated and Programmable VLSI DSP Systems", **Office of Naval Research**, $425k, (Oct. 1990 - Sept. 1993)

6. "CISE Research Instrumentation", **National Science Foundation**, $76k, (Jan. 1992 - Dec. 1992) (with R. Harjani and G. Sobelman)

7. "NYI: Dedicated VLSI Digital Signal and Image Processors", **National Science Foundation**, NSF Young Investigator Award, $312.5k, (Sept. 1992 - March 1998)

8. "Video Compression using Neural Networks", **Data Card Corporation**, $10k, (Sept. 1992 - June 1993)

9. "Design of Dedicated and Programmable VLSI DSP Systems", **Office of Naval Research**, $403k, (Oct. 1993 - Sept. 1996)

10. "Design of High-Speed Digital Signal Processing Architectures", **Office of Naval Research**, $85k (Sept. 1993 - Aug. 1996)

11. "VLSI System Design Methodologies", **NEC Corporation**, $58k, (May 1993 - June 1999)

12. "Design of High-Speed and Low-Power DSP Architectures", **Army Research Office**, $96k (Sept. 1993 - Aug. 1996)

13. "Design Tools and Architectures for Dedicated DSP Processors", **DARPA/Air Force - RASSP Program**, $600k (Aug. 1993 - Aug. 1996)

14. "Concurrent Architectures for VLSI Signal and Image Processing", **Army Research Office**, $169.5k, (Oct. 1994 - Sept. 1997)

15. "Low-Energy Embedded DSP Systems", **Lucent Technologies, Bell Labs.**, $25k (Oct. 1995 - Sept. 1996)

16. "NSF-CGP Fellowship: VLSI Digital Signal Processing and Multimedia Systems", **National Science Foundation**, $104.8k, (Sept. 1996 - July 1997)

17. "Design of Low-Power Arithmetic Systems", **Office of Naval Research**, $102.7k (Sept. 1996 - Sept. 1999)

18. "Application-Specific DSP System design", **Kawasaki Steel - LSI Division**, $60k, (Aug. 1997 - Aug. 1999)

19. "Programmable and Configurable Digit-Serial Digital Signal Processors", **DARPA/ITO Emedded Systems Program/ACS Program**, $1,454k, (Aug. 1996 - Aug. 2000)

20. "Low-Power Architectures for Video Compression", **Army Research Office**, $108.4k (March 1998 - March 2001)

21. "VLSI Architectures for Wavelets and Finite Field Arithmetic", **Army Research Office**, $305k, (June 1998 - June 2001)

22. "Low-Energy Datapath Design for Programmable Digital Signal Processors", **National Science Foundation**, $321k, (Nov. 2000 - Oct. 2003)

23. "High-Speed and Low-Power Error Control Coders", **Army Research Office**, $366k, (August 2001 - August 2004)

24. "Student Travel Grants for SIPS-2002 Workshop", **National Science Foundation**, $5k, (July 2002 - June 2003)

25. "SIPS-2002 Workshop", **Broadcom Corporation**, $5k, (July 2002 - June 2003)

26. "Student Travel Grants for SIPS-2002 Workshop", **Army Research Office**, $5.4k, (July 2002 - June 2003)

27. "Architecture Design Methodologies for Embedded Systems Terminals", **National Science Foundation**, $150k, (June 2003 - Sept. 2004)

28. "LDPC Decoders", **Chonbuk National University, Korea**, $25k (Jan - Dec. 2004)

29. "Architectures for soft-Decision Reed-Solomon Coders", **Army Research Office**, $250k, (July 2004-June 2007)

30. "Design of High-Speed Transceivers for Ethernet over Copper", **National Science Foundation**, $250k, (August 2004-August 2007)

31. "SBIR Phase I: Design of a 10-Gigabit Ethernet Transceiver Over Copper," **National Science Foundation**, $100k, Grant to Leanics Corporation, (Jan. 2005 - Dec. 2005) (PI: Y. Gu)

32. "Phase-I: Tactical Secure Voice/Variable Data Rate Inter Working Function," **U.S. Navy**, $100k, SBIR Contract to Leanics Corporation (2006-2007) (PI: A. Cohen)

33. "Phase-II: Tactical Secure Voice/Variable Data Rate Inter Working Function," **U.S. Navy**, $750k, SBIR Contract to Leanics Corporation, (2008-2010) (PI: A. Cohen)

34. "Collaborative Research: CPA-DA: Noise-Aware VLSI Signal Processing: A New Paradigm for Signal Processing Integrated Circuit Design in Nanoscale Era", **National Science Foundation**, $150k, (Sept 2008-August 2011)

35. "EAGER: Synthesizing Signal Processing Functions with Biochemical Reactions", **National Science Foundation**, $200k (Sept. 2009-Aug. 2011) (Co-PI: M. Riedel)

36. "SBIR Phase I: High-Rate Low-Power Wireless Telemetry System for Medical Applications," **National Science Foundation**, $100k, Grant to Leanics Corporation, (Jan. 2010 - Dec 2010) (PI: J. Lin)

37. "Phase-I: LeanTec: Field Programmable Gate Array (FPGA) Physical Unclonable Functions," $100k, **U.S. Army**, Contract to Leanics Corporation (Jan. 2011 - Dec. 2011) (PI: A. Cohen)

38. "SHF:Small:Digital Signal Processing with Biomolecular Reactions", **National Science Foundation**, $400k (July 2011-June 2014) (Co-PI: M. Riedel)

39. K. Parhi is a Co-I on the $3M NSF IGERT training grant (PI: Bin He) (2011-2016)

40. Broadcom Foundation Gift, $25k (2012-2013)

41. "Stochastic Computing using Digital Signal Processing," **National Science Foundation**, $375k (Sept. 2013-Aug. 2016)

42. Broadcom Foundation Gift, $25k (2013-2014)

43. Broadcom Foundation Gift, $25k (2014-2015)

44. "SHF:Small:Advanced Digital Signal Processing with DNA", **National Science Foundation**, $400k (August 2014-July 2017) (Co-PI: M. Riedel)

45. "Design of Secure and Anti-Counterfeit Integrated Circuits", **Semiconductor Research Corporation**, $168k (Oct. 2014-Sept. 2017) (Joint with NSF) (Co-PI: C. Kim)

46. "Design of Secure and Anti-Counterfeit Integrated Circuits", **National Science Foundation**, $332k (Oct. 2014-Sept. 2018) (Co-PI: C. Kim)

47. "EAGER: Low-Energy Architectures for Machine Learning," National Science Foundation, $125k (Aug. 2017-Aug. 2018)

48. ""SHF: Small: Collaborative Research: LDPD-Net: A Framework for Accelerated Architectures for Low-Density Permuted-Diagonal Deep Neural Networks," National Science Foundation, $275k,(Oct. 2018-Sept. 2021)

Technical Society Activities: Organizational

1. Member, Board of Governors, IEEE Circuits and Systems Society (2005, 2006, 2007)
2. Member, IEEE CAS Society (CASS) Fellow Selection Committee (2003, 2004, 2008, 2015, 2017)
3. Member, IEEE CASS Charles A. Desoer Technical Achievement Award Committee (2018)
4. Chair, IEEE CASS Charles A. Desoer Technical Achievement Award Committee (2019)
5. Chair, VLSI Systems and Applications Technical Committee, IEEE Circuits and Systems Society (2002-2004)
6. Member, IEEE CASS Outstanding Young Author Award Committee (2003)
7. Member, IEEE Darlington and Guillemin-Cauer Prize Paper Committee (2004, 2005)
8. Member, IEEE CASS Charles A. Desoer Technical Achievement Award Selection Committee (2018, 2019)
9. Chair, ASEE Frederick Emmons Terman Award Selection Committee (2005)
10. Judge, IEEE Fellow Committee, 1998, 1999
11. Judge, ASP-DAC Best Paper Selection Committee (1998)
12. Member, IEEE VLSI Trans. EIC Selection Committee (2002)
13. Editor-in-Chief, IEEE Trans. on Circuits and Systems, Part-I: Regular Papers, Jan. 2004-Dec. 2005
14. NSF Panel, 1993, Feb. 2002, Apr. 2003, Dec. 2004, March 2010, Oct. 2011, May 2012, May 2014, June 2014, May 2015, 2017
15. (Biomedial Imaging/Engineering) NIH R43/44 Panel, March 2011, March 2012
16. Judge, Davidson Fellowship Selection, 2011, 2012
17. Associate Editor, IEEE Trans. on Circuits and Systems (1990-1991)
18. Associate Editor, IEEE Transactions on Signal Processing (1993-1995)
19. Associate Editor, IEEE Circuits and Systems Trans., Part II: Analog and Digital Signal Processing, 1995-1997
20. Associate Editor, IEEE Trans. on VLSI Systems, 1997-9
21. Associate Editor, IEEE Signal Processing Letters, 1997-1999
22. Editor, Journal of VLSI Signal Processing, 1993-

23. Guest Editor, Special Issue on 1995 IEEE VLSI Signal Processing Wksp. for the Journal of VLSI Signal Processing, Vol. 16(1), May 1997

24. Guest Coeditor, Special Issue on "Theory and Application of Filter Banks and Wavelets", IEEE Trans. on Signal Processing, April 1998

25. Guest Editor, Special Issue on ASAP Conf. 1996 for the Journal of VLSI Signal Processing, Vol. 19(2), June 1998

26. Guest Co-Editor, Special Issue on Interconnect for the Journal of Analog Circuits and Signal Processing, Vol. 31, No. 3, June 2002

27. Guest Co-Editor, Special Issue on SIPS-2002 for the Journal of VLSI Signal Processing

28. Guest Co-Editor, Special Issue on Signal Processing for Broadband Access Systems: Techniques and Implementations for the EURASIP Journal on Applied Signal Processing (Dec. 2003)

29. Associate Editor, IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing, 2002-2003

30. Member, Editorial Board, IEEE Signal Processing Magazine (2003-2006)

31. General Chair, IEEE Signal Processing Systems (SiPS): Design and Implementation Workshop, Oct. 2002

32. International Coordination Chair of IEEE APCCAS 2004, Tainan, Taipei

33. Technical Program Cochair, IEEE VLSI Signal Processing Workshop, Oct. 1995

34. Technical Program Cochair, Applications Specific Array Processors, Sept. 1996

35. Track Chair, Parallel Processing Track, IEEE ISCAS - 1993

36. Track Chair, DSP Processing Track, IEEE ISCAS - 1995

37. Track Chair, VLSI Track, IEEE ISCAS - 2002, 2003

38. Track Chair, VLSI Track, Midwest Symp. on VLSI, 2004

39. Technical Program Committee, IEEE HOST, 2016, 2017

40. Technical Program Committee: IEEE VLSI SP Workshop, 1990 - 96

41. Technical Program Committee: IEEE SiPS Workshop, 1997 - 2004, 2010, 2012

42. Technical Program Committee: IEEE ICASSP 1991 - 2004

43. Technical Program Committee, European Signal Processing Conference (EUSIPCO), 2008

44. Technical Program Committee: IEEE ISCAS 1992 - 93, 1995 - 2002, 2010, 2012 [Track-Chair: 1993 (Parallel Processing), 1995 (DSP), 2002, 2003 (VLSI)]

45. Technical Program Committee, Int. Workshop on System-on-Chip (2003, 2004, 2005)

46. Technical Program Committee, Int. Symp. on System-on-Chip (2003, 2004)

47. Technical Program Committee: IEEE Symp. on Computer Arithmetic, 1997, 2016

48. Technical Program Committee: IEEE ASP-DAC Conference, 1998, 2000

49. Technical Program Committee: ASAP Conf., 1992 - 96, 2002, 2004

50. Technical Program Committee: Great Lakes Symp. on VLSI, 1996, 1999, 2000, 2001, 2003, 2004, 2005, 2006

51. Technical Program Committee: Int. Conf. Electronics, Circuits and Systems (IECS), Rhodes (Greece), 1996

52. Technical Program Committee: Int. Workshop on Image and Signal Processing, Advances in Computational Intelligence, 1996

53. Technical Program Committee: IEEE Wksp. on VLSI for Communications, 1993

54. Technical Program Committee: Workshop on CORDIC-related Paradigm to Signal Processing Problems, 1998

55. Technical Program Committee: INDICON-2004 (Kharagpur, India)

56. Registration Chair, 1993 IEEE ICASSP Conference (Minneapolis)

57. Advisory Board, 2014 International Conference on VLSI and Signal Processing, Jan. 2014, IIT Kharagpur, India

58. Advisory Board, 1st International Conference on Automation, Control, Energy and Systems, Feb. 2014, Hooghly, India

59. Session Chair, IEEE EMBC Conference, 2012, 2015, 2018

60. Session Chair, Asilomar Conference - 1998, 2001, 2012, 2015

61. Session Chair, IEEE ICASSP 91, 96, 99, 00, 2015

62. Session Chair, IEEE ISCAS 1992, ISCAS 1993, 1995, 1996, 1997, 1998, 2001, 2002, 2017

63. Session Chair, IEEE VLSI Signal Processing Workshop, 1992, 1993, 1995, 1996

64. Session Chair, IEEE SiPS Workshop, 1997, 2001

65. Session Chair, IEEE Workshop on VLSI in Communications, 1993

66. Session Chair, 3rd Int. Conf. on Image and Signal Processing, 1995

67. Session Chair, ASAP Conf., Aug. 1994, 1996

68. Session Chair, IEEE ASP-DAC Conf., Jan. 2000

Tutorials, Short Courses, Panels, Invited Keynote Talks

1. Co-Presenter, Tutorial Workshop on "VLSI DSP Synthesis" at IEEE ICASSP 92 (also available as an *IEEE Video Tutorial*)
2. Presenter, Tutorial on DSP Architectures and Synthesis at VLSI'95
3. Organizer and Copresenter, Tutorial on DSP Architectures and Synthesis at IEEE ISCAS 95
4. Organizer and Copresenter, Tutorial on Design of High-Performance DSP Systems at IEEE ISCAS 96
5. Organizer and Copresenter, Tutorial on High-Performance Video DSP Systems at IEEE ISCAS 97
6. Organizer and Copresenter, Tutorial on Low-Power Multimedia DSP Systems at IEEE ICASSP98
7. Presenter, Tutorial on VLSI Architectures for Video and Data Communications at IEEE ISCAS98
8. Copresenter, Tutorial on Design Methodologies for Low Power Signal Processing, IEEE Int. Symp. on Low Power Electronics and Design, Monterey, Aug. 1998
9. Organizer and presenter, Tutorial on Design of Low-Power Multimedia DSP Systems at IEEE ISCAS 1999
10. Panelist, Future of Digital Signal Processing, ISCAS'96
11. Plenary Talk Speaker, ICVC-97
12. Invited Speaker, IEEE CAS/COM Workshop on ADSL, Princeton, July 1999
13. Panelist, "Single Chip or Multiple Chips", IEEE CAS/COM Workshop on ADSL, Princeton, July 1999
14. Keynote Talk Speaker, 2001 IEEE SiPS Workshop (Antwerp, Belgium)
15. Invited Speaker, 2001 System-on-Chip Conference (Tampere, Finland)
16. Panlist, 2001 System-on-Chip Conference (Tampere, Finland)
17. Invited Speaker, 2003 IEEE SiPS Workshop, Seoul, Korea (August 2003)
18. Tutorial Copresenter, IEEE Portable 2007 Conf.

19. Tutorial Copresenter, IEEE ISCAS 2007 Conf.

20. Keynote Talk, ACM Great Lakes Symposium on VLSI, 2014

21. Short Course on VLSI Signal Processing, Indian Institute of Technology, Kharagpur, Dec. 2016

22. Short Course on VLSI Communications Systems and Ethernet Transceivers, Indian Institute of Technology, Kharagpur

23. Tutorial Presentation on Hardware Security, IEEE ISCAS, 2017

24. Keynote Speaker, Workshop on Processing for Communication and Intelligent Information (PCII), Fudan University, Shanghai, June 2017

25. Short Course on VLSI Signal Processing, Fudan University, China, June 2017

26. Short Course on Hardware Security: Authentication and Obfuscation, Guru Jambheshwar University of Science and Technology, Hisar, August 2017

27. Tutorial on Data-Driven Healthcare: Applications from Neurology, Psychiatry and Ophthalmology, IEEE ISCAS, 2018

Technical Society Activities: Reviews

1. Ph.D. Thesis Committee, Univ. of Grenoble, France, Feb. 1995
2. Ph.D. Thesis Committee, I.I.T. Bombay, India, Feb. 1998
3. , Ph.D. Thesis Committee, KJIST Univ., Korea (2003)
4. Ph.D. Thesis Committee, Linkoping Univ., Sweden (2003)
5. Ph.D. Thesis Committee, Univ. of Toronto (2003)
6. Ph.D. Thesis Opponent, Linkoping University, Sweden (2004)
7. Ph.D. Thesis Opponent, Lund University, Sweden (2012)
8. Ph.D. Thesis Examiner, Univ. Canterbury, New Zeland, 2015, 2016, 2019
9. Ph.D. Thesis Examiner and Committee, Univ. Calgary, Canada, 2015
10. Ph.D. Thesis Examiner and Committee, Indian Institute of Technology, Bhubaneswar, 2017
11. Ph.D. Thesis Examiner, National Institute of Technology, Meghalaya, 2018
12. Book Reviewer, Kluwer Academic Press, 1990-, McGraw Hill, 1992-, IEEE Press, 1993-, IEEE Comp. Society Press (1994-), CRC Press (2017)
13. Reviewer Swiss National Science Foundation (2013)(2015)(2017)
14. Italian Research Assessment Exercise VQR 2004-2010 (2013) (2015)
15. Reviewer, NSF Proposals (1989-), ARO Proposals (1992-), UK EPSRC
16. Reviewer, Nature Biomedical Engineering, 2017
17. Reviewer, Nature Pediatrics, 2015
18. Human Brain Mapping, 2018
19. Reviewer, NeuroImage, 2016-
20. Reviewer, IEEE Trans. NanoBio Science, 2017-
21. Reviewer, Clinical EEG and Neuroscience, Sage, 2014-
22. Reviewer, EURASIP Journal on Advances in Signal Processing, 2014-
23. Reviewer, Royal Society Interface, 2015
24. Reviewer, IEEE Proceedings, 1986-
25. Reviewer, IEEE Transactions on Circuits and Systems, 1986-

26. Reviewer, IEEE Transactions on Circuits and Systems, Part II, 1993-
27. Reviewer, IEEE Transactions on Circuits and Systems, Part I, 1996-
28. Reviewer, IEEE Trans. Neural Systems and Rehabilitation Engineering, 2018-
29. Reviewer, IEEE Transactions on Computers, 1987-
30. Reviewer, IEEE Journal of Solid State Circuits, 1990-
31. Reviewer, IEEE Trans. on Acoustics, Speech, and Signal Processing, 1989-
32. Reviewer, IEEE Trans. on Parallel and Distributed Systems, 1991-
33. Reviewer, IEEE Trans. on Circuits and Systems for Video Technology, 1991-
34. Reviewer, IEEE Trans. on VLSI Systems, 1993-
35. Reviewer, IEEE Trans. on Image Processing, 1994-
36. Reviewer, IEEE Trans. on Speech and Audio Processing, 1997-
37. Reviewer, IEEE Trans. on Vehicular Technology, 1996-
38. Reviewer, IEEE Signal Processing Letters, 1995-
39. Reviewer, IEEE Signal Processing Magazine, 1997-
40. Reviewer, IEEE Trans. on Communications, 1996-
41. Reviewer, IEEE Journal of Selected Areas in Communications, 1999-
42. Reviewer, IEEE Trans. on Computer Aided Design, 1999-
43. Reviewer, IEEE Trans. Medical Imaging, 2013-
44. Reviewer, IEEE Trans. Biomedical Engineering, 2014-
45. Reviewer, PLOS One, 2015-
46. Reviewer: IEICE
47. Reviewer, Elsevier Signal Processing, 2012
48. Reviewer, ACM TODAES, 1996-
49. Reviewer, Journal of Parallel and Distributed Computing, 1988-
50. Reviewer, Journal of VLSI Signal Processing (Kluwer Academic), 1988-
51. Reviewer, Journal of System Integration (Kluwer Academic), 1991-
52. Reviewer, Multidimensional Systems and Signal Processing (Kluwer), 1994-

53. Reviewer, The Computer Journal, 1993-
54. Reviewer, Applied Mathematics Letters, 2002-
55. Reviewer, Int. Journal of Circuits, Systems and Computers, 1997
56. Reviewer, IEE Proceedings, Circuits, Devices and Systems, 1994-
57. Reviewer, IEEE International Symposium on Circuits and Systems, 1986-
58. Reviewer, Int. J. of Computers and Mathematics, 2001-
59. Reviewer, IEEE Int. Conf. on Acoustics, Speech, and Signal Processing, 1990-
60. Reviewer, IEEE Int. Symposium on Computer Architecture, 1990-
61. Reviewer, IEEE Workshop on VLSI Signal Processing, 1990-
62. Reviewer, IEEE International Parallel Processing Symposium, 1991-
63. Reviewer, IEEE Asia Pacific Conference on Circuits and Systems, 1992 -
64. Reviewer, ACM/IEEE Design Automation Conference, 1991-
65. Reviewer, IEEE Int. Conf. on Image Processing, 1995-
66. Reviewer, International Conference on Parallel Processing, 1988-
67. Reviewer, Int. Conference on Applications Specific Array Processors, 1990-
68. Reviewer, Hawaii International Conference on System Sciences, 1991
69. Reviewer, European Conf. on Circuit Theory and Design, 1993-
70. Reviewer, Midwest Symp. on Circuits and Systems, 1995-
71. Reviewer, Int. Conf. on VLSI Design, 1994-
72. Reviewer, European Signal Processing Conference (EUSIPCO), 1998
73. Reviewer, IEEE Globecom Conf., 2001, 2003
74. Reviewer, Percom 2004
75. Reviewer, VTC-2004
76. Reiewer, IEEE ECCTD 2009
77. Reviewer, IEEEE SiPS Workshop -2009, 2012, 2017

Technical Society Activities: Membership

1. Fellow of IEEE – Circuits and Systems Society (CASS)
2. Fellow , IEEE – Signal Processing Society (SPS)
3. Fellow, IEEE – Engineering and Medicine in Biology Society (EMBS)
4. Member, Technical Committee on VLSI Systems and Applications, IEEE CAS Society (Chair-Elect: 2000-2002, Chair: 2002-2004)
5. Member, Tech. Cmt. on Visual Signal Processing and Communications, IEEE CAS Society (retired)
6. Member, Tech. Cmt. on Digital Signal Processing, IEEE CAS Society (retired)
7. Founding Member, Tech. Cmt. on Nanoelectronics and Gigascale Integration, IEEE CAS society (retired)
8. Member, Technical Committee on Design and Implementation of SP Systems, IEEE Signal Processing Society (1990-1996, Advisory Member, 1996-)
9. Member, Technical Committee on VLSI, IEEE Computer Society

University Activities

1. Director of Graduate Stuides (2008-2011)
2. MN Future Proposal Review Panel (2013)
3. Graduate Teaching Award Selection Committee (2014, 2015, 2016)
4. Dosdall Fellowship Evaluation Committee (2012)
5. Member, Graduate Education Committee, Graduate School (2012)
6. Chair, Graduate Standards Committee (2007-2008)
7. Member, Graduate Standards and Program Committee, Electrical Eng. Dept. (1989-90) (1997-98) (2003-2004)
8. Member, Faculty Recruiting Committee of Electrical Eng. Dept. (1990-95) (1998-99)(2002-03)(2004-2005)(2005-2006) (2011-2012) (2012-2013)(2016-17) (2019)
9. Member, Faculty Promotion and Tenure Committee of Electrical Eng. Dept. (1995-96) (1998-99) (2013-14) (Chair, 2017-2018)
10. Member, Ph.D. Written Qual. Exam. Committee (1989, 1990, 1998, 2002-3, 2004-5, 2009-10, 2012-13) (2015) (2017-2018)

11. Member, Space Committee (2014-2016)
12. Instructor for Oral Presentation Training (1990)
13. Member, *Adhoc* Committee on Ph.D. Written Examination, 1993
14. Chair-Systems and Hardware Track for Univ. Digital Summit (1997)

Post Doctoral Fellows and Visitors Supervised

1. Kazuhito Ito, Currently Professor, University of Saitama, Japan (1992-1993)
2. Ching-Yi Wang, Currently with Boston Scientific (1993-1996)
3. Luis Montalvo, Currently with Technicolor, France (1995-1996)
4. Michael Zervakis, Currently Professor at Technical Univ. of Crete, Chania, Crete, Greece (1996)
5. Steve Summerfield, Formerly with Univ. of Warwick, Coventry, U.K., Currently with Huawei, London (1997)
6. Hiroshi Suzuki, Curretly Senior Manager at Broadcom Limited, Irvine, CA (1997-1999)
7. Javier Valls, Currently Professor at Universidad Politecnica de Valencia, Valencia, Spain (1999)
8. Trini Sansaloni, Currently Professor at Universidad Politecnica de Valencia, Valencia, Spain (1999)
9. Yuke Wang, Currently Patent Lawyer (Dallas, Texas) (1999)
10. Jin-Gyun Chung, Currently Dean of Engineering, Chonbuk National Univ., Korea (2001)
11. Chester Park, Currently Asst. Prof. at Konkuk University, Korea (2005)
12. Chunlei Xia (Shanghai, China, 2006)
13. Mario Garrido, Currently Asst. Professor at Linkping University, Sweden (2007)
14. Hemant Patil, Currently Assoc. prof. at DA-IICT, Gandhinagar, India (2009)
15. Xiaoping Li, Nanjing Univ, China (2010)
16. Sayed Ahmad Salehi, Currently Asst Prof. at Univ. of Kentucky (2011-12)
17. Yun-Nan Chang, Currently Professor at National Sun Yat-Sen Univ., Taiwan (2012)
18. Mojtaba Bandarabadi, Currently with Inselspital Bern, Switzerland (2012) (coadvised by Dr. Tay Netoff)
19. Abdolreza Rashno, Predoctoral Visitor from Isfahan University of Technology, Iran, 2016-2017

Ph.D. Theses Supervised

1. Lori E. Lucke, "Applying Parallel Processing Techniques to Digital Signal Processing Algorithms and Architectures for High Level VLSI Synthesis", December 1992

   [Currently Fellow, Minnetronix Corp, St. Paul]

2. Ching-Yi Wang, "MARS: A High-Level Synthesis Tool for Digital Signal Processing Architecture Design", December 1992

   [Currently with Boston Scientific, St. Paul]

3. Naresh R. Shanbhag, "Design of Pipelined VLSI Adaptive Digital Filters with Relaxed Look-Ahead", July 1993

   [Currently Jack kilby Professor at Univ. of Illinois at Urbana]

4. H.R. Srinivas, "Floating Point Computer Arithmetic Architectures", September 1994

   [Currently Senior Manager, Broadcom limited, Irvine, CA]

5. K.J. Raghunath, "Pipelined STAR RLS Adaptive Filters", October 1994

   [Currently Principal Architect, Ikanos Communications, NJ]

6. Jin-Gyun Chung, "Pipelined IIR Lattice and Wave Digital Filters", November 1994

   [Currently Professor at Chonbuk National University, Chonju, South Korea]

7. Tracy C. Denk, "Retiming, Folding and Register Minimization", July 1996

8. Janardhan H. Satyanarayama, "Design of Low-Power DSP Systems", March 1998

   [Currently with Intel, PA]

9. Ahmed Shalash, "Architecture and System Design for Digital Subscriber Loop Communications", June 1998

   [Currently Professor at Cairo University, Egypt]

10. Leilei Song, "Low-Power VLSI Architectures for Finite-Field Applications", June 1999

    [Currently at Intel, CA]

11. Yun-Nan Chang, "Low-Power Bit-Serial and Digit-Serial DSP Systems", June 1999

    [Currently Professor at National Sun Yat-Sen University, Kaohsiung, Taiwan]

12. Jun Ma, "Pipelined RLS Adaptive Filters", July 1999

13. Martin Kuhlmann, "High-Performance Low-Power Arithmetic, Architectures and Circuits", Dec. 1999

    [Currently Director at MaxLinear, Irvine, CA]

14. Vijay Sundararajan, "Performance Optimization Methodologies for Design of Digital VLSI Systems", Jan. 2000

    [Currently Associate Technical Director at Broadcom Inc., San Jose, CA]

15. Zhongfeng Wang, "High-Performance and Low-Cost VLSI Design of Turbo Decoders", Aug. 2000

    [Currently Full Professor at Nanjing University, China]

16. Robert A. Freking, "Structural Strategies for High-Performance Undelimited-Codeword Source Coding", October 2000

    [Currently with MIT Lincoln Laboratories]

17. William L. Freking, "Algorithms and Architectures for High-Performance Public-Key Cryptography Systems", October 2000

    [Currently with MIT Lincoln Laboratories]

18. Lijun Gao, "Architecture Design and Mapping of DSP Systems", Feb. 2001

    [Currently with Analog Devices, Boston]

19. Zhipei Chi, "High Performance, High Speed VLSI Architectures for Wireless Communication Applications", June 2001

    [Currently with Marvell Technology Group, San Jose, CA]

20. Tong Zhang, "Efficient VLSI Architectures for Error Correction Coding", June 2002

    [Currently Full Professor of ECSE Dept., R.P.I., Troy, NY]

21. Yanni Chen, "Low-Complexity High-Speed VLSI Architectures for Error-Correction Decoders", June 2003

    [Currently at Apple, CA]

22. Junjin Kong, "Classical and Quantum Convolutional Codes: Design and Implementation", Feb. 2005

    [Currently a "Master" at Samsung, S. Korea]

23. Xinmiao Zhang, "Architectures for Error Control Coders and Cryptography Systems", June 2005

    [Tenured Assoc. Prof. at The Ohio State Univ.]

24. Yongru Gu, "VLSI Architectures for High-Speed Transceivers", July 2005

    [Currently at Inplay Tech, Irvine]

25. Jun Tang, "Architectures for OFDM Based Ultra Wideband Systems", July 2006

    [Currently with Inplay Tech, Irvine, CA]

26. Sangmin Kim ,"Efficient VLSI Architectures for Error Control Coders", Oct. 2006

    [Currently with Qualcomm, San Diego]

27. Jianhung Lin, "Algorithm and Architectures for Next Generation Multimedia Systems", Jan. 2007

    [Currently with Maxlinear, Irvine]

28. Yuping Zhang, "VLSI Architectures for Turbo Code Decoder, LDPC Code Decoder and List Sphere Decoder", May 2007

    [Currently with Apple, CA]

29. Chao Cheng, "High-Speed Low-Cost VLSI DSP Algorithms Based on Novel Fast Convolutions and Look-Ahead Pipelining Structures", May 2007

    [Currently with Qualcomm, San Jose, CA]

30. Aaron E. Cohen, "Architectures for Cryptography Accelerators" September 2007

    [Currently with Naval Research Lab, Washington, DC]

31. Daesun Oh, "Low Complexity VLSI Architectures for LDPC Decoders", May 2008

    [Currently with Samsung, S. Korea]

32. Jie Chen, "Efficient VLSI Architectures for High-Speed Ethernet Transceivers", Aug. 2008

    [Currently Manager at Marvell Technology Group, San Jose, CA]

33. Renfei Liu, "Error Control Algorithms and Architectures for Reliable DSP Systems", Nov. 2010

    [Currently with Broadcom Corp., Irvine, CA]

34. Yun Sang Park, "Reduced-Complexity Epileptic Seizure Prediction with EEG," Jan. 2012 (Coadvised by Prof. Theoden I. Netoff)

    [Currently with Samsung, S. Korea]

35. Hua Jiang, "Digital Logic and Signal Processing Computations with Molecular Reactions," May 2012 (Coadvised by Prof. Marc D. Riedel)

    [Currently with Netflix, CA]

36. Manohar Ayinala, "Low-Power Architectures for Signal Processing and Classification Systems," July 2012

    [Currently with Intel, Austin, TX]

37. Chuan Zhang, "Low-Latency Low-Complexity Channel Decoder Architectures for Modern Communication Systems," December 2012

    [Currently Associate Prof. with Southeast University, China]

38. Te-Lung Kung, "Synchronization and Coding in Wireless Communication Systems," September 2013

39. Sohini Roychowdhury, "Automated Segmentation and Pathology Detection in Ophthalmic Images," July 2014

    [Currently with Volvo, Mountain View, CA]

40. Yingjie Lao, "Authentication and Obfuscation of Digital Signal Processing Integrated Circuits," July 2015

    [Currently Assistant Professor at Clemson University, South Carolina]

41. Bo Yuan, "Algorithm and Architecture for Polar Codes Decoder," July 2015

    [Currently Assistant Professor at Rutgers University, NJ]

42. Tingting Xu, "Biomarkers for Mental Disorders from Neuroimaging Data," December 2016

    [Currently with Ad Colony, Seattle]

43. Yin Liu, "Digital Signal Processing and Machine Learning System Design using Stochastic Logic," July 2017

    [Currently with Microsoft, Redmond, WA]

44. Sayed Ahmad Salehi, "A Framework for Computing Discrete-Time Systems and Functions using DNA," July 2017 (Coadvised by Prof. Marc D. Riedel)

    [Currently Assistant Professor at University of Kentucky]

45. Zisheng Zhang, "Approaches to Feature Identification and Feature Selection for Binary and Multi-Class Classification," July 2017

    [Currently with irhythm, San Francisco]

46. Sandhya Koteshwara, "Secure, Resilient and Low-Energy Hardware Architectures for Internet-of-Things," September 2018

    [Currently with IBM T.J. Watson Research Center, Yorktown Heights, NY]

47. Shu-Hsien Chu, "pproaches to Anatomical and Functional Brain Connectivity Analysis with Applications to Adolescent Major Depressive Disorder," September 2018 (Coadvised by Prof. Christophe Lenglet)

    [Currently with Intel, Oregon]

M.S. Projects Supervised

1. Gregory S. Munson, "Finite Precision Effects in Scattered and Clustered Look-Ahead Pipelined Recursive Digital Filter Implementations", June 1989

   [Currently with JAMF Software, Eau Claire, WI]

2. Jim Malaney, "Design of a Programmable Digital Filter", November 1989

   [Manager at GE Healthcare, Madison, Wisconsin]

3. Lai Q. Pham, "Roundoff Error in Digital Filters using Redundant Numbers", November 1989

4. Syed Babar Raza, "Reduction of Hardware Overhead in Recursive Filters by Interleaving", January 1991

5. Joo-Sang Lee, "A New Approach For Design Of Data Format Converter Architectures Using Register Allocation", May 1991

   [Currently with Micron Technology, Dallas, TX]

6. H.R. Srinivas, "High-Speed VLSI Arithmetic Processor Architectures Using Hybrid Number Representation", July 1991

   [Currently Senior Manager at Broadcom, Irvine, CA]

7. N. Iyer, "iSchematic: An Automatic Schematic Generator for OCT 5.0 Data Base", September 1991

8. Andrew P. Brown, "Applications of Circuit Retiming to DSP Architecture Design", October 1991

   [Currently with MBA Engineering, MN]

9. J.-G. Chung, "Synthesis of Pipelined Lattice IIR Digital Filter", November 1991

   [Currently Dean of Engineering, Chonbuk National Univ., S. Korea]

10. Gireesh Shrimali, "Fast Arithmetic Coder Architectures", June 1993

11. Wayne C. Amendola, Jr., "VLSI Implementation of a 200 MHz 16X16 Redundant Digit Multiplier and a 125 MHz 16X16 Booth-Encoded Redundant Digit Multiplier", June 1993

    [Currently Data Analyst, Capital One, CA]

12. Bin Fu, "VLSI Design Advances in Arithmetic Coding", May 1995

13. Santosh Misra, "CDMA Based Mobile Communication Systems", May 1995

    [Indian Administrative Service (IAS), Officer, Govt. of Chhattisgarh, India]

14. Darren Pearson, "Low Power Strategies for VLSI Implementation of Digital Filters", May 1995

    [Currently Instructor at St. Paul College, MN]

15. Surendra Jain, "Efficient VLSI Architectures for Finite Field Arithmetic", June 1995

    [Currently Venture Capitalist, Bengaluru, India]

16. Yun-Nan Chang, "High-Level DSP Synthesis using Heterogeneous Functional Units", June 1995

    [Currently Professor at National Sun Yat-Sen University, Taiwan]

17. Yuet Li, "STAR Adaptive Lattice Recursive Least Square Filters", February 1996

    [Currently Associate Technical Director at Broadcom, Fremont, CA]

18. Chong Xu, "Power-Speed Reconfigurable FIR Filters", February 1996

    [Currently with Intel, CA]

19. David A. Parker, "Low-Area/Power Parallel FIR Filters", May 1996

    [Currently Director at Altera, CA]

20. Mayukh Majumdar, "Low-Area Data Format Converters", June 1996

21. Leilei Song, "Efficient Bit-Serial Finite Field Multipliers", June 1996

    [Currently Senior Manager at Marvell]

22. John Bratt, "VHDL Interface for MARS DSP Synthesis System", June 1996

    [Currently with AMD, CO]

23. Hojun Kim, "Coefficient Optimization in Pipelined IIR Digital Filters", July 1996

    [Currently with Telematics, CA]

24. Mousumi Gayen, "ILP Scheduling with Processor Interconnection", Jan. 1997

25. Nikhil Sarpotdar, "Radix-2 Division and Square Root Algorithms: Study and Implementation", July 1997

26. William Ho, "Power Efficiency of the Carry-Select Adder", August 1997

    [Currently with a Startup, CA]

27. Ashish Karandikar, "Low-Power and High-Performance Static Random Access Memory", December 1997

    [Currently Vice President, Nvidia]

28. Zhipei Chi, "Pipelined Single and Multi-Channel Lattice RLS Adaptive Filters", Sept. 1998

    [Currently with Marvell, CA]

29. Nidish Kamath, "Scheduling of DSP Algorithms for Low-Power Design", Jan. 1999

    [Currently Technologist, Bay Area, CA]

30. Dhiraj Kumar, "Performance Tradeoffs of DCT Architectures in Xilinx FPGAs", April 1999

    [Currently Senior Director at Paypal, NY; Previously Sales Executive, Facebook]

31. Ziyu Li, "DLMS Adaptive FIR Filter: Bit-Serial Systolic Array VLSI Implementation", July 1999

    [Predictive Modeling Analyst at Travelers, MN]

32. Robin Bansal, "Optimized Power and Delay Solutions for Digital CMOS Circuits by Transistor Reordering using HEAT", August 1999

    [President and CEO, Bansi Holdings, PA]

33. Ru-Guang Chen, "Double Error Correction on Residue Number System", Feb. 2000

    [Currently with Amazon, CA]

34. Bibhudatta Sahoo, "A Low Power Correlator", Aug. 2000

    [Currently Associate Professor in Amrita University, Bengaluru, India]

35. Siwei Chen, "Minimal Switching Activity Schedules for Various FIR Filters", Aug. 2000

    [Currently with Focaltech, Providence, RI]

36. Wenhao Wu, "VLSI Design and Implementation of Two Viterbi Decoders", Aug. 2000

    [Currently with Intel, CA]

37. Karuna Prasad, "Power Analysis of 4-2 and 5-2 Compressors", Jan. 2001

38. Aaron E. Cohen, "VLSI Architectures for RSA," June 2004

    [Currently with Naval Research Lab, Washington, DC]

39. Saurabh Jain, "Low-Complexity Pipelined-Parallel Decision Feedback Decoder (PDFD) for 1 Gbps Ethernet", August 2004

    [Currently with Marvell, CA]

40. Lina Long, "A VLSI Implementation for Viterbi Decoder in Ultra Wide-band System", March 2005

    [Currently with Cisco, CA]

41. Manoj Yadav, "LDPC Decoder for DVB System", May 2005

    [Currently Manager at Marvell, CA]

42. Renfei Liu, "VLSI Architectures for Viterbi Decoders," May 2007

    [Currently at Broadcom, Irvine, CA]

43. Daesun Oh, "LDPC Decoder Architectures," Feb. 2008

    [Currently with Samsung, S. Korea]

44. Jie Chen, "Architectures for 10-Gigabit Ethernet," Feb. 2008

    [Currently Manager at Marvell, CA]

45. Priyadharshini Vijayakumar, "Timing Variations in Digital Filters with Supply Voltage Variations", Aug. 2008

    [Currently with Intel, CA]

46. Prashant Metkar, "Improved Approach for Calculating Model Parameters in Speaker Recognition using Gaussian Mixture Models", May 2009

    [Currently Financial Engineer in Pune, India]

47. Jaime Rivera, "Research for the Development of an Apparatus To Help Prevent Sudden Infant Death", May 2009

    [Currently with Eagle Properties, Rochester, MN]

48. Xiaoming Zhu, "Lung Sound Separation by Independent Component Analysis", June 2009

    [Currently at Marvell, CA]

49. Yun-Sang Park, "Seizure Prediction by Support Vector Machine Classification," Jan. 2010

    [Currently with Brown Univ as Postdoc]

50. Yingbo Hu, "Subthreshold Circuit Design", August 2010

    [Currently with Maxim, CA]

51. Manohar Ayinala, "High-Throughput VLSI Architectures for CRC/BCH Encoders and FFT Computations", Nov. 2010

    [Currently with Intel, Allentown, PA]

52. Lan Luo, "Postprocessing of Seizure Prediction by Kalman Filter", May 2011

    [Currently with Intel, Oregon]

53. Te-Lung Kung, "Frame Start Synchronization in OFDM System," September 2011

54. Michael Brown, "A Low-Complexity Seizure Prediction Algorithm," November 2011

    [Currently with Digi Wireless Devices, MN]

55. Chuan Zhang, "Polar Code Decoder Architectures," April 2012
    [Currently Associate Prof. at Southeast University, China]
56. Tingting Xu, "Schizophrenia Classification from MEG," May 2013
    [Currently PhD Candidate at UMN]
57. Manikandan Palani, "EEG Data Compression," May 2014
    [Currently with Qualcomm, Denver, CO]
58. Aravinth Chinnapalanichamy, "Serial and Interleaved FFT Architectures for Real Signals," Jan. 2015
    [Currently with Nvidia]
59. Sandhya Koteswara, "Obfuscated FFT Architecture," Feb 2015
    [Currently IBM T.J. Watson Research Center, Yorktown Heights]
60. Sayed Ahmad Salehi, "DNA Computing," April 2015
    [Currently University of Kentucky]
61. Yingjie Lao, "Removing Redundancies of Fast Fourier Transform Computations," July 2015
    [Currently with Clemson Univ., South Carolina")
62. Goutham N. C. Shanmugam, "Obfuscated Real FFT Architecture," August 2015
    [Currently with ARM, Austin, TX]
63. Vaishnavi Santhapuram, "Timing Induced Error Analysis for Wallace Tree Multipliers," Oct. 2015
    [Currently with Intel, CA]
64. Vishal Vijayakumar, "Artery/Vein Classification in Fundus Images," 2018
    [Currently Ph.D. student at the University of Minnesota]
65. Anoop Koyily, "A Study on Modeling of MUX-based Physical Unclonable Functions," April 2018
66. S.V. Sandeep Avvaru, "Attack-Resistance and Reliability Analysis of Feed-Forward and Feed-Forward XOR Arbiter PUFs," April 2019
    [Currently with Intel, San Diego]

Graduate Advisees

I am currently advising following Graduate Students.

1. Bhaskar Sen (PhD)
2. Satya Venkata Sandeep Avvaru (PhD)
3. Xingyi Liu (Ph.D.)
4. Nanda Kumar Unnikrishnan (Ph.D.)
5. Lulu Ge (Ph.D.)

New Course Development

1. I developed two new classes "VLSI Digital Signal Processing (EE 5329)" and "Digital Signal Processing Structures for VLSI" (EE-5549) in Spring 1989/Spring 1990.
2. I developed and taught the "VLSI Low-Power and Digital Video Systems (EE 8451)" Course in Fall 1997.
3. I developed and taught the "Digital Arithmetic, Error Control Coding and Cryptography Architectures" (EE 5953)" Course in Winter 1999
4. Developed and taught a new class "VLSI Communications Systems" in Spring-2003 (EE-8950)
5. Introduced and Taught "Teaching Experience in EE" class (EE-8920) (2010-11) (Spring 2012) (Spring 2014)
6. Introduced and Taught "Ethics and Professional Conduct in EE" (EE-8925) (Fall-2010) (Spring 2011) (Spring 2013) (Spring 2015)
7. I taught a new graduate course on Digital Signal Processing Applications (Spring 2015). Applications from neuroengineering and biomedical signal analysis were emphasized.

Non-Conference Invited Talks

1. "Pipelining and Parallel Processing of Recursive Digital Filters," University of California, Santa Barbara, May 1986

2. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Minnesota, Minneapolis, 1988

3. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," IBM T.J. Watson Research Center, Yorktown heights, NY, 1988

4. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," AT&T Bell Laboratories, Holmdel, NJ, 1988

5. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Texas Instruments, Dallas, 1988

6. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Motorola, Austin, Texas, 1988

7. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Bell Communications Research, NJ, 1988

8. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Southern California, Los Angeles, 1988

9. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Michigan, Ann Arbor, 1988

10. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Carnegie Mellon University, Pittsburgh, 1988

11. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Maryland, College Park, 1988

12. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Washington, Seattle, 1988

13. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Wisconsin, Madison, 1988

14. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Yale University, 1988

15. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Pennsylvania, Philadelphia, 1988

16. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," North Carolina State University, Raleigh, 1988

17. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Purdue University, West Lafayette, 1988

18. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," University of Texas-Austin, Austin, 1988

19. "Algorithm and Architecture Designs for High-Speed Digital Signal Processing," Cornell University, Ithaca, NY, 1988

20. "Multiprocessor Scheduling in Signal Processing Programs," U.S. West Advanced Technologies, Englewood, Colorado, August 1989

21. "Application of Unfolding in Signal Processing Applications," University of Colorado, Boulder, August 1989

22. "CAD of Real-Time DSP ICs," Texas Instruments, Dallas, Feb. 1990

23. "Approaches to High-Speed Digital Signal Processing," National University of Singapore, May 1991

24. "Critical Path Reduction by Unfolding and Folding Techniques," NEC Computer & Communication Lab., Japan, April 1992

25. "High-Speed Digital Signal Processors", NEC Computer & Communication Lab., Japan, May 1992

26. "Dedicated VLSI Digital and Signal Processors", Toshiba (Japan), May 1992

27. "Dedicated VLSI Digital and Signal Processors", Tokyo Inst. of Technology (Japan), May 1992

28. "Dedicated VLSI Digital and Signal Processors", NTT Transmission Laboratory (Japan), May 1992

29. "Dedicated VLSI Digital and Signal Processors", Tohuku University, Sendai (Japan), May 1992

30. "VLSI Wavelet Architectures", NEC Computer & Communication Lab., Japan, June 1992

31. "Dedicated VLSI Digital and Signal Processors", Indian Institute of Technology, New Delhi (India), July 1992

32. "Dedicated VLSI Digital and Signal Processors", Swiss Federal Institute of Technology, Zurich (Switzerland), August 1992

33. "Register Minimization in DSP Architectures", NCUBE Corporation, Bangalore, India, December 1993

34. "High-Speed Multiplication and Addition", IEEE Section, Bangalore, India, December 1993

35. "Pipelined VLSI IIR and Adaptive Digital Filters", Indian Institute of Science, Bangalore, India, December 1993

36. "High-Level Transformations for DSP Synthesis", Indian Institute of Science, Bangalore, India, December 1993

37. "Pipelined VLSI IIR and Adaptive Digital Filters", Department of Electrical Engineering Seminar, University of California, Davis, August 1994

38. "VLSI Architectures for Approximation Algorithms", Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, August 1994

39. "Dedicated VLSI Digital Signal Processors", Department of Electrical and Computer Engineering, University of Iowa, Iowa City, August 1994

40. Lectures on "VLSI Digital Signal Processing," Central Electronics Engineering Research Institute (CEERI), Pilani, India, Dec. 1994

41. Four Lectures on "VLSI Digital Signal Processing," Center for Development of Advanced Computing, Pune, Feb. 1995

42. "Low-Energy Embedded DSP Systems," AT&T Bell Laboratories, July 1995

43. "High-Performance VLSI Digital Signal Processing," Indian Telephone Industries, Bangalore, March 1996

44. Two Lectures on "VLSI Digital Signal Processing," Indian Institute of Technology, New Delhi, March 1996

45. "VLSI Digital Signal Processors", Univ. of Nottingham, U.K. (June 1995)

46. Lectures on "VLSI Digital Signal Processing", Delft Univ. of Technology, March and April 1996

47. "High-Performance VLSI Digital Signal Processing," National Tsing-Hua University, Hsinchu, Taiwan, October 17, 1996

48. "High-Performance VLSI Digital Signal Processing," National Chao-Tung University, Hsinchu, Taiwan, October 18, 1996

49. "High-Performance VLSI Digital Signal Processing," National Taiwan University, Taipei, Taiwan, October 21, 1996

50. "Design and Implementation of Dedicated and Programmable DSP Systems," Univ. of Ryukyus, Okinawa, Jan. 20, 1997

51. "Design and Implementation of Dedicated and Programmable DSP Systems," Kyushu University, Fukuoka, Jan. 21, 1997

52. "Design and Implementation of Dedicated and Programmable DSP Systems," LSI Division, Kawasaki Steel, Makuhari, Feb. 12, 1997

53. "Design and Implementation of Dedicated and Programmable DSP Systems," Technical Group Meeting of IEICE DSP, CAS and CS Groups, March 6, 1997, Hiroshima University

54. "Dedicated and Programmable VLSI Signal Processing Systems," Osaka University, Osaka, Japan, March 31, 1997

55. "Dedicated and Programmable VLSI Signal Processing Systems," Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, April 7, 1997 (IEEE CAS Distinguished Lecture)

56. "Dedicated and Programmable VLSI Signal Processing Systems," K-JIST, Kwanju, Korea, April 8, 1997 (IEEE CAS Distinguished Lecture)

57. "Dedicated and Programmable VLSI Signal Processing Systems," Chonbuk National University, Chonju, Korea, April 8, 1997 (IEEE CAS Distinguished Lecture)

58. "Dedicated and Programmable VLSI Signal Processing Systems," Seoul National University, Seoul, Korea, April 9, 1997 (IEEE CAS Distinguished Lecture)

59. "Dedicated and Programmable VLSI Signal Processing Systems," Daewoo Center, Seoul, Korea, April 9, 1997 (IEEE CAS Distinguished Lecture)

60. "Dedicated and Programmable VLSI Signal Processing Systems," Tohoku University, Sendai, Japan, April 18, 1997

61. "Dedicated and Programmable VLSI Signal Processing Systems," University of Southern California, Los Angeles, April 21, 1997 (Invited Talk)

62. "Dedicated and Programmable VLSI Signal Processing Systems," Inst. of Electronics, Academia Sinica, Beijing, China, June 2, 1997 (IEEE CAS Distinguished Lecture)

63. "Dedicated and Programmable VLSI Signal Processing Systems," Tsinghua University, Beijing, China, June 3, 1997 (IEEE CAS Distinguished Lecture)

64. "Dedicated and Programmable VLSI Signal Processing Systems," Tokyo Institute of Technology, Tokyo, Japan, June 30, 1997

65. "VLSI Architectures for High-Performance DSP Systems," University of California at Berkeley, Sept. 19, 1997

66. "Low-Power Digital Signal Processing for Multimedia Systems," University of Minnesota (Colloquim Talk), Oct. 9, 1997

67. "Low-Power VLSI Digital Signal Processing for Multimedia Systems," PLENARY TALK, IEEE Biannual Int. Conf. on VLSI Design and CAD, (ICVC), Oct. 12-15, 1997, Seoul, Korea

68. "Low-Power Arithmetic Components," Intel Corporation, Aug. 13, 1998

69. "Low-Power VLSI Digital Signal Processing Systems," Broadcom Corporation, Irvine, California, Aug. 14, 1998

70. "Low-Power Multimedia DSP Systems," ECE Colloq. talk at University of Illinois at Urbana, Sept. 15, 1998

71. "Low-Power Multimedia DSP Systems," Lucent Technologies, Bell Laboratories, Allentown, PA, Sept. 23, 1998

72. "Low-Power DSP Systems for Multimedia Communications," Texas Instruments, Dallas, Oct. 1, 1998

73. "Low-Power Multimedia DSP Systems," EECS Department, Univ. of California, Berkeley, Nov. 2, 1998

74. "Low-Power Multimedia DSP Systems," ECE Dept. Colloq. talk at North Carolina State University, Nov. 30, 1998

75. "Low-Power DSP Components for Multimedia Communications," National Univ. of Singapore, Feb. 22, 1999

76. "Low-Power DSP Components for Multimedia Communications," University of California-Davis, March 10, 1999

77. "Low-Power DSP Components for Multimedia Communications," Broadcom Corporation, March 18, 1999

78. Lectures on VLSI Signal Processing, Lund University, April-May 1999

79. Lectures on VLSI Signal Processing, KTH Royal Institute of Technology, Stockholm, May 1999

80. "Low-Power and High-Speed Computer Arithmetic Architectures," Stanford University, Nov. 23, 1999

81. "Low-Power DSP Components for Multimedia Communications," IEEE Orange County section, Oct. 23, 2000

82. "Low-Power DSP Components for Multimedia Communications," U.C. Santa Barbara, April 20, 2001

83. "Low-Power DSP Components for Multimedia Communications," U.C.L.A., May 16, 2001

84. "Low-Power DSP Systems," NEC Corp., Japan, July 26, 2001

85. "Low-Power DSP Components for Multimedia Systems," Invited Talk at System-on-Chip Conference, Nov. 2001, Tampere

86. "VLSI Architectures for Digital Signal Processing Systems," Invited Talk at St. Cloud State, April 26, 2002

87. "Architectures for Broadband Communications Systems," Seoul National University, Seoul, Korea

88. "Design of High-Speed DSP Receivers," Lund University, Sweden, Sept. 2003

89. "Design of High-Speed DSP Receivers," Linkoping University, Sweden, Sept. 2003

90. "Architectures for Broadband Communications Systems," National Taiwan University, Taipei, Taiwan, Nov. 2003

91. "Architectures for Broadband Communications Systems," National Chiao-Tung University, Taiwan, Nov. 2003

92. "Architectures for Broadband Communications Systems," National Cheng-Kung University, Taiwan, Nov. 2003

93. "VLSI Architectures for Turbo and LDPC Codes," University of California, San Diego, August 2004

94. Presented a talk on "Data Fusion" on Dec. 20, 2006 at Medtronic, Inc.

95. Eminent Speakers Series Colloquim at the University of Virginia (Electrical Engineering Dept.) on Feb. 23, 2007

96. Presented a talk on "Electricity" to 4th Grade students at Providence Academy, April 2007

97. Series of 6 talks on Biomedical Signal Processing, Feature Extraction and Classification at Medtronic, April-May 2007

98. "Feature Extraction and Classification of Biomedical Signals," Indian Institute of Technology, Kharagpur, Jan. 3, 2008

99. "Feature Selection and Classification in Heart Sound," Tech Tuneup, UMN, June 2008

100. Talk on Seizure Prediction, UMN Neuroengineering Center, May 2009

101. Talk on EEG Signal Processing, Medtronic, June 2009

102. Talk on EEG Signal Processing, U.C. Berkeley, Aug. 2009

103. "Signal Processing Device for Seizure Prediction," Neuroengineering Symp., University of Minnesota, Feb. 2, 2010

104. "Digital Signal Processing with Protein Molecules and DNA Strands," Information Systems Lab (ISL) Colloquium, Stanford, Nov. 9, 2010

105. "Digital Signal Processing with Protein Molecules and DNA Strands", CHESS Seminar, University of California, Berkeley, Nov. 10, 2010

106. "Seizure Prediction and Detection", Neuroengineering Symposium, Univ. of Minnesota, Feb. 9, 2011

107. "Processing Signals from EEG Electrodes and Protein Molecules: Convergence of DSP, Machine Learning, and Digital Design," Broadcom, June 7, 2011

108. "Digital Signal Processing for Embedded Communications and Biomedical Systems at Samsung", Korea, May 23, 2012

109. "Language Understanding of Schizophrenic Patients from MEG Data," Neuroengineering Symposium, Univ. of Minnesota, Feb. 16, 2012

110. "Ethics and Professional Conduct for Electrical Engineers," North Central Electrical Engineering Society (NCEES), Minneapolis, October 15, 2013

111. "Biomarkers and Brain Connectivity for Neurological and Psychiatric Disorders," Distinguished Speaker Series, ECE Department, University of Arizona, April 24, 2014

112. "VLSI Systems for Neurocomputing and Health Informatics," Proc. of 2014 ACM Great Lakes Symposium on VLSI, pp. 1-2, Houston, May 2014 (Keynote Talk)

113. "VLSI Computing of Digital Signal Processing Functions," University of Alberta, October 16, 2014

114. "Biomarkers and Brain Connectiviy for Neurological and Psychiatric Disorders", Electrical Engineering Distinguished Talk, University of Alberta, Oct. 17, 2014

115. "Biomarkers and Brain Connectivity for Neurological and Psychiatric Disorders," Minneapolis VA Center, Sept. 28, 2015

116. "Molecular Machine Learning Systems," Workshop on Coding Techniques for Synthetic Biology at the University of Illinois, Urbana, October 30, 2015

117. "Fundus Image Analysis for Retinopathy using Signal Processing and Machine Learning," Univ. of Calgary, Dec. 14, 2015

118. "Network Analysis of Human Brain Connectivity in Psychiatric Patients and Healthy Humans," Neuroengineering/Neuroimaging Seminar, UMN, Feb. 18, 2016

119. "Architectures for Emerging Industrial Internet of Things: Reducing Energy and Enhancing Security," Invited Talk at 2016 NTU-MediaTek IC Design Workshop, Nanyang Technological University, Singapore, Aug. 10, 2016

120. "Brain, Biomedical, and Biomolecular Informatics: Convergence of Signal Processing, Machine Learning and Computing," ECE Colloquium Talk at University of Washington, Seattle, Oct. 25, 2016

121. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," ECE Colloquium Talk at Cornell, Oct. 31, 2016

122. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," IEEE Student Branch, Indian Institute of Technology, Khaagpur, India, Dec. 26, 2016

123. "Computing Signal Processing and Machine Learning Functions using DNA," Indian Institute of Technology, Bhubaneswar, India, Jan. 4, 2017

124. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," S O A University, Bhubaneswar, India, Jan. 6, 2017

125. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," Indian Institute of Technology - Madras, Chennai, India, Jan. 9, 2017

126. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," Indian Institute of Science, Bengaluru, India, Jan. 10, 2017

127. "Authentication and Functional Obfuscation of Integrated Circuits," Texas Instruments, Bengaluru, India, Jan. 13, 2017

128. "Internet of Things: Energy-Efficient Machine Learning Classification and Hardware Security," University of Illinois at Chicago, April 21, 2017

129. "Authentication and Functional Obfuscation of Integrated Circuits," Shanghai Jiao Tong University, June 28, 2017

130. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," Talk in Computer Science and Engineering Dept., Indian Institute Technology, New Delhi, Aug. 25, 2017

131. "Information Analytics, Energy-Efficiency and Hardware Security for Internet-of-Things Applications," Seoul National University, Jan. 26, 2018

132. "Data Analytics and Data-Driven Computing: Applications from Internet-of-Things to Classifying Neuropsychiatric Disorders," University of Texas at Austin, Feb. 15, 2018

133. "Multi-Dimensional Time-Series Data Analysis: A Convergence of Signal Processing and Machine Learning," Shanghai Maritime University, June 8, 2018

134. "Design of Features and Classifiers for Neuro-Psychiatric Disorders via Machine Learning," Fudan University, School of Microelectronics, June 19, 2018

135. "VLSI Architectures for Low-Energy Machine Learning Systems," Fudan University, School of Microelectronics, June 20, 2018

136. "Authentication and Obfuscation of Integrated Circuits," Fudan University, School of Microelectronics, June 21, 2018

137. "VLSI Architectures for Low-Energy Machine Learning Systems," Xi'an Jiao Tong University, School of Microelectronics, July 1, 2018

138. "Internet of Things: Energy-Efficient Data Analytics, and Hardware Security," Tsinghua University, School of Microelectronics, Beijing, China, July 24, 2018

139. "Seizure Prediction and Detection using Machine Learning," Nanyang Technological University (NTU), Singapore, August 30, 2018

140. "Brain Disorders, Brain Connectivity Analysis and Brain-Inspired Computing," Nanyang Technological University (NTU), Singapore, August 31, 2018

141. "Machine Learning: Low-Energy Architectures and Applications," Indian Institute of Technology, Kharagpur, India, September 5, 2018

142. "Machine Learning: Low-Energy Architectures and Applications," Indian Institute of Technology, Bhubaneswar, India, September 6, 2018

143. "Low-Energy VLSI Architectures for Machine Learning Systems and Applications," Stanford University, Oct. 8, 2018

144. "Low-Energy VLSI Architectures for Machine Learning Systems and Applications," Intel, Santa Clara, Oct. 10, 2018

145. "Machine Learning Systems: Low-energy VLSI Architectures and Applications," University of California-Irvine, November 16, 2018