DSP Applications

DSP applications are often real time but with a wide variety of sample rates

• High rates
  – Radar
  – Video

• Medium rates
  – Audio
  – Speech

• Low rates
  – Weather
  – Finance
...with different demands on

- numeric representation
  - float or fixed
  - and number of bits
- Throughput/speed
- Power/energy dissipation
- Cost
DSP features

Fast Multiply/Accumulate (MAC)
- FIR
- FFT
- etc.

- Multiple Access Memories
- Specialized addressing modes
- Specialized execution control (loops)
- Specialized interfaces, e.g. AD/DA
Addressing Modes

- Implied addressing
  \[ P = X \times Y; \] operation sets location
- Immediate data
  \[ AX0 = 1234 \]
- Memory direct
  \[ R1 = \text{Mem}[101] \]
- Register direct
  \[ \text{sub } R1, R2 \]
- Register indirect
  \[ A0 = A0 + \ast R5 \]
- Register indirect with increment/decrement
  \[ A0 = A0 + \ast R5++ \]
  \[ A0 = A0 + \ast R5-- \]
Standard DSP Alternatives

PCs or Workstations
• Non-real time
• low requirements

General purpose microprocessors
• slower for DSP applications
• might be one $\mu$proc. there anyway

Custom
• performance
• low cost at volume
• High development cost
Standard Processors vs. Special Purpose

**Standard Processor**
- Programmable
- Low Design cost
- Standard Interface
- Good supply of tools

**Special Purpose**
- High Calculation Capacity
- Low Power
- User defined Interface
- Variable Wordlength
- Low Price at Volume

**Algorithm**
- Processor Cores
- Domain Specific Processors etc.
Architectural Partitioning

Conflicting req.
- Throughput
- Flexibility
- Power Consumption
- Time to market

Flexibility by using programmable processor core

MIPS intensive algorithms in dedicated HW to increase throughput and save power

Local busses and Distributed memory to decrease data transfers
Fixed point DSP
Motorola DSP56000x

• Usually DSP has single cycle multiplier, may be pipelined
• Double wordlength out
• + guard bits
• scaling
• Alternative is mult with reduced wordlength output, e.g. 24

Operand Registers

Operand
Registers

Shifter

Shifter/Limiter

Accumulators

24 24
24 24
24 24
Memory Structures, von Neuman
Memory Structures, Harvard

Original Harvard
- one data
- one program

Processor Core

Address bus 2
Data bus 2
Address bus 2
Data bus 2

Memory A
Memory B
TI Processors, high speed
TI Processors, low power

C5000 Roadmap to the Future

1st Generation
- C541 40 MIPS
- C542 50 MIPS
- C548 80 MIPS

0.6 mW/MIPS
1/2 the Power

2nd Generation
- C5410 100 MIPS
- C5416 160 MIPS

0.32 mW/MIPS
5x Higher Performance

3rd Generation
- C5510 320/400 MIPS
- C55x Multi-core

140 MIPS
1/6 the Power

- C55x Multi-core
- C55x 800 MIPS

- C55x 600 MIPS

Software Compatible

Announcement of 1st Device: June 12, 2000

Core mW/MIPS

Time
TI, C64
TI, C55
Processor Architectures

SIMD – Single Instruction Multiple Data

Program

Processor Processor Processor Processor
Processor Architectures
MIMD –
Multiple Instruction Multiple Data

Program
Processor

Program
Processor

Program
Processor

Program
Processor
Processor Architectures

VLIW –

Very Long Instruction Words

Control Unit

VLIW Instruction

Functional Unit

Functional Unit

Functional Unit

Functional Unit
Split Processors

Functional units can be split into submodules, e.g. for images (8bits) TI320C80, 1 RISC 4 x 32bit DSP which can be split into 8bit modules
Vector Processors

\[
\begin{array}{c}
\text{V0} & \text{V1} & \text{V0} & \text{V1} \\
\ast & \ast & \ast & \ast \\
\text{M00} & \text{M01} & \text{M10} & \text{M11} \\
+ & + & + & + \\
\text{V0} \ast \text{M00} + \text{V1} \ast \text{M01} & \text{V0} \ast \text{M10} + \text{V1} \ast \text{M11} \\
\end{array}
\quad
\begin{array}{c}
\text{V2} & \text{V3} & \text{V2} & \text{V3} \\
\ast & \ast & \ast & \ast \\
\text{M02} & \text{M03} & \text{M12} & \text{M13} \\
+ & + & + & + \\
\text{V2} \ast \text{M02} + \text{V3} \ast \text{M03} & \text{V2} \ast \text{M12} + \text{V3} \ast \text{M13} \\
\end{array}
\]

\[
\begin{array}{c}
A0 & A1 \\
\end{array}
\]
Low Power MMAC
Multiplier Multiple Accumulator

### Low Power MMAC

#### Schedule 16-tap FIR 4 acc. MMAC

<table>
<thead>
<tr>
<th>Cycle #</th>
<th>acc0</th>
<th>acc1</th>
<th>acc2</th>
<th>acc3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$a_{15} \cdot x(4j - 10)$</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>2-3</td>
<td>$a_{14} \cdot x(4j - 14)$</td>
<td>$a_{15} \cdot x(4j - 14)$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4-6</td>
<td>$a_{13} \cdot x(4j - 13)$</td>
<td>$a_{14} \cdot x(4j - 13)$</td>
<td>$a_{15} \cdot x(4j - 13)$</td>
<td>-</td>
</tr>
<tr>
<td>7-10</td>
<td>$a_{12} \cdot x(4j - 12)$</td>
<td>$a_{13} \cdot x(4j - 12)$</td>
<td>$a_{14} \cdot x(4j - 12)$</td>
<td>$a_{15} \cdot x(4j - 12)$</td>
</tr>
<tr>
<td>11-14</td>
<td>$a_{11} \cdot x(4j - 11)$</td>
<td>$a_{12} \cdot x(4j - 11)$</td>
<td>$a_{13} \cdot x(4j - 11)$</td>
<td>$a_{14} \cdot x(4j - 11)$</td>
</tr>
<tr>
<td>15-18</td>
<td>$a_{10} \cdot x(4j - 10)$</td>
<td>$a_{11} \cdot x(4j - 10)$</td>
<td>$a_{12} \cdot x(4j - 10)$</td>
<td>$a_{13} \cdot x(4j - 10)$</td>
</tr>
<tr>
<td>19-22</td>
<td>$a_{9} \cdot x(4j - 9)$</td>
<td>$a_{10} \cdot x(4j - 9)$</td>
<td>$a_{11} \cdot x(4j - 9)$</td>
<td>$a_{12} \cdot x(4j - 9)$</td>
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<tr>
<td>23-26</td>
<td>$a_{8} \cdot x(4j - 8)$</td>
<td>$a_{9} \cdot x(4j - 8)$</td>
<td>$a_{10} \cdot x(4j - 8)$</td>
<td>$a_{11} \cdot x(4j - 8)$</td>
</tr>
<tr>
<td>27-30</td>
<td>$a_{7} \cdot x(4j - 7)$</td>
<td>$a_{8} \cdot x(4j - 7)$</td>
<td>$a_{9} \cdot x(4j - 7)$</td>
<td>$a_{10} \cdot x(4j - 7)$</td>
</tr>
<tr>
<td>31-34</td>
<td>$a_{6} \cdot x(4j - 6)$</td>
<td>$a_{7} \cdot x(4j - 6)$</td>
<td>$a_{8} \cdot x(4j - 6)$</td>
<td>$a_{9} \cdot x(4j - 6)$</td>
</tr>
<tr>
<td>35-38</td>
<td>$a_{5} \cdot x(4j - 5)$</td>
<td>$a_{6} \cdot x(4j - 5)$</td>
<td>$a_{7} \cdot x(4j - 5)$</td>
<td>$a_{8} \cdot x(4j - 5)$</td>
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<tr>
<td>39-42</td>
<td>$a_{4} \cdot x(4j - 4)$</td>
<td>$a_{5} \cdot x(4j - 4)$</td>
<td>$a_{6} \cdot x(4j - 4)$</td>
<td>$a_{7} \cdot x(4j - 4)$</td>
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<tr>
<td>43-46</td>
<td>$a_{3} \cdot x(4j - 3)$</td>
<td>$a_{4} \cdot x(4j - 3)$</td>
<td>$a_{5} \cdot x(4j - 3)$</td>
<td>$a_{6} \cdot x(4j - 3)$</td>
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<tr>
<td>47-50</td>
<td>$a_{2} \cdot x(4j - 2)$</td>
<td>$a_{3} \cdot x(4j - 2)$</td>
<td>$a_{4} \cdot x(4j - 2)$</td>
<td>$a_{5} \cdot x(4j - 2)$</td>
</tr>
<tr>
<td>51-54</td>
<td>$a_{1} \cdot x(4j - 1)$</td>
<td>$a_{2} \cdot x(4j - 1)$</td>
<td>$a_{3} \cdot x(4j - 1)$</td>
<td>$a_{4} \cdot x(4j - 1)$</td>
</tr>
<tr>
<td>55-58</td>
<td>$a_{0} \cdot x(4j)$</td>
<td>$a_{1} \cdot x(4j)$</td>
<td>$a_{2} \cdot x(4j)$</td>
<td>$a_{3} \cdot x(4j)$</td>
</tr>
<tr>
<td>59-61</td>
<td>$a_{0} \cdot x(4j + 1)$</td>
<td>$a_{1} \cdot x(4j + 1)$</td>
<td>$a_{2} \cdot x(4j + 1)$</td>
<td>$a_{3} \cdot x(4j + 1)$</td>
</tr>
<tr>
<td>62-63</td>
<td>$a_{0} \cdot x(4j + 2)$</td>
<td>$a_{1} \cdot x(4j + 2)$</td>
<td>$a_{2} \cdot x(4j + 2)$</td>
<td>$a_{3} \cdot x(4j + 2)$</td>
</tr>
<tr>
<td>64</td>
<td>$a_{0} \cdot x(4j + 3)$</td>
<td>$a_{1} \cdot x(4j + 3)$</td>
<td>$a_{2} \cdot x(4j + 3)$</td>
<td>$a_{3} \cdot x(4j + 3)$</td>
</tr>
</tbody>
</table>