Self-assembly of microscopic chiplets at a liquid–liquid–solid interface forming a flexible segmented monocrystalline solar cell

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This paper introduces a method for self-assembling and electrically connecting small (20–60 micrometer) semiconductor chiplets at predetermined locations on flexible substrates with high speed (62500 chips/45 s), accuracy (0.9 micrometer, 0.14°), and yield (>98%). The process takes place at the triple interface between silicone oil, water, and a penetrating solder-patterned substrate. The assembly is driven by a stepwise reduction of interfacial free energy where chips are first collected and preoriented at an oil-water interface before they assemble on a solder-patterned substrate that is pulled through the interface. Patterned transfer occurs in a progressing linear front as the liquid layers recede. The process eliminates the dependency on gravity and sedimentation of prior methods, thereby extending the minimal chip size to the sub-100 micrometer scale. It provides a new route for the field of printable electronics to enable the integration of microscopic high performance inorganic semiconductors on foreign substrates with the freedom to choose target location, pitch, and integration density. As an example we demonstrate a fault-tolerant segmented flexible monocrystalline silicon solar cell, reducing the amount of Si that is used when compared to conventional rigid cells.

flexible solar cells | fluidic self-assembly | macroelectronics | printable electronics | solder-directed self-assembly

Progress in the fields of microelectronics and microoptics has traditionally been measured by the level of overall miniaturization. The emerging field of macro and printable electronics, however, has a different set of goals and draws attention to new manufacturing methods that enable large-area integration, preferably on flexible low temperature plastic substrates. Manufacturing processes employed to deliver the integrated materials include inkjet printing, parallel transfer, robotic pick-and-place, and fluidic self-assembly. Inkjet printing is most suitable to produce low-performance devices, whereas parallel transfer, robotic pick-and-place, and fluidic self-assembly aim to integrate higher performance inorganic devices formed by high temperature processes prior to integration; inorganic devices provide orders of magnitudes higher switching speeds due to the much higher carrier mobility, occupy orders of magnitude less area due to the superior conductance and thus require less material and cost per function when compared to their organic counterparts. Motivated by the higher performance and cost advantage per function of inorganic semiconductors, parallel transfer (1–4) and self-assembly techniques (5–9) have been advanced in recent years to integrate, among others, ZnO (10), GaAs (7, 11), InP (12), GaN (13, 14), and Si (2, 3, 8, 15, 16) on flexible low temperature substrates in a massively parallel fashion. Demonstrated applications include flexible (17) and curved displays (8), curved focal plane arrays (2), oscillators (3), radio frequency identification (RFID) tags (18), and solar cells (4). Transfer techniques, when compared to engineered self-assembly methods, use a donor substrate/wafer and maintain orientation and integration density that is in stark contrast to directed/engineered self-assembly, which can redistribute components over large areas and order unorganized parts. For example, a container full of semiconductor dies/chiplets can be redistributed and assembled at precise locations on a substrate at any desired pitch or required function density using methods of directed self-assembly (19).

At present there are two comparable self-assembly methods to assemble semiconductor dies/chiplets with yields approaching 100%. The first method uses gravity in combination with complementary 3D shapes to assemble trapezoidal Si dies onto plastic substrates to produce RFID tags (6, 20, 21). The second method relies on gravity in combination with surface tension-directed assembly, either using hydrophilic/hydrophobic surface patterns (22–25) or solder-patterned surfaces to assemble semiconductor dies/chiplets with similar yields (7–9, 13, 26). Solder-directed self-assembly provides the ability to form electrical interconnects and has been applied to flip-chip assembly with unique contact pad registration (27), the packaging of light emitting diodes (7, 13, 26), the formation of transponders that can be interrogated remotely (27), the assembly of uni- (8) and multicolor (28) display segments, as well as multicomponent circuits (5) on flexible substrates. Interestingly, the minimal component size for high-yield assemblies of electronic components has been limited to >100 μm sized chiplets using current methods primarily because gravity-driven sedimentation used to introduce the components to the substrate has not been effective at the <100 μm length scale. Gravitational forces scale with the volume and are ineffective in delivering highly scaled components that remain suspended in solution during agitation. This report describes a new surface tension-directed self-assembly approach that eliminates this dependency on gravity and sedimentation. Instead, the method uses a liquid–liquid–solid interface to define a progressing linear front for the self-assembly to take place in a conveyor belt-like fashion. The process has been engineered to provide a stepwise reduction of the interfacial free energy providing an energy cascade to (*i*) transport, (*ii*) preorient, and (*iii*) assemble microscopic components at predefined surface areas. The prototype system enables the assembly of smaller components than previously possible and achieves a higher throughput; 62 thousand components are assembled and electrically connected in 3 min. The approach is tested using 20–60 μm sized chiplets made out of SU-8 and Si. Assembly yields ranged between 98%–100%. The positional accuracy exceeds previous results: 0.9 μm lateral and 0.14° (SD) angular positional accuracy is observed. As an application we demonstrate the fabrication of a segmented flexible monocrystalline silicon solar cell using silicon dies that are 20 μm thin to reduce the required use of Si by a factor of 10 when compared to conventional 300 μm thick and rigid monocrystalline solar cells.

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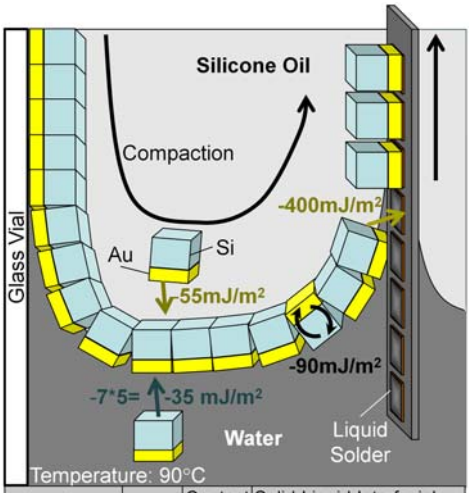
Results and Discussion

Fig. 1 illustrates the experimental strategy of surface tension-directed self-assembly of ultra small dies at a liquid–liquid–solid interface. The process uses a stepwise reduction of the interfacial energy to (*i*) move components from a suspension to the interface (55 mJ/m^2), (*ii*) preorient the components within the interface to face in the right direction (90 mJ/m^2), and (*iii*) assemble the components on molten solder through dipping (400 mJ/m^2). To achieve this energy cascade it is necessary to correctly choose and/or adjust the surface energies. We tested a water–oil interface and components made out of SU-8 and silicon (20 μm wide, 20 μm deep, 10 μm thick and 60 μm wide, 60 μm deep, and 20 μm thick, respectively) with a gold coated contact on one face. The gold surface was treated with a mercaptoundecanoic acid (MUA) self assembled monolayer in a 10 mM (ethanol) solution for 15 min to render it hydrophilic, while the silicon faces were treated to become hydrophobic using 3-glycidoxypropyltrimethoxysilane (GPTMS, Dow Corning Z-6040) by soaking with 200 mM GPTMS in ethanol for 15 min followed by a dehydration bake at 115 °C for 5 min. The SU-8 surface was hydrophobic and needed no adjustments. These treatments yield the measured tabulated (Fig. 1, *Lower*) contact angles and interfacial energies between the solids and liquids as determined using Young's equation $\gamma_{s,1} = \gamma_s - \gamma_1 \cos(\theta_{s,1})$ (29) where γ_s (usually not unknown) is the surface energy of the solid, γ_1 (known) is the surface energy of the liquid, and $\theta_{s,1}$ is the measured contact angle (known). The surface energy of water, silicone oil, and solder (Y-LMA-117, mp. 47 °C, Small Parts) are 72, 20, ~500 mJ/m^2, respectively, at a temperature of 95 °C where the solder is molten. The surface energies of the solids γ_s (typically unknown) are not needed as this parameter cancels out when computing the energy differences. For example, considering the illustrated cubic component, the transition from being immersed in oil to the interface is favored because the hydrophilic gold surface prefers to be in contact with water instead of oil; transfer to the liquid–liquid interface is favored by 55 mJ/m$^2 = \gamma_{\text{Au,water}} - \gamma_{\text{Au,oil}} = \gamma_{\text{oil}} \cos(\theta_{\text{Au,oil}}) - \gamma_{\text{water}} \cos(\theta_{\text{Au,water}})$. The components are confined to this interface because they face a 35 mJ/m$^2 = (\gamma_{\text{Si,oil}} - \gamma_{\text{Si,water}}) * 5 = (\gamma_{\text{water}} \cos(\theta_{\text{Si,water}}) - \gamma_{\text{oil}} \cos(\theta_{\text{Si,oil}})) * 5$ energy barrier preventing them from completely entering the water because the 5 hydrophobic Si sides prefer to remain in contact with oil instead of water. For a cube to be oriented upside down within the interface would require the sum of 90 mJ/m^2. Consequently, the components are introduced to the solder with the correct orientation whereby the gold side faces the solder with a water layer in between. Solder has a higher affinity to wet the gold contact than water and attachment is favored by 400 mJ/m^2.



Solid	Liquid	Contact Angle	Solid-Liquid-Interfacial-Energies $\gamma_S - \gamma_L \cos(\theta)$	
Au+MUA (hydrophilic)	Oil	30°	$\gamma_{MUA\text{-}Au}$ - 17 mJ/m²	-55
Au+MUA (hydrophilic)	Water	5°	$\gamma_{MUA\text{-}Au}$ - 72 mJ/m²	-400
Au+MUA (hydrophilic)	Solder	20°	$\gamma_{MUA\text{-}Au}$ - 470 mJ/m²	
Si+GPTMS (hydrophobic)	Water	80°	$\gamma_{Z6040\text{-}Si}$ - 13 mJ/m²	-7
Si+GPTMS (hydrophobic)	Oil	2°	$\gamma_{Z6040\text{-}Si}$ - 20 mJ/m²	

Fig. 1. Procedure of surface tension-directed self-assembly at a liquid–liquid–solid interface employing an energy cascade to (*i*) move components from a suspension to the interface (55 mJ/m^2), (*ii*) preorient the components within the interface to face in the right direction (90 mJ/m^2), and (*iii*) assemble the components on molten solder through dipping (400 mJ/m^2). The illustration depicts the situation for an oil–water interface and chiplets made out of Si (SU-8 is detailed in main body), which carry an Au contact on one face. Depicted Au and Si surfaces are treated using hydrophilic MUA and hydrophobic GPTMS functional groups and yield the tabulated measured contact angles, calculated solid–liquid interfacial energies, and energy differences (gray boxes to the right) required to drive the assembly. The available area and curved shape of the interface cause the components to form a closely packed 2D sheet. Upward motion of substrate yields a dynamic contact angle where the receding water layer becomes sufficiently thin for the gold to contact the solder. Patterned assembly on solder is favored by 400 mJ/m^2 within this layer.

The actual transfer and self-assembly onto the substrate occurs as the sample is pulled upward through the interface (Fig. 1). Upward motion at a typical speed of 30 mm/s reduces the contact angle forming a receding water layer that becomes sufficiently thin for the gold to contact the solder. Transfer onto the solder-coated substrate occurs within this thin progressing interface in a conveyor belt-like fashion. For the assembly to work well, the conditions that follow were essential. The temperature has to be maintained constant, which is achieved using a heated ethylene glycol bath that is kept at 95 °C surrounding the glass assembly container. Metal surfaces including the solder need to be free of surface oxide, which is achieved by reducing the pH of the assembly solution to pH 2.0 by adding drops of hydrochloric acid. It is possible to get good >90% coverage in a single pass; however, full coverage (99%–100%) required several passes through the interface. Assembly in this system occurs only during upward motion. Downward motion removes loose unassembled components that transition back to the liquid–liquid interface. Saturation is observed in 5–10 passes, which takes <1 min. The short <1 min. assembly time is an important advantage over previous settled assembly trials for reasons further detailed in the reference section [*].

Fig. 2 shows patterned self-assembly results of Si and SU-8 with 20 μm and 60 μm side lengths. Assembly with different area densities is tested using regular arrays [approximately 25% area density (Fig. 2*A* and *B*)] and arbitrary text [<5% area density (Fig. 2*A* and *B* insets)]. Defects, measured by the cumulative number of missing, misaligned, and excess components, were found to be independent of the area density, component type, and component size. For example, Fig. 2*A* depicts 100 receptors

*Solder directed assembly is sensitive to surface oxides that reduce the surface energies driving the self-assembly and self-alignment. As a result all metal surfaces including the solder need to be free of surface oxide, which is achieved by reducing the pH of the assembly solution to be slightly acidic, here to pH 2.0. Residual oxygen, however, cannot be completely eliminated and re-oxidation and oxide removal is a continuous process, which results in loss and change of the solder composition over time. This is the case for all self-assembly methods involving liquid solder and it is therefore important to limit the total assembly time. This especially important for the discussed highly scaled components where the solder volume is 2–3 orders of magnitude smaller than what was used before. The reduced solder volume together with slower progression of prior methods (8) that did depend on gravity and sedimentation to transport the components to the surface caused prior methods to come to a complete stop before full coverage was reached. This problem has been overcome in this study. At assembly times of <1 min we did not detect negative effects due to oxidation.

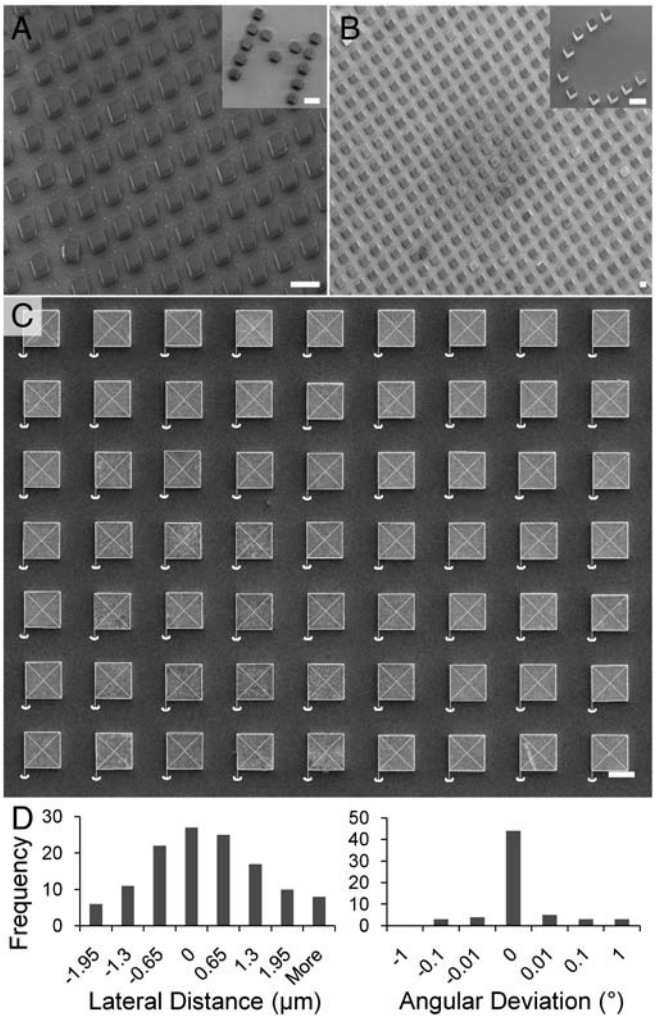


Fig. 2. SEM of (*A*) SU-8 (20 μm side length) and (*B*, *C*) Si chiplets (20 μm and 60 μm side length) assembling in regular arrays and arbitrary text patterns (insets). The overlaid CAD guides visible in (*C*, white lines) are used to measure variations in the center-to-center distance and angular-orientation. (*D*) Histogram of measured variations. 40 μm scale bars.

carrying a single SU-8 component where one is misaligned reducing the yield to 99%. Fig. 2*B* depicts approximately 400 receptors, and each receptor carries a correctly aligned Si chiplet, however, three additional components were found to be present reducing the yield to 99.3%. These pictures are representative images of assemblies that extend over larger areas, currently limited to 1 cm long and wide substrates; the present assembly system has a 1 cm^2 interfacial area/capacity, which provides room for approximately 250 thousand 20×20 μm sized dies. The number of components that transfer onto the surface depends on the area covered by solder. For example, for the intermediate 25% area density test structures (Fig. 2*A* and *B*) approximately 62,500 components assemble onto the substrate in 45 s. Components assemble with good alignment accuracy, which is determined using overlaid CAD measurement guides. For example, 60 μm sized high precision Si components (Fig. 2*C*) yield an average placement accuracy of 0.9 μm (STD) and angular orientation accuracy of 0.14° (STD) (Fig. 2*D*) that are, respectively, 21 and 2.2 times better than previously reported (9). The observed accuracy does not represent the limits of the self-assembly process itself because the recorded numbers fall within the precision of the lithography and etching methods used to produce the components and receptors—the lateral dimensions of the Si blocks varied by 1 μm, SU-8 blocks varied by 1.5 μm, receptors on Si varied by 1 μm, and receptors on propylene terepthalate (PET) varied by as much as 2.5 μm. Additionally, SU-8 blocks had rounded corners with 2 μm radius of curvature, which was smaller than the observed 3–4 μm radius of curvature of the solder-coated
receptors.

The process is scalable toward both larger and smaller component dimensions. Considering macroscopic dimensions, gravity sets a scaling limit. Gravitational forces scale with the volume (x^3 for cubic components) yielding an energy gain over a distance x, which is proportional to x^4. The energy gain due to the reduction of surface free energy scales with the area x^2 and become less important at macroscopic scales. For example, gravity causes a 1 cm^3 cube (Fig. 3*A*) of hydrophobic Si with a hydrophilic metal contact to drop through the oil–water interface whereas 1 mm (Fig. 3*B*, square) and 100 μm (Fig. 3*C*, triangular) sized components are correctly captured by the interface, transported, and assembled. The upper limit for the lateral dimensions can be pushed upward by using components with reduced density or thickness. Considering an extension toward nanoscopic dimensions, the thermal energy (32 meV at 95 °C) provides a theoretical scaling limit. The interfacial energy gain (here larger than 50 mJ/m^2) exceeds the Brownian energy by many orders of magnitude until the components reach sub molecular (<1 nm^2) dimensions, suggesting that a continued scaling is possible; the self-assembly of phospholipids into two dimensional sheets at an oil–water interface can be seen as an analogue to provide experimental evidence that this might be possible. Experimentally, however, the process is challenged by the ability to realize receptors that remain stable over time. Solder-directed assembly is sensitive to surface oxides that reduce the surface energies driving the self-assembly and self-alignment. As a result, all metal surfaces including the solder need to be free of surface oxide, which is achieved by reducing the pH of the assembly solution to be slightly acidic, here to pH 2.0. Residual oxygen, however, cannot be completely eliminated and reoxidation and oxide removal is a continuous process, which results in loss and change of the solder

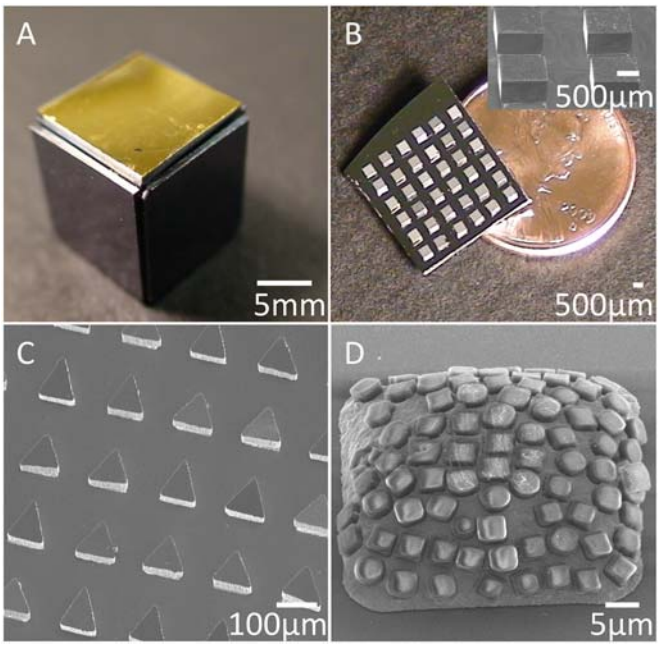


Fig. 3. Scaling limits illustrating components and assembly spanning 3 orders of magnitude in size including (*A*) 1 cm Si cubes (assembly not possible), (*B*) 1 mm Si blocks (assembly possible), (*C*) 100 μm Si triangle (assembly possible), and (*D*) 3 μm-sized SU-8 blocks and discs (discussed in the text).

composition over time. This is especially important for highly scaled receptors because the solder volume drops with x^3 for dip-coated receptors. At present a $20 \times 20 \times 10$ μm^3 solder bump remains sufficiently stable to complete the assembly, which is not observed for $1 \times 1 \times 0.5$ μm^3 bump where the solder volume is 3 orders of magnitudes smaller and less stable over time. Whereas the solder oxidation is a challenge, the general process of surface tension-directed chip assembly using an energy cascade to transport and preorient the components should remain intact at much smaller scales. There is some experimental evidence supporting this statement. Fig. 3*D* shows a stable $20 \times 20 \times 10$ μm^3 solder bump used to capture $3 \times 3 \times 2$ μm^3 sized SU-8 objects. Transport and assembly remains intact for these highly scaled components and we anticipate scaling to continue if solutions are found to form highly scaled receptors that maintain stable over time.

Fig. 4 illustrates an application of the process realizing a segmented monocrystalline solar cell on a flexible PET substrate while reducing the material use of Si by a factor of 10 when compared to conventional monocrystalline cell architectures. The material reduction was achieved by using 20 μm thin silicon chiplets instead of commonly used 200–300 μm thick Si wafers where most of the Si is used to provide a mechanical support. The difference between the Si chiplets in this figure and the Si chiplets used in previous test experiments is that they carry a p-n junction, which is fabricated using an LPCVD-deposited phosphosilicate glass (PSG) dopant layer and a high temperature diffusion step prior to their assembly onto the flexible PET substrate; the section on component fabrication provides further details. The 20 μm thin layer of Si adds little height to the 175 μm thick PET substrate. Another difference shown in Fig. 4*A* is that the PET substrate carries a common copper contact on the entire surface, which is partially masked with chromium to prevent wetting of solder in undesired areas; solder does not wet chromium. The process steps to form the solar cells use an SU-8 isolation layer, which is applied by spin coating before it is etched back in a reactive ion etcher to reveal the p-doped region of the chips. The section on component fabrication provides further details. The process is designed to be tolerant of assembly defects (Fig. 4*B*) where SU-8 fills in voids and locations of missing dies (vacancies); SU-8 and other polymers form a thinner film over protruding objects when compared to valleys when spun. This self-leveling behavior makes the cells tolerant against assembly defects; a missing Si diode (highlighted region, Fig. 4*B*) will not result in a short and failure of the cell because these regions are coated with SU-8. As a top contact we used a semitransparent 20 nm thin sputter deposited film of Au (Fig. 4*C*), however, materials including transparent conducting oxides could be used as well. Fig. 4*D* depicts a respective closeup (SEM) of the completed structure. We tested the cells before and after assembly and found very little difference in terms of their electrical properties (Fig. 4*E*). Individual cells that were released from the wafers had 4.4% power conversion efficiencies, 0.34 V open circuit voltage, and 0.67 filling factor at 0.7 suns (Philips PAR38 lamp, calibrated with an International Light Technologies 1400-A photometer), which could be improved to established levels by incorporating an intrinsic region and through optimization of doping levels/profiles, geometry, antireflection coatings, surface passivation layers, and contacts, which is outside of the focus of this work. The cells retained their electrical properties when assembled (4.2% efficiency 0.30 V, 0.56FF) (red line), confirming that the assembly procedure and exposure to the oil–water interface does not alter the cells. Similarly, the electrical properties changed only slightly (3.8%, 0.31 V, 0.55FF) (black line) when bent as long as the radius of curvature remains above 1 cm. The change in the recorded I/V curve between bent and unbent structures is reversible suggesting that a change in the local illumination angle is the likely cause. We repeated the assembly of modules as shown in Fig. 4*F* several times and found a slight

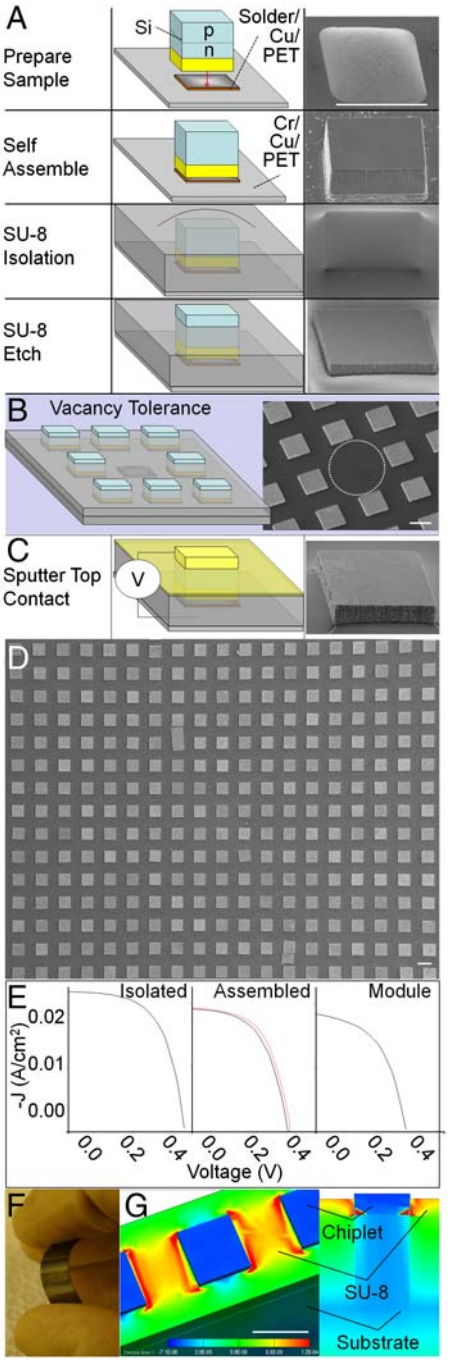


Fig. 4. Flexible segmented monocrystalline solar cell fabrication procedure, result, and characterization. (*A*) Assembly and isolation process next to SEM representative of each step. (*B*) Defect tolerant design strategy and result (SEM) where vacancies are covered with SU-8, preventing shorts to the substrate. (*C*) Top contact deposition process and representative SEM. (*D*) Micrograph of an assembled array. (*E*) IV load curves of cells before (left) and after assembly in unbent (red curve, center) and bent configuration (1 cm radius of curvature, black curve, center); (*E*, right) IV load curve of a module as depicted in (*F*); (*G*) Finite element computer simulation (Coventor-Ware) of the strain inside the composite flexed (1 cm radius of curvature) structure composed of a 175 μm PET layer holding a 20 μm thin film of Si cubes surrounded by SU-8 where the region of maximum strain is located at the top metal contact between silicon cells and at the chiplet edges. Perspective and side slice views are shown. 60 μm scale bars.

reduction in the open circuit voltage and short circuit current when compared to the original isolated cells. For example the module (marked as module) had an efficiency, which was 1%

smaller when compared with the original isolated cells (marked as isolated). This decrease in efficiency as the components are connected in parallel is likely due to variances in component doping, top contact uniformity, and isolation layer thicknesses. We have not yet tested effects of fatigue and minimal possible radius of curvature of bent structures but have observed situations where the top contact failed. The top contact and chiplet edges are the locations of highest strain, which is consistent with finite element modeling (CoventorWare Suite, Coventor Inc.) of the structure (Fig. 4*G*).

Conclusions

We demonstrated a surface tension-directed self-assembly approach to assemble and electrically connect microscopic chiplets at predetermined locations on flexible supports. The liquid–liquid–solid interface proved to be a successful mechanism to deliver highly scaled components to the substrate primarily because it eliminates the dependency on gravity and sedimentation exhibited by prior concepts, which were limited to >100 μm sized chips. Minimal chiplet size (20 μm), throughput (62,500 chips/45 s), and positional accuracy (0.9 μm, 0.14°) exceed prior high yield ($>98\%$) chip-to-substrate self-assembly methods. We anticipate that the method can be further improved through automation. The ability to define a triple interface and linear front where components arrive at the surface in a compacted preoriented fashion, much like in a Langmuir trough, provides a number of new opportunities to facilitate transfer of semiconductor chiplets to predefined locations on foreign substrates. "Roll-to-roll" like system prototypes are possible extensions. Applications should not be limited to solar cells. It should also be possible to combine the method with known concepts of geometrical shape recognition (5, 9) to achieve microscopic flip-chip integration forming multiple interconnects to a single face. Integration and distribution of microscopic light source, signal processing, energy producing elements should be possible over increasingly large surfaces.

Materials and Methods

SU-8 Component Fabrication. SU-8 components were fabricated on a 500 μm thick p-type silicon handling wafer (Ultrasil). A 13 nm release layer of Omnicoat (Microchem) was spun on the wafer at 3000 rpm for 30 s and baked for 1 min at 200 °C. SU-8 2010 (MicroChem) was then spin coated at 3,000 rpm for 30 s and baked at 65 °C for 1 min and 95 °C for 2 min. The 20 μm components were defined by an 132 mJ/cm^2 UV exposure and cured with a post exposure bake of 65 °C for 1 min and 95 °C for 2 min. The SU-8 was developed for 4 min in propylene glycol methyl ether acetate (PGMEA). Next the Omnicoat layer surrounding the newly revealed SU-8 blocks was removed by a 40 s oxygen plasma reactive ion etch clean (O_2-100 sccm-100 W-100 mTorr). A 200 Å adhesion layer of chromium and a 3,000 Å thick gold binding site were then deposited by e-beam evaporation and the sacrificial Omnicoat layer was underetched by Microposit MF-319 developer (Shipley), releasing the SU-8 components. These completed blocks were finally rinsed in isopropyl alcohol by pipette and were then introduced to a 10 mM solution of mercaptoundecanoic acid in ethanol for 15 min to apply a hydrophilic self-assembled monolayer to the gold. After one more rinse step by pipette in isopropyl alcohol, the SU-8 component fabrication was complete. Results seen in Fig. 2.

Solar Cell Fabrication. The silicon solar cell components were fabricated on a p-type silicon on insulator wafer (SOI, 20 μm device layer, 0.095–0.1 Ω/cm^2, Ultrasil) that was first cleaned using a standard wet chemical clean: 1:1:5 solution of $NH_4OH + H_2O_2 + H_2O$ at 80 °C for 15 min, 1:50 solution of $HF + H_2O$ at 25 °C for 15 s, 1:1:6 solution of $HCl + H_2O_2 + H_2O$ at 80 °C for 15 min, and finally $HF + H_2O$ at 25 °C for 15 more seconds with a DI water rinse after each step. Following the clean, the surface p-type device layer was doped n-type using 3,500 Å of LPCVD-deposited PSG as a source. The phosphorous dopant was diffused into the silicon in a nitrogen ambient at 1,150 °C for 3 h in a furnace and the remaining PSG was stripped in a 1 min buffered oxide etch. The wafer was once again cleaned with the RCA process before being immediately inserted in an e-beam evaporation deposition system and coated with a 200 Å adhesion layer of chromium and a 2,000 Å thick binding site pad of gold. The wafer was then photolithographically patterned by exposing spin coated photoresist (Microposit 1813, Shipley) with 96 mJ/cm^2 UV light. After a 25 s developing step in 1 MIF-351:5 H_2O developer, the patterned wafer was ready to be etched. First the gold surrounding the component pads was removed in GE-6 (1:10) (Acton Technologies, Inc.) for 9 min. Second, the chromium was etched in Cr-12S (1:4) (Cyantek, Corp) for 80 s. Finally, the field silicon was etched using a Bosch process in a deep reactive ion etch with the SOI buried oxide acting as the etch stop. The sacrificial buried oxide layer was etched in 49% HF for 7 min to release the completed monocrystalline silicon solar cells. The released cells were treated with a 10 mM mercaptoundecanoic acid (MUA) in ethanol solution for 15 min to to render the gold surface hydrophilic, and rinsed in isopropyl alcohol, and treated with 200 mM hydrophobic glycidoxy functional methoxy silane, Dow Corning Z-6040, in ethanol for 15 min, followed by a dehydration bake at 115 °C for 5 min to render the Si surface hydrophobic.

Silicon Substrate Fabrication. A 500 μm thick p-type silicon wafer (Ultrasil) was patterned by liftoff to serve as the self-assembly substrate. The wafer was first cleaned in a sulfuric acid and hydrogen peroxide solution at 115 °C for 15 min before being rinsed, etched in HF (1:10), and dump rinsed again. Photoresist (Microposit 1813, Shipley) was then spin coated at 2,500 rpm for 30 s. After a soft-bake at 105 °C for 1 min, the substrate was patterned with 96 mJ/cm^2 UV light and developed in 1 Microposit 351:5 H_2O developer for 25 s. A 15 s descum in an oxygen reactive ion etch next ensured subsequent metal adhesion. The 200 Å Cr and 3,000 Å Cu pads were then deposited in an e-beam evaporator. Acetone was used as a solvent to lift off the metal and leave behind the patterned pads on silicon. Finally, the pads were dip-coated with solder (Y-LMA-117, mp. 47 °C, Small Parts). Results seen in Figs. 2 and 3.

Conductive Flexible PET Substrate Fabrication. A 170 μm thick sheet of propylene terepthalate (PET) used to create a self-assembly substrate that featured a conductive backplane. The PET surface was cleaned by soaking in isopropyl alcohol for 10 min and then treated in a 100 W reactive ion etch ammonia plasma for 30 min. Immediately following the plasma surface treatment, the PET was sputter-coated with 3,000 Å (11 min, 250 W) of copper, followed by 200 Å (2 min, 250 W) of chromium. AP-300 (Silicon Resources) adhesion promoter was applied by spin coating at 3,000 rpm for 30 s. A spin on glass (SOG, Accuglass 111) etch mask was applied at 3,000 rpm for 30 s, soft baked for 2 min at 80 °C on a hotplate, and 1 h at 100 °C in an oven. Adhesion promoter hexamethyldisilazane was introduced in vapor form for 2 min. Photoresist (Microposit 1813, Shipley) was applied by spin coating and exposed with 96 mJ/cm^2 UV light. After a 25 s developing step in 1 MIF-315:5 H_2O developer, the SOG etch mask was etched in a reactive ion etcher (150 W, 75 mTorr, Ar:50 sccm, CF_4:25 sccm, CHF_3:50 sccm) forming windows down to the chromium layer. Acetone was used to remove the surrounding photoresist and the chromium was etched using Chromium Cermet Etchant TFE (Transene Company, Inc) in 2 min revealing the copper squares. The SOG mask is easily removed with a 30 s HF dip. Finally, the solder was applied to the copper squares by dip-coating the substrate in a bath of molten solder (Y-LMA-117, mp. 47 °C, Small Parts). Results seen in Fig. 4.

Self-Leveling Polymeric Isolation Process. Following self-assembly, SU-8 2010 was spin coated at 2,500 rpm for 30 s over the sample surface and soft baked at 65 °C for 10 min. It was then flood-exposed with 200 mJ/cm^2 UV light, post-exposure baked for 10 min at 65 °C, washed in propylene glycol methyl ether acetate for 4 min, and etched back using a reactive ion etcher (CF_4:20 sccm, O_2:80 sccm, 200 W, 100 mT). Finally, 20 nm of Au was sputtered by a DC magnetron sputterer.

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