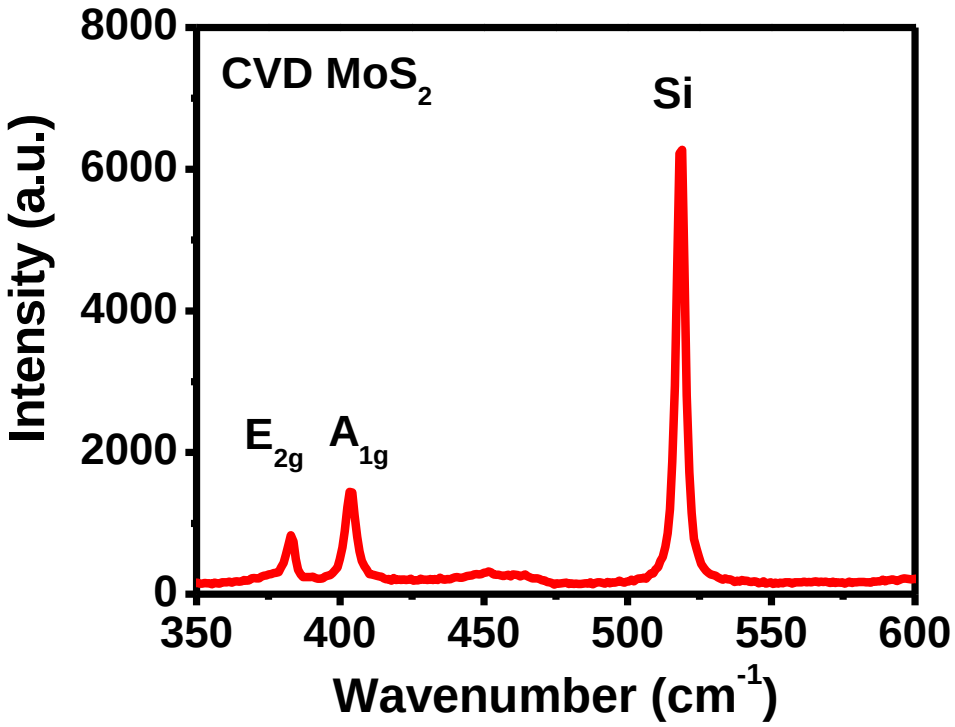
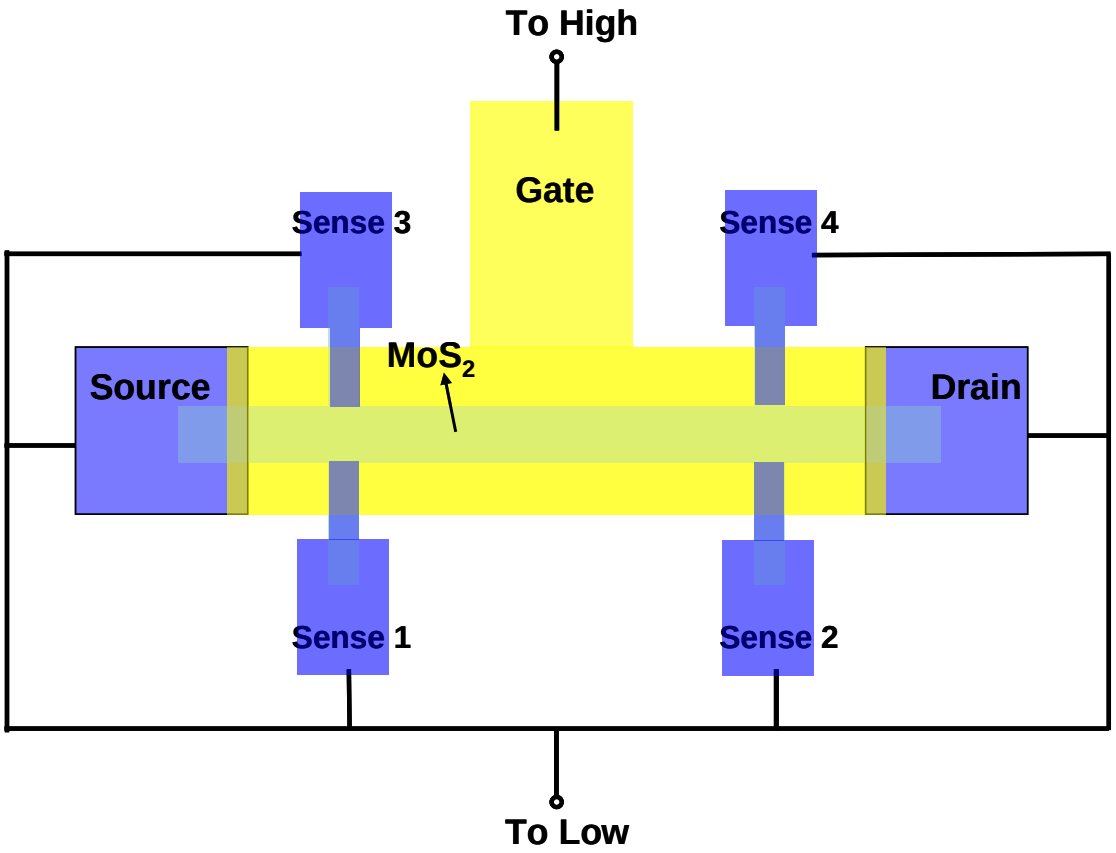
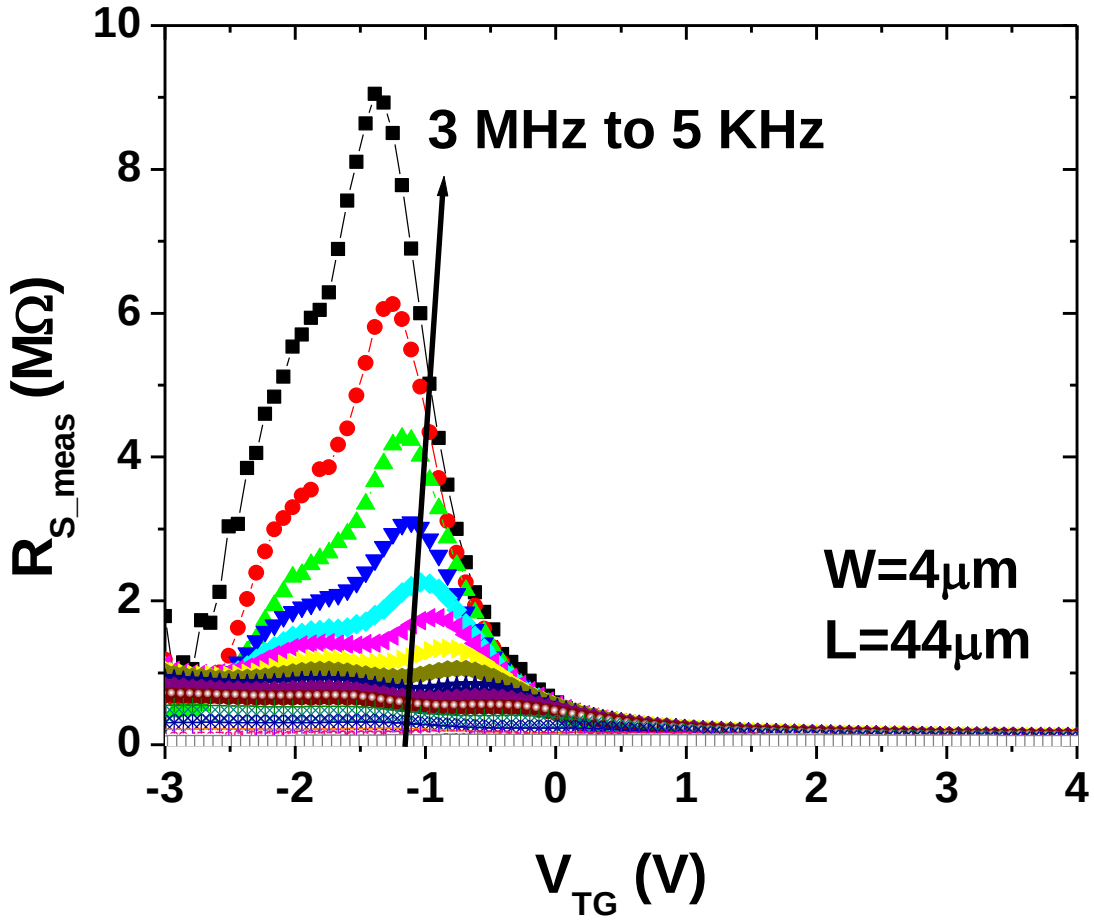
Supplementary Figures:



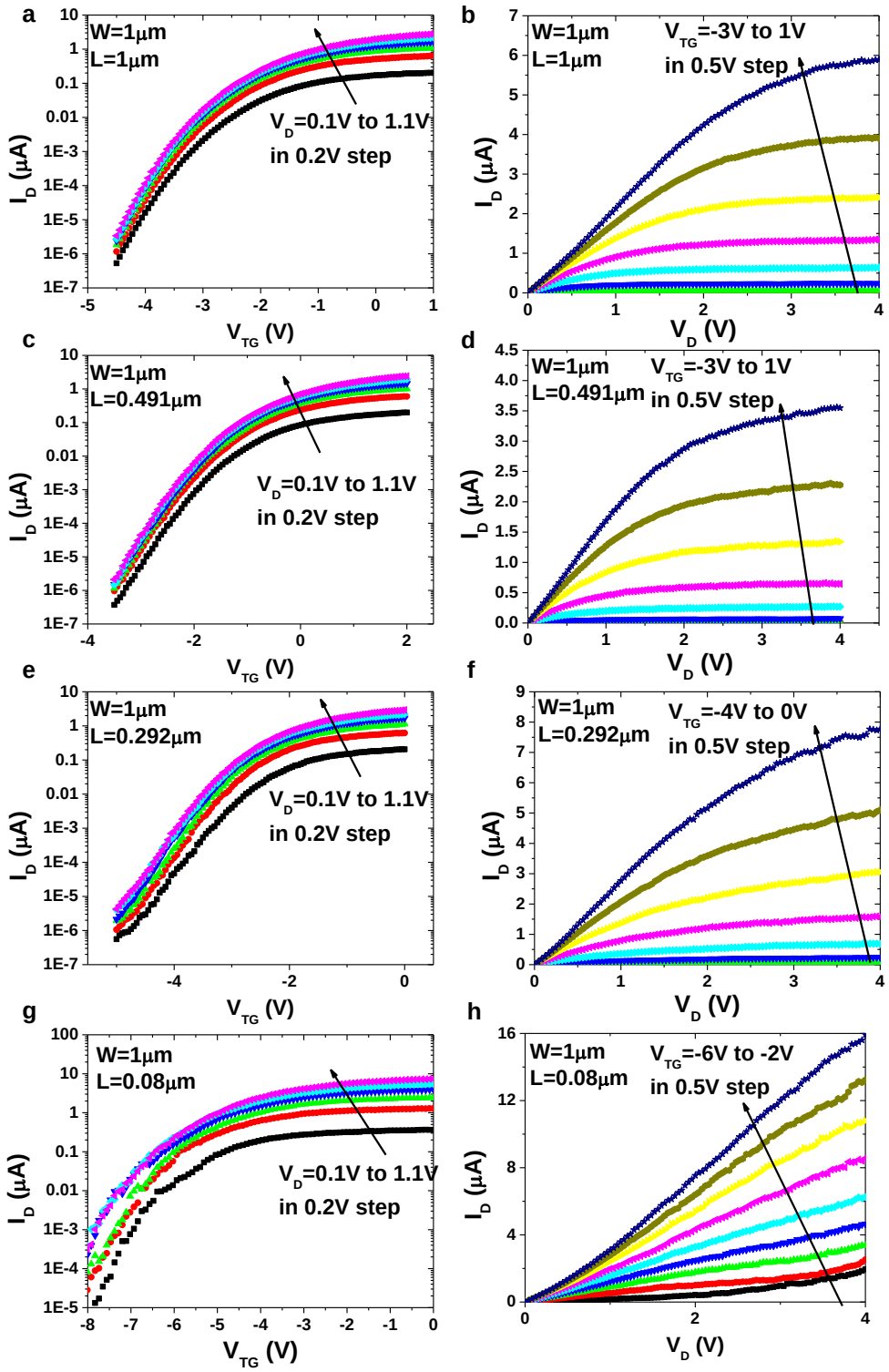
Supplementary Figure 1. Raman spectrum of CVD MoS_2 on SiO_2/Si substrate.



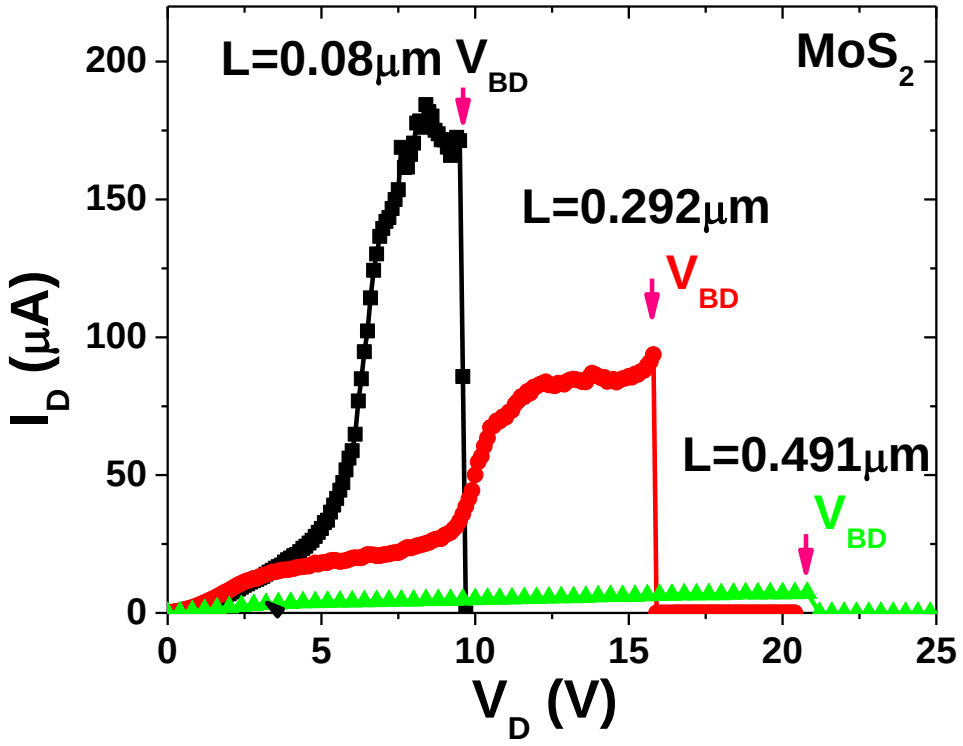
Supplementary Figure 2. The configuration of the gate-to-channel capacitance measurement on MoS_2 Hall-bar devices.



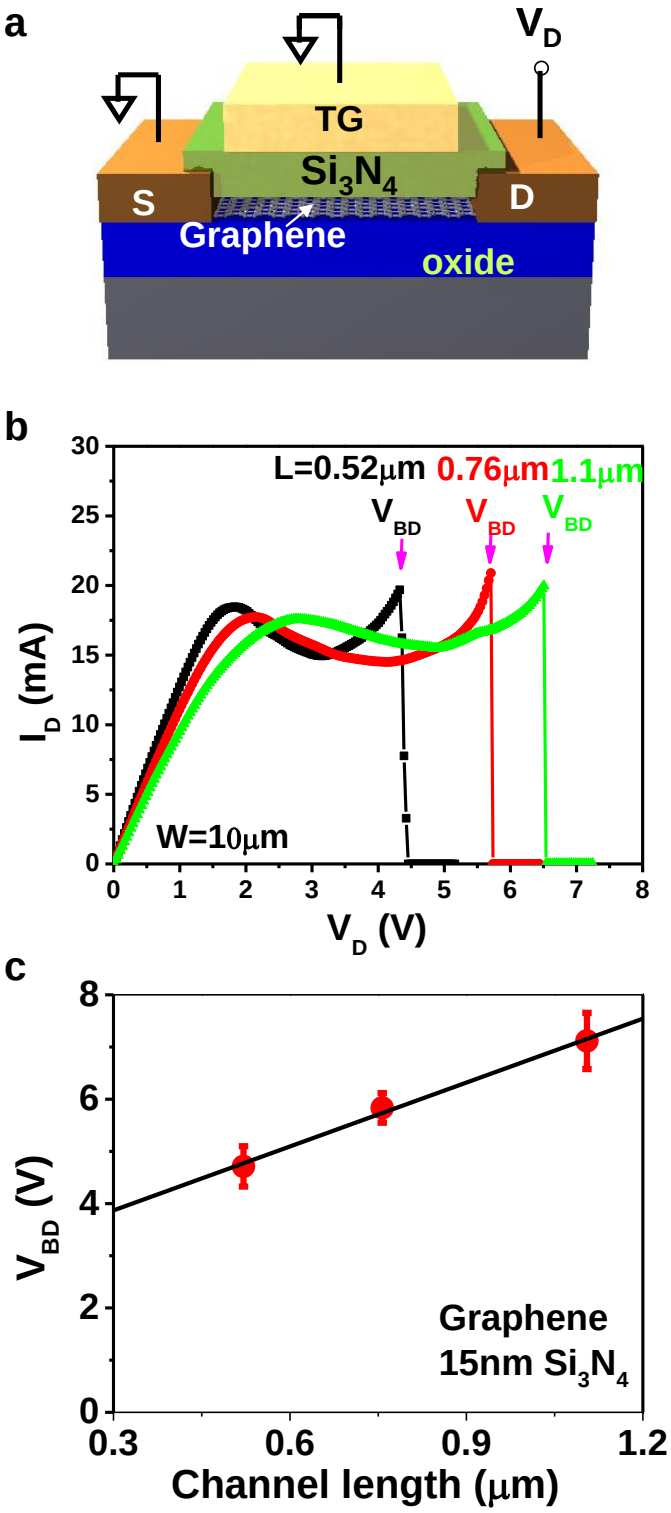
Supplementary Figure 3. Alternating (AC) resistance of MoS_2 Hall-bar structure measured in series mode at various frequencies.



Supplementary Figure 4. Direct current (DC) performance of MoS_2 transistors. (a),(c),(e) and (g) are drain current I_D vs gate voltage V_{TG} characteristics, and (b),(d),(f) and (h) are drain current I_D vs drain voltage V_D characteristics of MoS_2 transistors. The gate lengths are 1μm in (a) and (b), 0.491μm in (c) and (d), 0.292μm in (e) and (f), 0.08μm in (g) and (h), respectively. The drain current as a function gate voltage was measured at various drain voltages from 0.1V to 1.1V.



Supplementary Figure 5. Drain current as a function of drain voltage for MoS_2 transistor with various gate lengths.



Supplementary Figure 6. Critical electrical field measurements on graphene MOSFETs. (a) Schematic of graphene MOSFET with silicon nitride gate dielectrics for breakdown field measurement. (b) Drain current as a function of drain voltage for graphene transistor with various gate lengths. (c) Lateral breakdown voltage as a function of gate length. The symbols are measurement results and the line is the fitting.

Supplementary Notes:

Supplementary Note 1

Extraction method for AC conductance

The ac conductance G_p can be extracted from the measured capacitance and resistance. The parallel circult model is shown in Fig. 2b. Compare to the measurement circuit model shown in Fig. 2b, we can derive that:

$$G_p = \mathrm{Re}\{[R_{ms} - r_s + (i\omega C_{ms})^{-1} - (i\omega C_{ox})^{-1}]^{-1}\}$$

where C_{ms} and R_{ms} are the measured capacitance and resistance in series mode, r_s is the device series resistance and C_{ox} is the oxide capacitance. The serise resistance r_s can be estimated from the measured resistance at accumulation, since at this bias the accumulation layer capacitance C_s is very large, shunting the admittance of the traps. The gate capacitance C_{ox} can be extracted from the capacitance at accumulation C_{ms_acc}:

$$C_{ox} = (C_{ms\_acc}^{-1} - C_{qm}^{-1})^{-1}$$

where C_{qm} is the quantum capacitance of the MoS_2, which can be calcualted based on the density-of-state of MoS_2.

Supplementary Note 2

Breakown voltage in MoS_2

The lateral breakdown voltage in MoS_2 is tested by apply high drain voltage on MoS_2 MOSFET. Supplementary Fig. S5 shows the drain current as a function of drian voltage for MoS_2 MOSFET with various gate length 0.08μm, 0.292μm and 0.491μm. The top gate dielectric is compose of 2nm aluminum deposited by e-beam and re-oxidized as a seed layer, followed by 30nm HfO_2 deposited by atomic layer deposition (ALD). As the drain voltage increases, the drain current first increase, then at a critical voltage, the measured current drops precipitously, indicating the breakdown of the device. The longer the channel, the higher the breakdown voltage. From the slope of breakdown voltage vs gate length, we can extract the breakdown field, shown in inset of Fig. 5b.

Supplementary Note 3

Graphene breakdown field

The device structure and measurement configuration for graphene MOSFET are shown in Supplementary Fig. S6a. The graphene is grown by chemical vapor deposition and the gate dielectric is 15nm silicon nitride. The drain current as a function of drain voltage for graphene transistors with various gate length are shown in Supplementary Fig. S6b. The drain current first increases with drain voltage, reaches a local maximum, then decreases to a local minimum and increases again. This negative differential resistance effect was previously observed in graphene transistors and was attrinuted to drain voltage induced charge neutrality region in the graphene channel [63-65]. When the drain voltage increases further, the drain current drop steeply to zero, indicating device breakdown. The breakdown current density is about 2mA/um. Assuming the van der Waals thickness of 0.335 nm as sheet thickness of graphene, this corresponds to a current density of $6x10^8 A/cm^2$. This is consistent with previous reports [66-68]. The breakdown voltage as a fucntion of gate length is plotted in Supplementary Fig. S6c. The breakdown field is extracted from the slope of the plot. The extracted breakdown field in graphene is compared with the breakdown field in MoS_2, shown in Fig. 5b.

Supplementary References:

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