# A 1V Printed Organic DRAM Cell Based on Ion-Gel Gated Transistors with a Sub-10nW-per-Cell Refresh Power

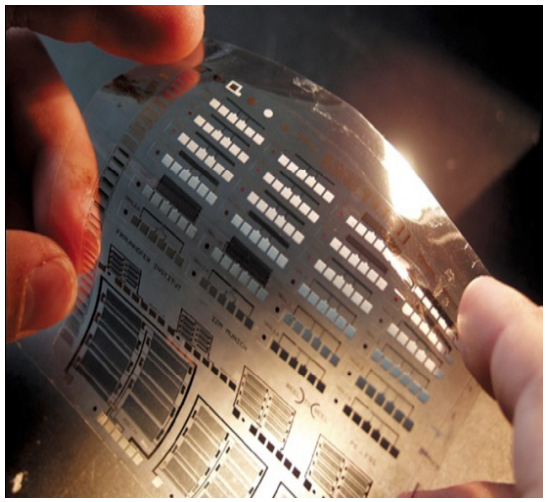
Wei Zhang, Mingjing Ha, Daniele Braga,
Michael J. Renn*, C. Daniel Frisbie, Chris H. Kim

University of Minnesota, Minneapolis, MN
*Optomec, St. Paul, MN

# Agenda

- Motivation
- Previous Organic Memory Research
- Electrolyte Gated Organic TFT with an Unusually High Gate Capacitance
- Proposed 3T DRAM Array Design
- 1V 8x8 Printed DRAM Measurements
- Conclusions

# Organic Electronics



*Flexible circuit*

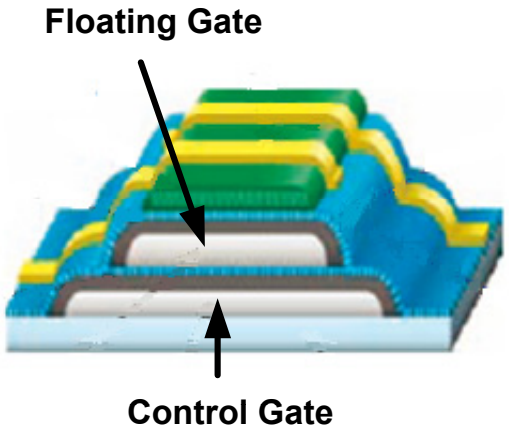
*E-paper*

*Solar Cell*

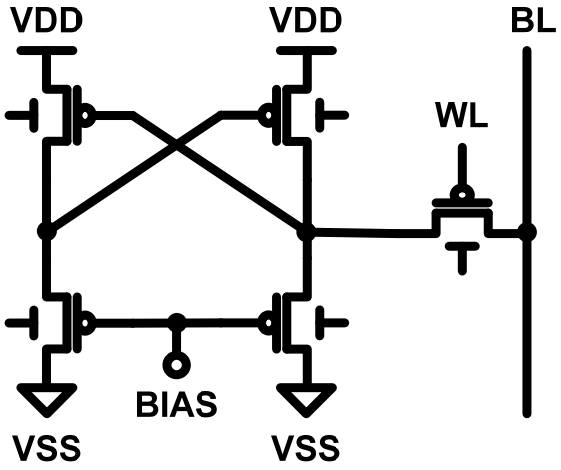
- **Flexible, large area low temperature processing, low cost, printable**
- **Emerging applications: Active display matrix, e-paper, RFID, solar cell, etc**
- **Memory: Key component in flexible applications**

# Previous Organic Memory Reseach

- **Non-volatile memory**
  - **Floating-gate structure**
  - **Ferroelectric materials**
  - **Fuse-based**
- **Volatile memory**
  - **Write-only SRAM (JSSC07)**
    - **Braille sheet display**
    - **Static power problem**
  - **No previous work on general purpose DRAM**

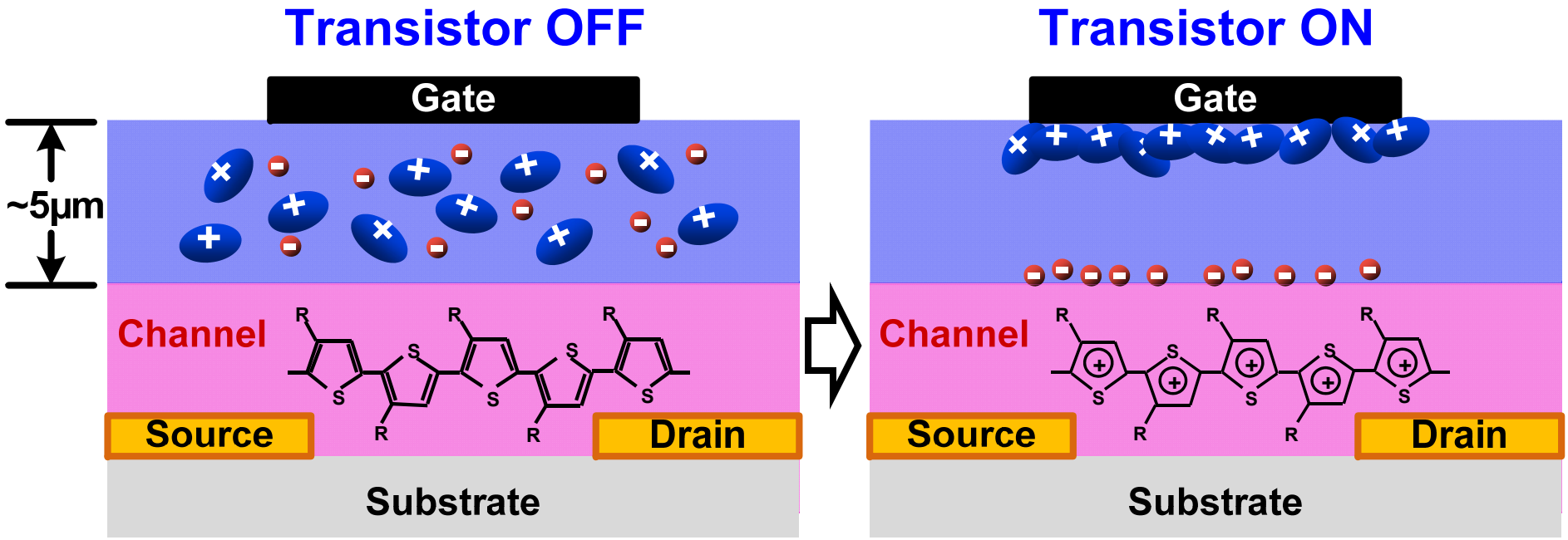



*T. Sekitani, Science 2009*




*M. Takamiya, JSSC 2007*

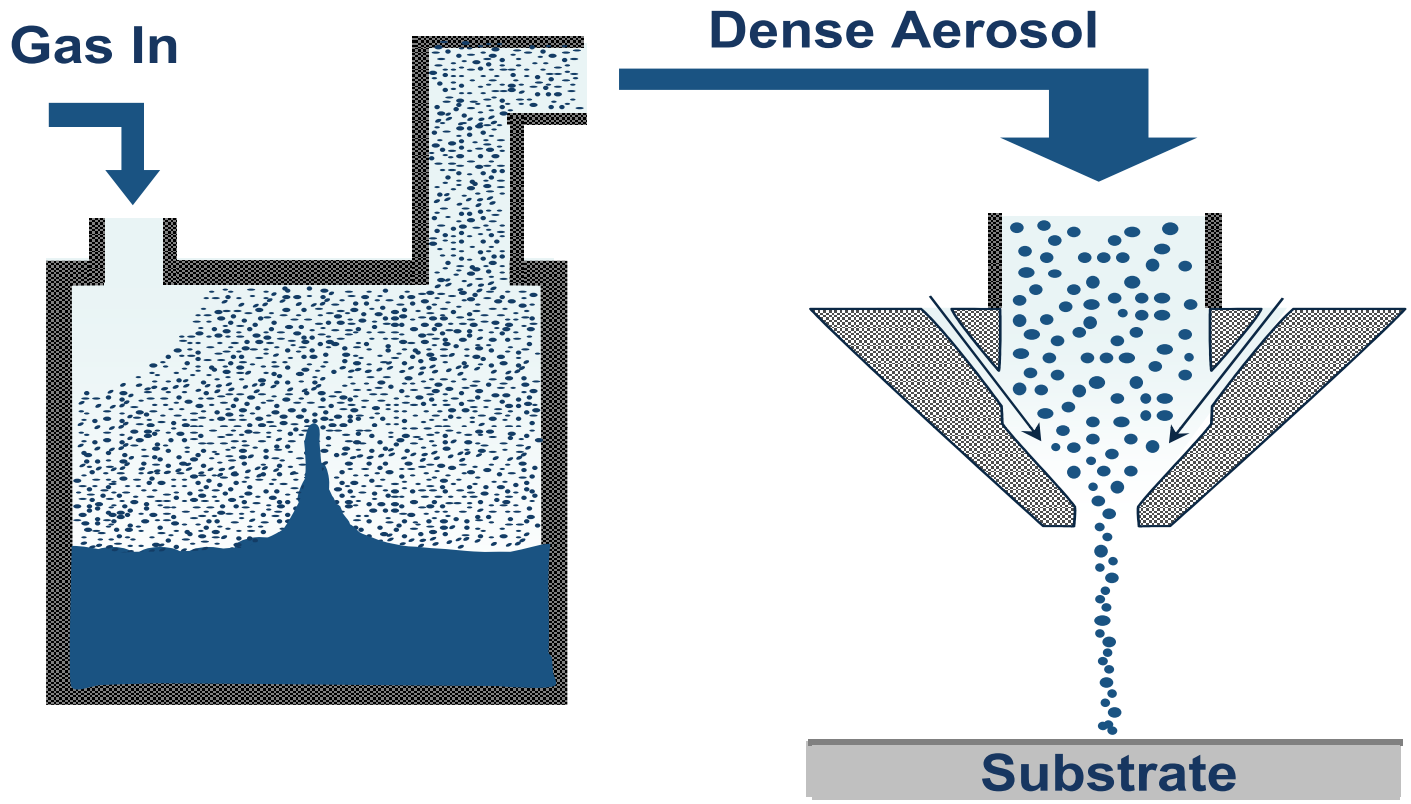
# Electrolyte Gated OTFT with an Unusually High Gate Capacitance




- Polarized ions enable $C_{gate}$=10~100μF/cm$^2$
  - High gate capacitance ideal for DRAM cells
  - 65nm LP CMOS: $C_{gate}$~1.4μF/cm$^2$

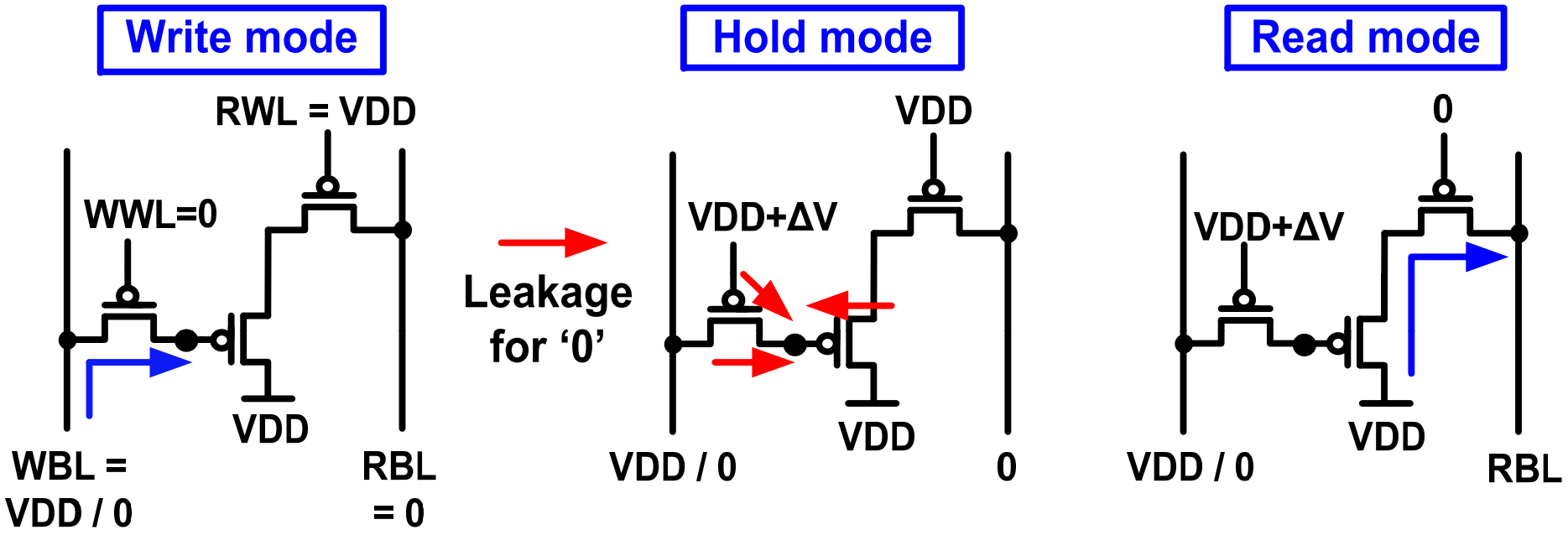
[3] Y. Xia, et al., Adv. Func. Mater., 2010

# Aerosol Jet Printing Method




- Ultrasonic atomizer: aerosol generation
- Output nozzle produces small droplets (1-5 µm)
  - Sub-5 µm line width printing capability

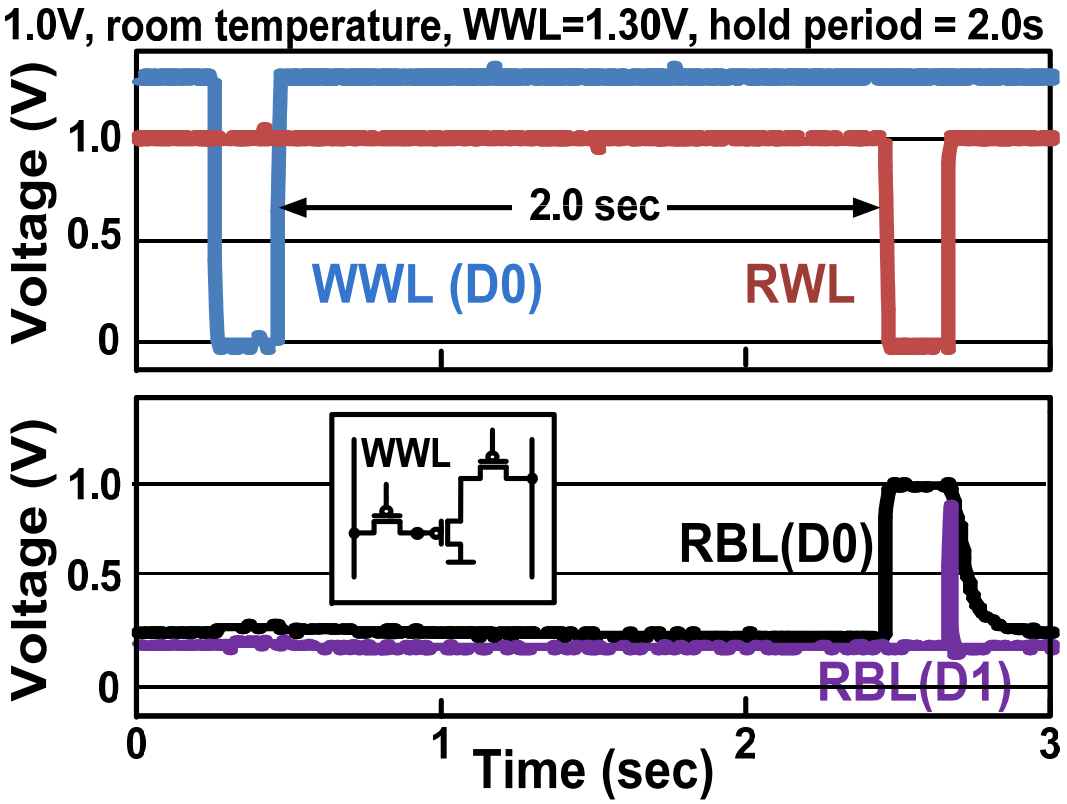
# P-type Only 3T DRAM Gain Cell

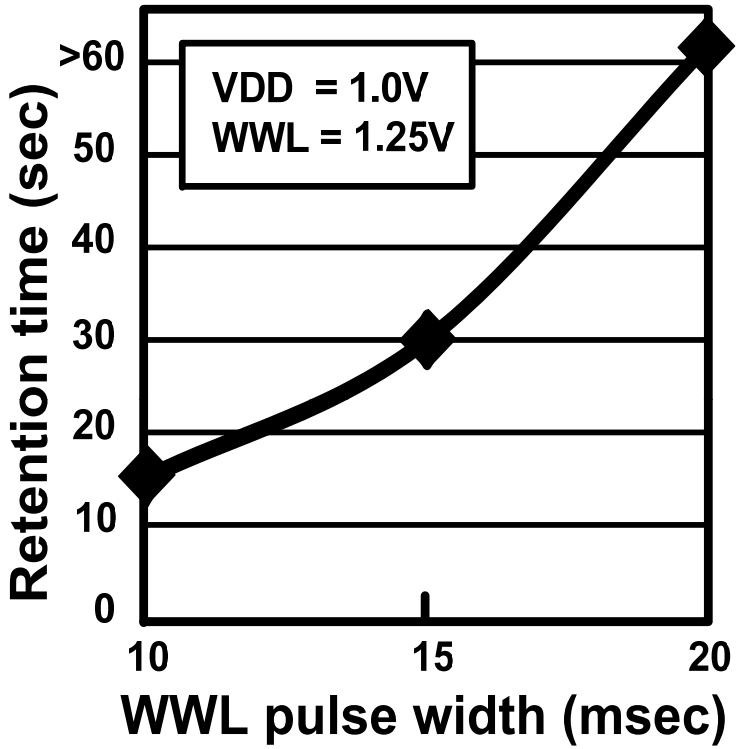



- **Ideal memory cell for electrolyte gated OTFTs**
  - **Long retention time (> 1 minute), compared to 65nm CMOS (~100µs [4])**
  - **P-type only implementation possible, no static power**

**[4] K. Chun, et al., VLSI symp., 2009**

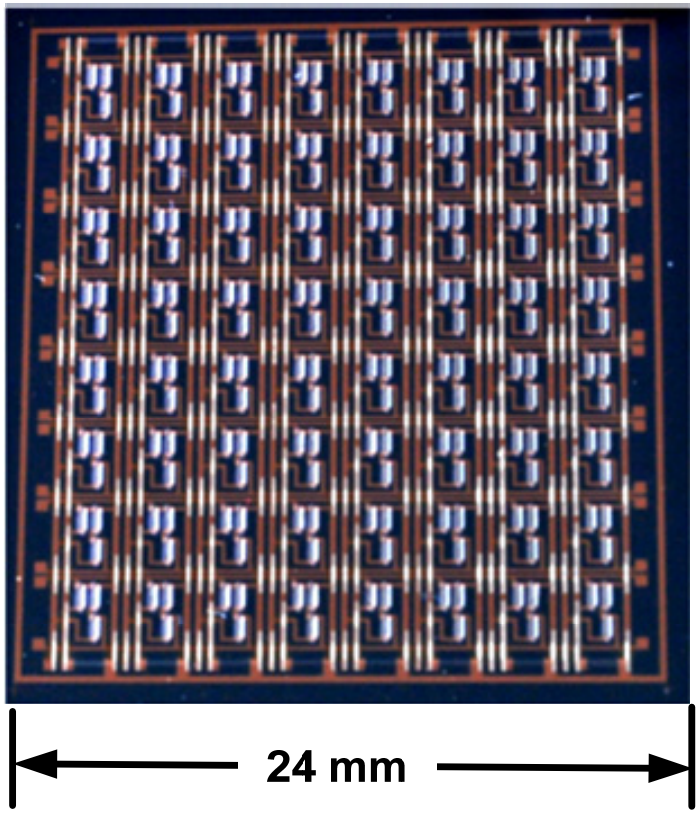
# DRAM Cell Measurement




- **Verified full read and write functionality**
  - **Required WL pulse width: 20 ms (write), 12 ms (read)**
  - **Operating voltage range: 0.8V – 1.2V**

# 8x8 Printed Organic DRAM Array

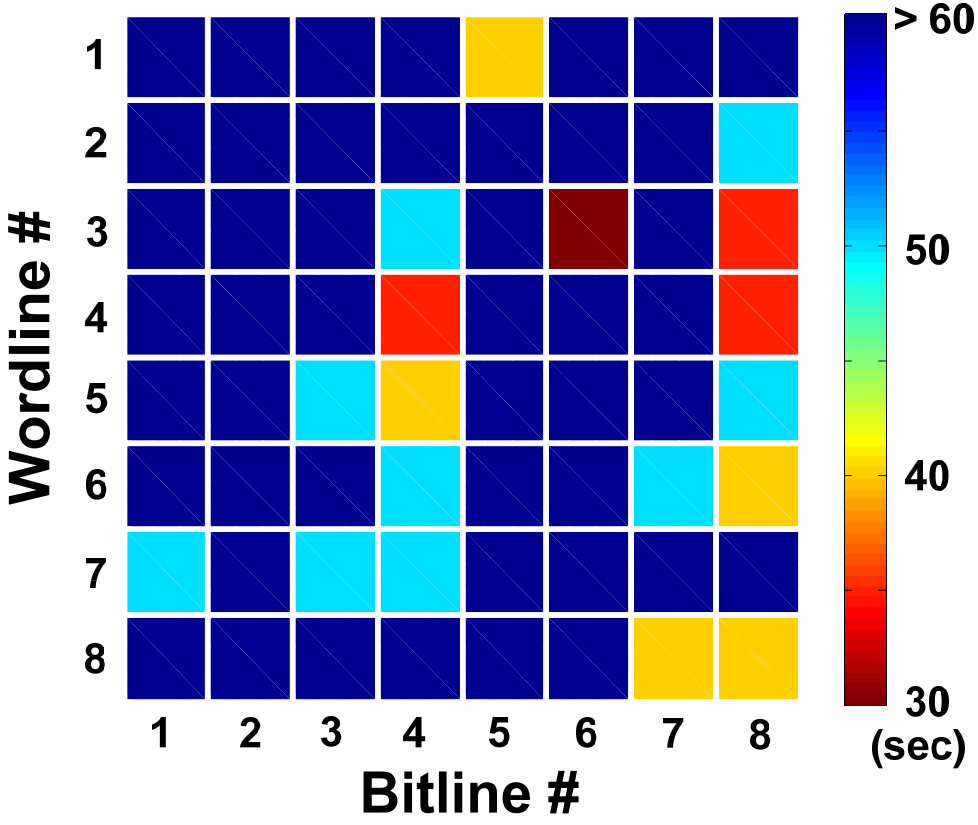


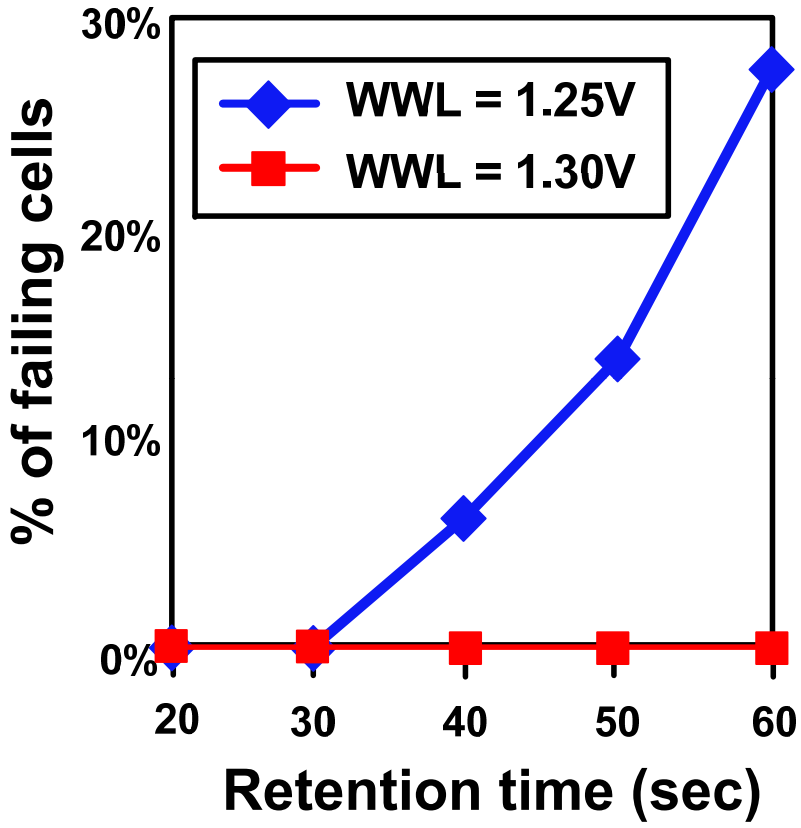

Photograph of Printed Organic DRAM Array

| Process | Ion-gel organic TFT |
|---|---|
| Channel | Poly(3-Hexylthiophene) |
| TR dim. | W/L = 500µm / 25µm |
| Array dim | 24 x 25 $mm^2$ |
| Array size | 64 bits (8 WLs, 8 BLs) |
| Read delay | < 12 msec |
| Write delay | < 20 msec |
| Supply | 0.8V - 1.2V |
| $T_{RETENTION}$ | > 60sec @ 1.30V WWL |
| $P_{ACTIVE}$ | 8 µW/bit |
| $P_{STANDBY}$ | 5.5 nW/bit |

- **Custom IC design flow adopted for OTFTs**

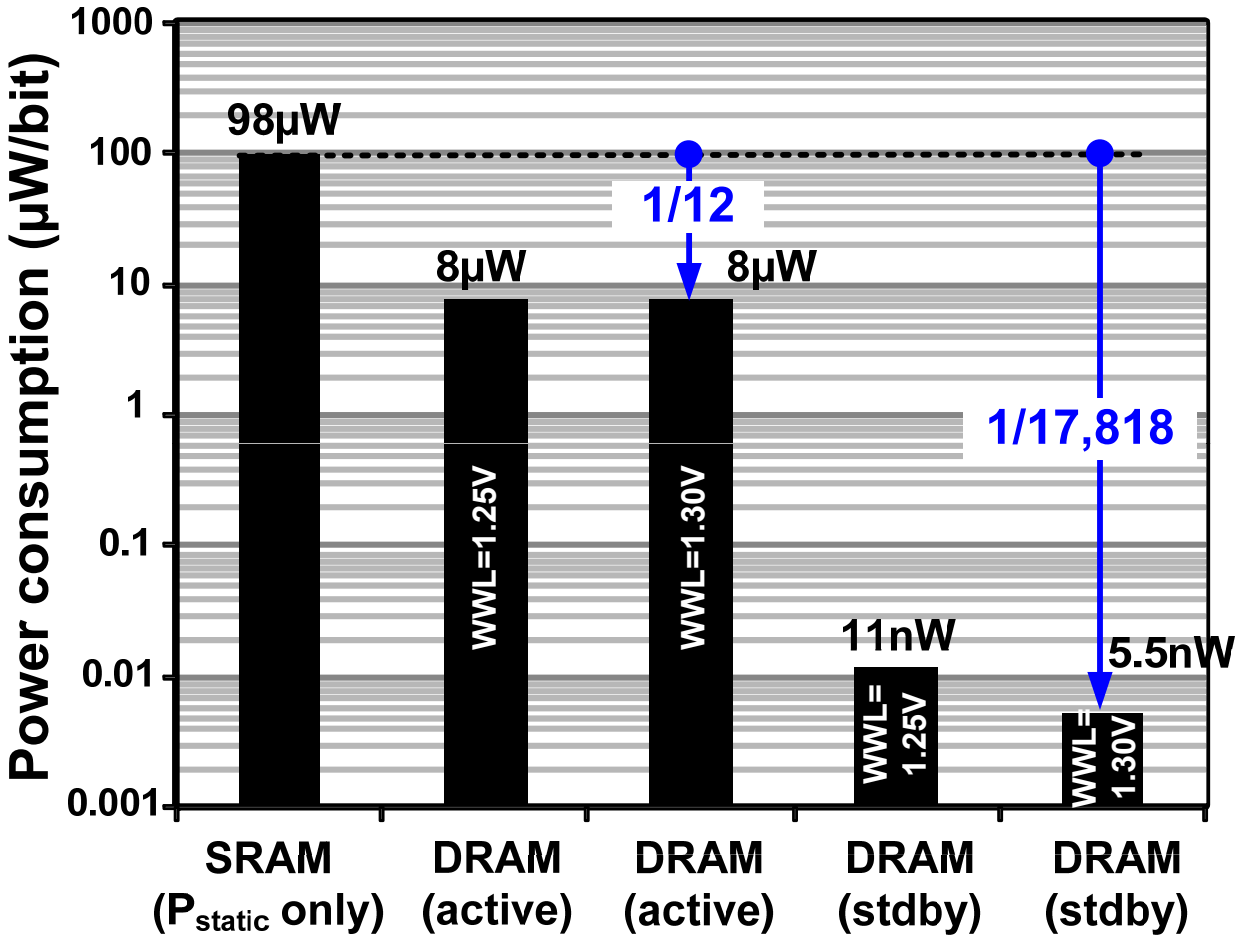
# Array Retention Time Measurements

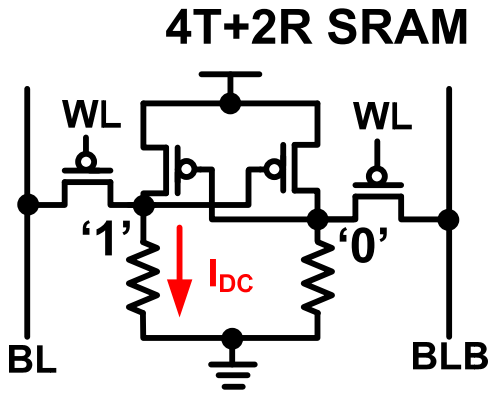


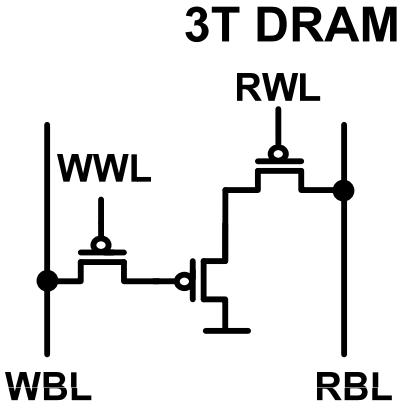




- Worst case retention time: 30 sec for WWL=1.25V
- Retention time over 1 minute for WWL=1.30V

# Power Consumption Comparison

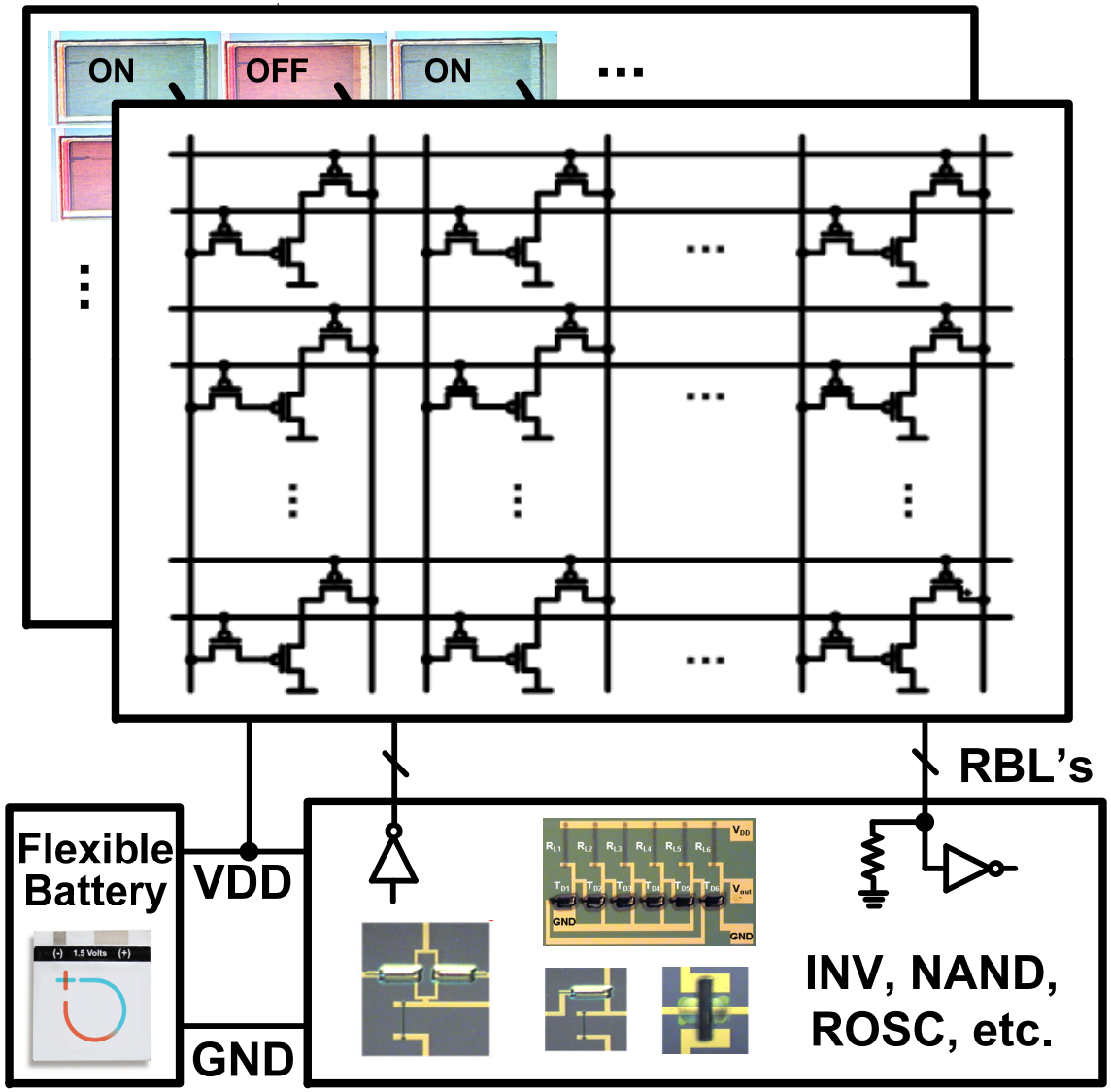



- 12X+ power savings in active mode
- < 10nW/bit refresh power in retention mode

# Proposed General Purpose DRAM Array for Display/Sensor Applications




- Low voltage, low power
- Random access
- Compatible with existing OTFT logic circuits [3]

[3] Y. Xia, et al., Adv. Func. Mater., 2010

# Conclusions

- An 8x8 printed organic DRAM array demonstrated for the first time
  - Retention time > 1min, refresh power < 10nW/b
  - 12X power reduction over SRAM in active mode
  - Cell operation: 50Hz
  - VDD down to 0.8V
- Future work
  - Periphery circuit design
  - Integration with displays or sensors