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Printed Sub-2 V Gel-Electrolyte-Gated Polymer Transistors and Circuits

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The fabrication and characterization of printed ion-gel-gated poly(3-hexylthiophene) (P3HT) transistors and integrated circuits is reported, with emphasis on demonstrating both function and performance at supply voltages below 2 V. The key to achieving fast sub-2 V operation is an unusual gel electrolyte based on an ionic liquid and a gelating block copolymer. This gel electrolyte serves as the gate dielectric and has both a short polarization response time (<1 ms) and a large specific capacitance (>10 μF cm^{-2}), which leads simultaneously to high output conductance (>2 mS mm^{-1}), low threshold voltage (<1 V) and high inverter switching frequencies (1–10 kHz). Aerosol-jet-printed inverters, ring oscillators, NAND gates, and flip-flop circuits are demonstrated. The five-stage ring oscillator operates at frequencies up to 150 Hz, corresponding to a propagation delay of 0.7 ms per stage. These printed gel electrolyte gated circuits compare favorably with other reported printed circuits that often require much larger operating voltages. Materials factors influencing the performance of the devices are discussed.

1. Introduction

The integration of electronics onto flexible plastic or metal foils and paper will greatly expand the application space for microelectronics and engender a range of new products such as large area, distributed sensor arrays, time-temperature smart labels, programmable drug-delivery patches, and roll-up displays.[1] One strategy (there are others) for producing flexible circuitry is to employ traditional printing methods, such as screen, flexographic, gravure, or ink jet printing, to pattern metallic, semiconducting, and insulating materials onto plastic, paper, or metal substrates.[2–12] This in turn requires the development of compatible liquid inks that yield functional materials with good electrical performance in devices. Particular challenges for printed electronics include achieving circuits with sufficient operating speed and stability. It is also desirable for printed circuits to operate at low voltages and low currents to conserve power that will be supplied by thin film batteries, external radio frequency fields, or energy harvesting schemes.[13]

In this paper, we report the fabrication and characterization of low voltage, printed polymer transistors and circuits that employ a novel high capacitance gel electrolyte as the gate insulator. The gel electrolyte, a so-called ion gel, comprises a room temperature ionic liquid, such as 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]), and a gelating triblock copolymer, typically poly(styrene-*b*-methylmethacrylate-*b*-styrene) (PS-PMMA-PS).[14] The block copolymer self-assembles into a physically crosslinked network within the ionic liquid, imparting mechanical strength to the composite gel. The capacitance of the gel exceeds 10 μF cm^{-2}, deriving from the motion of the organic ions within the composite upon application of a gate voltage.[15]

The principal advantages of using ion gels for printed electronics applications stem from their very large specific capacitance. When applied as gate dielectrics in organic thin film transistors (OTFTs), high capacitance ion gels enable substantial reduction in the applied gate voltages required to switch the OTFTs and simultaneously they provide very high source-to-drain conductances and ON currents. For example, applying 1 V on the gate of an ion-gel-gated OTFT (a so-called gel-OTFT) induces approximately 50 times greater charge (and even more current because of a mobility enhancement effect[16]) than 40 V applied to an OTFT with the same channel dimensions but with a 500-nm-thick standard polymer dielectric layer.[2] The low voltage aspect is desirable from a power consumption perspective, as mentioned above, and it simplifies circuit layouts that will be powered by thin film batteries, that is, multiple batteries do not have to be wired in series nor does one have to build charge-pumps or other schemes to boost the battery supply voltage, which is typically 1–2 V. In

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addition, the high device transconductances can be employed to shrink the device footprint in cases where large currents are not needed or to facilitate applications where substantial drive currents are required (e.g., iontophoresis in drug delivery patches).

The large specific capacitance of ion gels may also be useful for the fabrication of printed capacitors for displays or for energy storage and memory devices.[17] Finally, the large specific capacitance of the ion gel is essentially independent of its thickness (though the polarization time is not), meaning that relatively thick (1–10 μm) layers of the gel can be deposited. This is clearly a processing advantage, as thickness control in the sub-100 nm regime across a flexible moving web, as would be required for roll-to-roll processing of printed circuits, may be challenging.

It is important to note that any electrolyte can provide high specific capacitances and a number of groups have reported transistors gated with different solid polymer and liquid electrolytes;[18–23] the bulk of the early work derives from the 1980s.[24–26] Distinguishing characteristics of the rubbery ion gels employed here are that they have very large ionic conductivity (10^{-3}–10^{-2} S cm^{-1}), small (sub-ms) polarization time, and a wide electrochemical window (±3 V).[14,27,28] They are also chemically inert, optically transparent, and thermally very stable (>200 °C). From room temperature to approximately 100 °C they exhibit an elastic modulus in the range of 1–10 kPa, depending on polymer content.[14]

There are some disadvantages of using electrolytes as gate dielectrics. First, there are materials compatibility issues. Only expensive noble metals (e.g., Au, Pd, Pt) or less expensive, electrochemically stable carbon-based conductors can be used as source, drain, and gate electrodes. This is because electropositive metals such as Ag or Cu can be oxidized easily (e.g., $Ag -> Ag^{+} + e^{-}$) when in contact with an electrolyte at positive biases; this will lead to high OFF currents and device degradation. In addition, the semiconductor must also be stable to the electrolyte upon repeated switching. This is less of a problem than the metals compatibility, though, as many polymer semiconductors are stable upon electrochemical oxidation.

Second, the polarization response time of the electrolyte will be the ultimate speed limiting factor. Application of a gate bias requires that ions move to the gate-electrolyte and semiconductor-electrolyte interfaces to establish electrical double layers. The timescale for this process depends on the resistance of the electrolyte (R) and the interfacial capacitance (C), that is, the RC time constant. Using a typical ionic liquid resistivity of $10^{3}\ \Omega \cdot$ cm, a thickness of 1 μm, and specific capacitance of 10 μF cm^{-2},[15,29] we estimate that minimum electrical double layer formation times are on the order of 1 μs, meaning that one cannot expect to switch electrolyte-gated transistors faster than 1 MHz, but this may be adequate for many envisioned applications.

A third issue is that while for some applications low voltage operation is desirable, for others, such as display drivers, higher voltages are necessary. The inherent voltage stability window of the electrolyte (up to ±3 V for ion gels) will set limits on the maximum operating voltage of electrolyte-gated TFTs, which will disqualify them for some applications. A related consideration is power consumption. While electrolyte-gated OTFTs can switch at very low voltages, the switching currents (gate displacement currents) scale with capacitance. In terms of power consumption, higher currents offset lower voltage operation. It remains to be determined whether truly low power electrolyte-gated circuits can be fabricated.

Finally, it is worth noting that there is to some extent an ingrained bias against applying electrolytes in electronic devices as it is well-accepted in silicon microelectronics that mobile ions are a nuisance, particularly in dielectrics where ionic motion under applied gate biases can lead to undesirable effects, such as threshold voltage shifts. Such effects, however, may not be problematic when using highly conductive electrolytes. The application of electrolytes in super-capacitors and batteries demonstrates that these materials can perform stably and reversibly. Ultimately, the application of electrolytes in printed electronics will rest on finding applications where high capacitance, low voltage operation, and processability are of paramount importance, and the disadvantages described above can be tolerated or effectively managed.

Here we have substantially expanded upon our initial work in which we demonstrated that ion gels are printable and can be incorporated into discrete polymer transistors.[29] Specifically, we describe for the first time the fabrication and characterization of a variety of low voltage, printed gel-OTFT circuits that can serve as building blocks for more complex functions. These circuits include a tunable transistor-loaded inverter, a 5-stage ring oscillator, a NAND gate, and a *D* flip-flop. To our knowledge, integration of electrolyte-gated transistors at the level of a flip-flop circuit has not been reported before. We also demonstrate that gel-OTFTs can be fabricated with source, drain, and gate electrodes composed of the conducting polymer poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) instead of Au, which is important from a cost perspective. Finally, we show that the geometrical scaling (channel width and length) of both the output current and the switching speed of gel-OTFTs is predictable and largely consistent with expectations for conventional TFTs, greatly facilitating the modeling of these devices by commercially available software. Collectively, these results establish that functional sub-2 V circuitry based on electrolyte-gated polymer TFTs can be fabricated using a printing process and liquid-based inks. Reproducible circuit behavior and predictive modeling enhance opportunities for the incorporation of electrolyte-gated OTFTs in flexible electronics applications where low voltages and high transconductances are a distinct advantage.

2. All-Organic, All-Printed Gel-OTFTs

Conductive metal inks based on Au and Ag nanoparticles have been widely employed in demonstrations of printed circuitry, primarily due to their low resistivity.[30–34] However, Au inks are relatively expensive. In addition, for the electrolyte-gated devices discussed here, Ag is not a viable option for the source, drain, and gate electrodes because it is an electropositive metal. Under positive bias, Ag electrodes and other non-noble metals (e.g., Al, Cu) can dissolve in the electrolyte. Furthermore, nanoparticle inks commonly require a long post-annealing period under elevated temperatures that may not be compatible with some types of substrates. These factors have lead us to consider the use of a low cost and easily processable conductive ink composed of 90% PEDOT:PSS (1–1.4 wt% polymer in water) and 10% ethylene glycol for all conductive electrodes. This PEDOT:PSS ink was deposited

with a typical thickness of 40 nm using a commercial aerosol jet printing technique.[29] The measured conductivity of the printed electrodes was as high as 500 S cm^{-1} with no post-annealing requirement. The strategy of adding ethylene glycol or other chemicals to increase the conductivity of PEDOT:PSS has been reported previously by Sholin et al. and others.[35,36]

Four-layer all-organic OTFTs (Fig. 1a) were fabricated by sequential printing of PEDOT:PSS, poly(3-hexylthiophene) (P3HT), the ion gel, and PEDOT:PSS again to form the source/drain electrodes, semiconductor channel, gate dielectric, and gate electrode, respectively. We used aerosol jet printing for all layers, as described previously.[29] Figure 1b shows an array of 30 semitransparent all-organic transistors printed on a flexible poly(ethylene naphthalate) (PEN) substrate with all the functional layers overlaid with good registration. Note that in each device the PEDOT:PSS gate electrode was printed over the ≈10-μm-thick ion gel step (i.e., the electrode was extended from the top of the ion gel layer to the substrate) while maintaining good electrical conductivity. The ion gel ink was composed of a mixture of the ionic liquid [EMIM][TFSI] and the PS-PMMA-PS block copolymer dissolved in ethyl acetate. Upon drying of the solvent, the gel formed spontaneously.

As sketched in Figure 1a, when a negative gate voltage is applied with respect to the grounded source, the positive $[EMIM]^+$ ions and the negative $[TFSI]^-$ ions are subsequently driven towards the gate-ion gel and semiconductor-ion gel interfaces, respectively. The strong polarization of the dielectric leads to extremely high specific capacitance (>10 μF cm^{-2}) and low voltage device operation. We have previously established that anions from the gel can penetrate the polymer such that the channel formation process can be electrochemical in nature.[15] This process is reversible, which allows the device to be switched ON and OFF repeatedly.

The typical transfer characteristic (channel current vs. gate voltage, I_D–V_G) of an all-organic, all-printed ion-gel-gated OTFT is plotted in Figure 1c, which was acquired with a drain-source voltage (V_D) of −1 V and a gate voltage (V_G) sweep rate of 50 mV s^{-1}. The transistor turned on near 0 V, with a sub-threshold swing of ≈200 mV per decade. The channel current increased five orders of magnitude by $V_G = -1$ V, reflecting a significant increase in charge carrier density in the channel. Such transfer characteristics are comparable to those we reported previously for printed ion-gel-gated P3HT transistors, where source and drain electrodes were printed using Au nanoparticle ink.[29] This observation is in agreement with previous work that demonstrated the conductivity of PEDOT:PSS ink is high enough to serve as the conductive layer in OTFTs.[35] The fact that we observed low OFF-current (10^{-8} A) and negligible current hysteresis between forward and reverse V_G sweeps (Fig. 1a) also suggests that the PEDOT:PSS electrodes are compatible with the ion gel material. We note that OTFTs with PEDOT:PSS electrodes have been reported before,[35–37] but not in conjunction with the ion gel dielectric.

We have constructed an all-organic inverter, a basic circuit building block, by connecting the gel-OTFT described above in series with a 20 kΩ printed PEDOT:PSS-based resistor. The circuit diagram and input-output voltage characteristics (V_{IN}–V_{OUT}) are plotted in Figure 1d. It is clear that the output voltage switched from the "0" state (−1.5 V) to the "1" state (0 V) when the input signal was swept from "1" to "0," and vice versa. The switching took place near $V_{IN} = 0$ V and the inverter was completely switched within only 0.5 V of V_{IN} variation, with a maximum gain (dV_{IN}/dV_{OUT}) as high as 7 (Fig. 1d, inset). No output hysteresis was observed between the forward (inverter switched to "1") and reverse (inverter switched to "0") V_{IN} sweeps, indicating reliable low-voltage switching behavior.

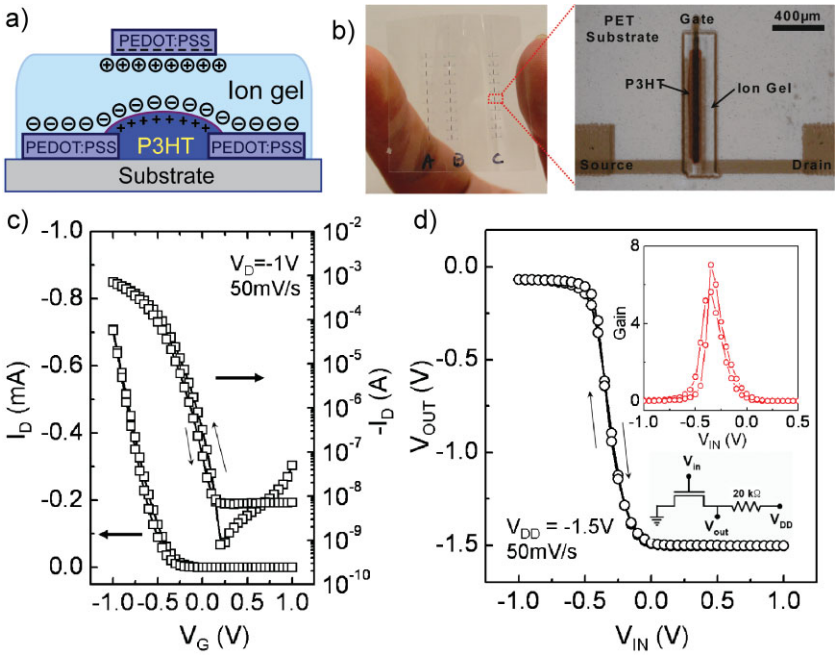

Figure 1. All-organic all-printed gel-OTFTs. a) Scheme of an all-printed ion-gel-gated P3HT transistor with PEDOT:PSS electrodes. b) Optical image of a 30 transistor array printed on a plastic (PEN) substrate. The right image shows a magnified single transistor, where all the functional layers can be clearly distinguished. c) I_D–V_G characteristics of a typical gel-OTFT with PEDOT:PSS electrodes. $L = 50$ μm, $W = 500$ μm. d) Characteristics of an all-organic ion-gel-gated inverter. The lower inset shows the circuit diagram and the upper right inset shows the gain of this inverter.

3. Geometric Scaling of Output Current and Response Time of Gel-OTFTs

To verify the quality of the aerosol jet printing process we employed, as well as the function of the devices, we characterized transistor performance as a function of channel length (L from 5 μm to 200 μm with $W = 500$ μm) and channel width (W from 20 μm to 500 μm with $L = 20$ μm). The results are summarized in Figure 2. For clarification, the source and drain electrodes and the interconnects for these transistors, as well as for the other devices discussed later, were fabricated using thermally evaporated Au and a standard photolithography lift-off process (on an SiO_2/Si substrate) in order to minimize printing time.

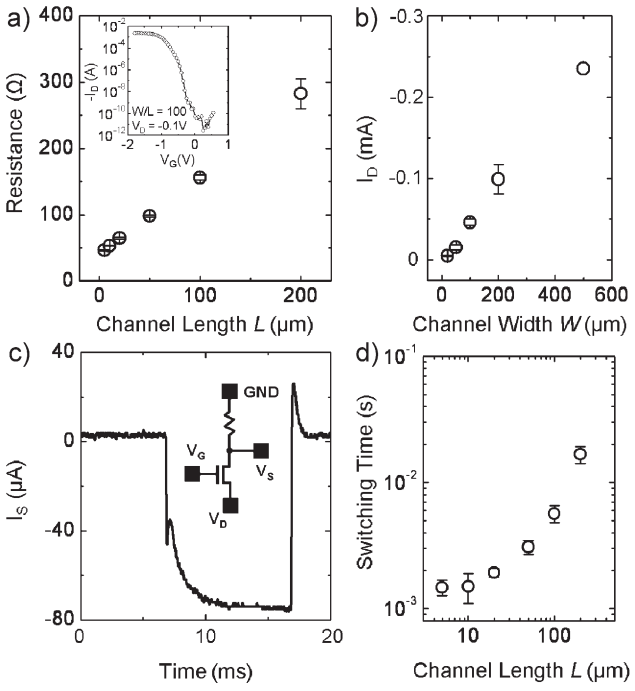

Figure 2. Geometric scaling of printed gel-OTFTs with lift-off Au source and drain electrodes. The substrate was SiO_2/Si. a) Resistance of the transistors as a function of channel length, acquired with $V_G = -1.5$ V and $V_D = -0.1$ V. $W = 500$ μm. The inset shows a typical I_D–V_G characteristic, with ON/OFF current ratio higher than 10^7. b) Drain current as a function of channel width, acquired with $V_G = -0.9$ V and $V_D = -0.2$ V. $L = 50$ μm. c) Current-time response of a resistor-loaded inverter upon stepping V_G from +0.6 V to −1.6 V with $V_D = -0.1$ V. The gel-OTFT had $L = 50$ μm and $W = 500$ μm. The inset shows the inverter scheme. The switching time of the device is defined as the time interval for 90% increase of the current response. d) Switching time of gel-OTFTs as a function of channel length ($W = 500$ μm).

All the other functional layers (semiconductor, gate dielectric, and gate electrode) were deposited by printing. It is noteworthy that, as shown in the typical I_D–V_G characteristic in the inset of Figure 2a, the gel-OTFTs with evaporated Au source/drain electrodes display 100 times smaller OFF current compared to devices with printed electrodes ($<10^{-10}$ A vs. $\approx 10^{-8}$ A for both PEDOT:PSS ink-printed source/drain, Fig. 1c, and Au nanoparticle ink-printed source/drain, Ref. [29]). The lower OFF current can be attributed to the lower surface area and roughness of the lift-off electrodes. The lift-off electrodes have narrower width (10 μm vs. ≈50 μm for the printed electrodes) and smoother surfaces, which reduces the effective contact area with the electrolyte, leading to smaller overlap capacitance and smaller displacement currents (the major source of the OFF current) during gel-OTFT operation. Achieving low overlap capacitance is a challenge for printed electronics because in general printed electrode widths and roughnesses are larger. Yet, we estimate that with proper optimization, ON/OFF current ratios higher than 10^7 can be expected in all-printed gel-OTFTs, similar to what is shown in the Figure 2a inset.

As illustrated in Figure 2a and b, a linear relationship is clearly observed for resistance ($R = V_D/I_D$ at $V_G = -1.5$ V) as a function of L and for I_D as a function of W, demonstrating that the devices behave as expected (where $I_D \propto W/L$)[38] and that the printing process is reproducible over a range of channel dimensions ($L = 5$–200 μm and $W = 20$–500 μm). The intercept of R versus L at $L = 0$ μm indicates that the contact resistance of the devices is approximately 40 Ω at $V_G = -1.5$ V (i.e., when the transistor is ON). This corresponds to a specific contact resistance of 2 Ω · cm, which is an extraordinarily low (typical Au/P3HT contact resistances in OTFTs are ≈1 kΩ · cm).[39] Detailed contact resistance measurements as a function of gate voltage will be described in a later publication.

Switching time (or propagation delay) is one of the most important performance metrics for inverters employed in functional circuits. Previously, we showed resistor-loaded inverters that operated at input frequencies near 1 kHz.[29] Here we have systematically examined the switching time of inverters as a function of channel length (Fig. 2c and d) in order to assess how the devices may be optimized. Our measurement setup was as illustrated in the inset to Figure 2c, where a printed resistor was connected between the source electrode of the gel-OTFT and ground. The resistance values ranged from 1 kΩ to 40 kΩ, that is, they were scaled with the dimensions of the transistor channels such that the load resistance was ≈2 times the channel resistance of the gel-OTFT in the ON-state. During the measurement, the transistor was switched ON and OFF. We obtained the channel current response by measuring the voltage on the source electrode with an oscilloscope and dividing it by the resistance of the load resistor. A drawback of this approach is that it does not accurately simulate the dynamic behavior of an inverter connected to other inverters in a circuit, e.g., the oscilloscope does not have the same input impedance as another gel-OTFT. However, this measurement at least provides a sense of the magnitude of the switching time and how it varies with channel length. We have also employed ring oscillators to measure the propagation delay, as described later, which is a more accurate approach to determining switching time.

As can be seen in the inset of Figure 2c, switching V_G from 0.6 V to −1.6 V resulted in a significant increase in channel current, which stabilized within several ms. The spikes observed in the switching characteristics are caused by the parasitic capacitance effect. We estimated the switching time of gel-OTFTs from the time required for the current to reach 90% of its maximum value, and plotted this time as a function of channel length in Figure 2d. Figure 2d shows that the switching time for gel-OTFTs decreased with decreasing channel length but that below $L = 10$ μm the switching times appeared to asymptote at 1.3 ms.

A spectrum of factors likely limits the response time of the current devices to ≈1 ms. At short channel lengths the switching speed will be limited by the polarization response (RC time constant) of the electrolyte and not by electronic transport in the semiconductor channel.[29] We have measured the thickness of the printed gel layer to be ≈10 μm and thus the specific resistance of the electrolyte is on the order of 10 Ω · cm^2. The specific capacitance of these devices can approach 100 μF cm^{-2}, because ions from the gel electrolyte can penetrate P3HT. Multiplying these two numbers yields $RC = 10^{-3}$ s, consistent with the measured switching time. Indeed, previous measurements of the capacitance-frequency response of 10-μm-thick ion gel layers suggest that above 1 kHz (corresponding to 1 ms switching time) the

capacitance of the gel begins to decrease, indicating that polarization processes (such as ion movement) within the gel are becoming rate limiting.[15]

For channel lengths longer than 10 μm, there is no clear power-law dependence of switching time with channel length. This is likely due to the effects of competing mechanisms such as gel polarization coupled with charge (hole) drift in the channel at longer channel lengths. Similar channel length scaling effects in electrolyte gated transistors have been seen by Sirringhaus and Berggren,[30] and more work is necessary to unravel the various mechanisms that control channel formation in gel-OTFTs. The essential conclusion from the data in Figures 1 and 2, however, is that gel-OTFTs can be printed reproducibly with excellent low voltage performance and the scaling of the device output current with geometry matches expectations.

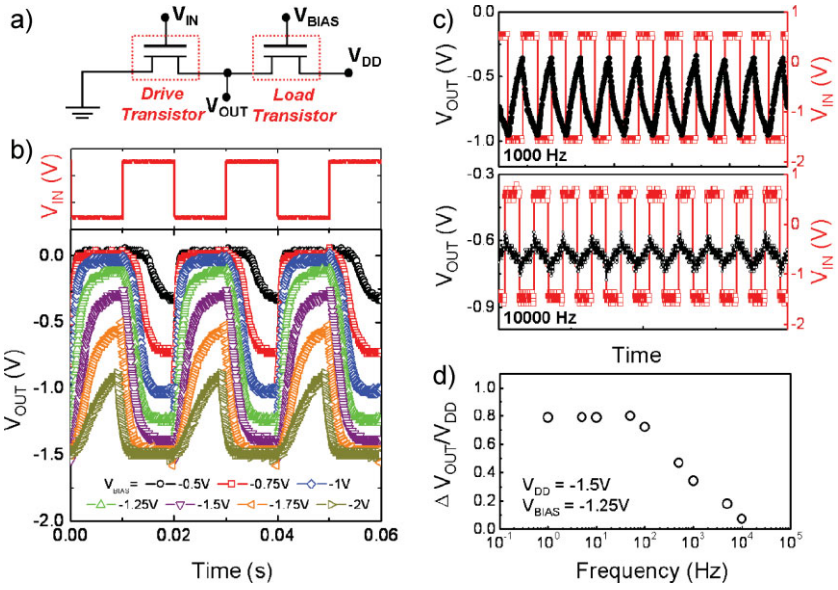

Figure 3. Transistor-loaded gel-OTFT inverter with additional gate bias control. All components of the gel-OTFTs were printed with the exception of Au interconnects and the source and drain electrodes, which were fabricated by photolithography and lift-off. a) Circuit diagram. b) Inverter output characteristics (bottom panel) in response to a 50 Hz square-wave input signal (top panel, switched between 0.5 V and −1.6 V), with $V_{DD} = -1.5$ V and various values of V_{BIAS}. c) Dynamic output response of an optimized inverter to 1 kHz (top) and 10 kHz (bottom) square-wave input signals, respectively. The red squares represent input voltage signals and the black circles represent output voltage responses. d) Inverter output range as a function of frequency. Both c) and d) were acquired with $V_{DD} = -1.5$ V and $V_{BIAS} = -1.25$ V. Drive transistor dimensions: $L = 25$ μm, $W = 500$ μm. Load transistor dimensions: $L = 50$ μm, $W = 100$ μm.

4. Printed Gel-OTFT Circuits

For resistor-loaded inverters just described, the ideal response is realized when the load resistance is twice the channel resistance of the transistor in its ON state (see Supporting Information for the derivation). However, the value of channel resistance varies with the applied gate voltage as well as other non-ideal factors. Therefore, the optimization of resistor-loaded inverters is difficult. Instead, as sketched in the circuit diagram in Figure 3a, we constructed a transistor-loaded inverter by connecting the ion-gel-gated OTFT (the drive transistor) with another OTFT (the load transistor) that had an individual bias control (V_{BIAS}). By tuning the resistance of the load transistor with V_{BIAS}, the output of the inverter can be modified.

Figure 3b illustrates the output voltages of a typical inverter under various V_{BIAS} conditions, acquired with a 50 Hz square-wave input signal (switched between 0.5 V and −1.6 V). At $V_{BIAS} = -0.5$ V, the inverter was easily switched ON but was very difficult to switch OFF, which resulted in a small output range ($\Delta V_{OUT} = V_{OUT,HIGH} - V_{OUT,LOW} = 0.36$ V). The shape of the transient output voltages for ON and OFF switching became more and more balanced with decreasing V_{BIAS} until approximately −1.25 V, where ΔV_{OUT} also reached its maximum ($\Delta V_{OUT} = 1.16$ V). The inverter output characteristics were thereby optimized. Further decreasing of V_{BIAS} resulted in the degradation of inverter response in the opposite sense (i.e., device was easily switched OFF but more

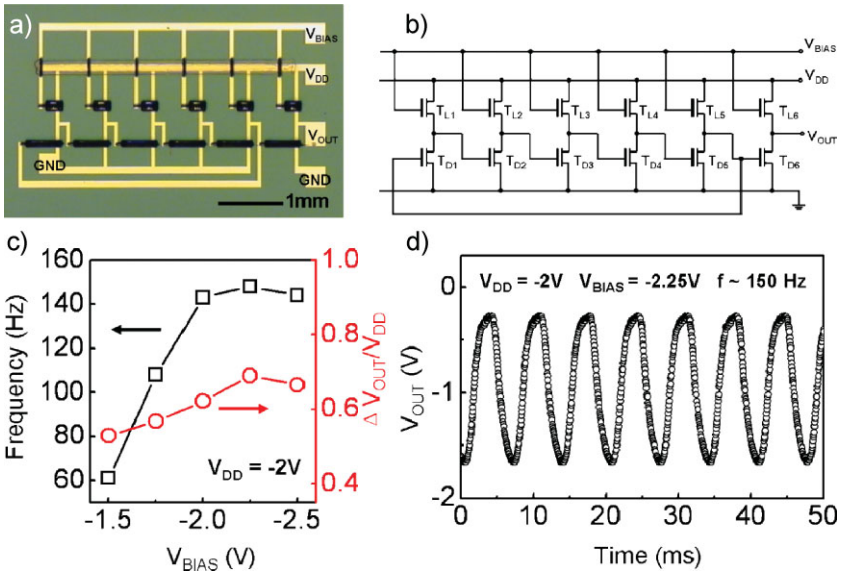

Figure 4. Low-voltage, five-stage ring oscillator. a) Optical image of printed gel-OTFT layout on SiO_2/Si. Au interconnects and supply lines were fabricated by photolithography and lift-off. b) Circuit diagram. c) Frequency and output range of the ring oscillator as a function of load-transistor gate voltage, V_{BIAS}. d) Output characteristics of a typical ring oscillator with oscillation frequency as high as 150 Hz. Drive transistor dimensions: $L = 25$ μm, $W = 500$ μm. Load transistor dimensions: $L = 50$ μm, $W = 100$ μm.

difficult to switch ON, and ΔV_{OUT} was reduced). As demonstrated in Figure 3c, the optimized device showed a clear inverter response to square-wave input signals up to 10 kHz in frequency, equivalent to a minimum switching time of less than 50 μs (count two switches in one period). When operating at 1 kHz, the optimized inverter showed better output characteristics compared to our previous report.[29] Figure 3d shows the output range of the inverter remained constant (≈80% V_{DD}) until 50 Hz, and then gradually decreased with increasing operation frequency. Within 20 ms these inverters could be switched without any signal degradation, which is fast enough for many sensing, actuating and display applications.[4,40,41]

We extended this work by fabricating five-stage ring oscillators using six transistor-loaded inverters. As shown in the device image (Fig. 4a) and circuit diagram (Fig. 4b), the output of the 5th inverter was connected to the input of the 1st inverter (while the 6th inverter served as an output buffer); the output signal started to oscillate when a constant drain supply voltage (V_{DD}) was applied above a critical value, typically near −1 V. Again by controlling V_{BIAS}, as plotted in Figure 4c, we were able to tune the oscillation frequency of the ring oscillator and optimize the output range. Figure 4d displays the output voltage characteristics of our fastest ring oscillator, which was acquired at $V_{DD} = -2$ V and $V_{BIAS} = -2.25$ V. The ring oscillator switched between −0.28 V and −1.66 V ($\Delta V_{OUT} = 1.38$ V) at a frequency of 150 Hz. This corresponds to a propagation delay for each inverter stage of ≈0.7 ms, a similar, but slightly shorter response time than we measured by examining discrete inverters (Fig. 2).

To our knowledge, reports on printed organic ring oscillators are rare,[34,42,43] and the performance (e.g., frequency, operation voltage, $\Delta V_{OUT}/V_{DD}$, etc.) of our devices is comparable to or better than the best reported values, while the operation voltage for our devices is much lower. We have recently become aware of a report of 7-stage electrolyte-gated ring oscillators operating at frequencies up to 225 Hz.[44] The channel lengths in these devices were 2.5 μm, however, which is 10 times smaller than the channel lengths we have used here.

We also kept the ring oscillator operating continuously at constant V_{DD} and V_{BIAS} for an extended period. After 15 h, the device was still oscillating (see Supporting Information). However, the frequency dropped by nearly 80%, and the output range was reduced by half. This time-dependent performance decay is caused by threshold voltage shift in the gel-OTFTs. The cause of this shift and strategies to mitigate it will be the subject of further investigation.

We have fabricated fast five-stage ring oscillators based on resistor-load inverters as well, as detailed in the Supporting Information. The oscillation frequencies of the devices were found to increase with increasing V_{DD} and decreasing channel length, with a maximum frequency of approximately 117 Hz.

NAND logic gates were fabricated by printing two identical transistors and a resistor. The circuit diagram and logic sequence of the device are displayed in Figure 5a. Similar to the inverter, we define any voltage more positive than 0 V as state "1" and values near −1 V as state "0". Figure 5b shows good NAND logic gate response to two square-wave input signals (V_A at 100 Hz and V_B at 200 Hz). Only when the gate voltages of both inputs were held at "1" was the output voltage (V_{OUT}) switched to "0". In all other conditions, at least one of the transistors had resistance

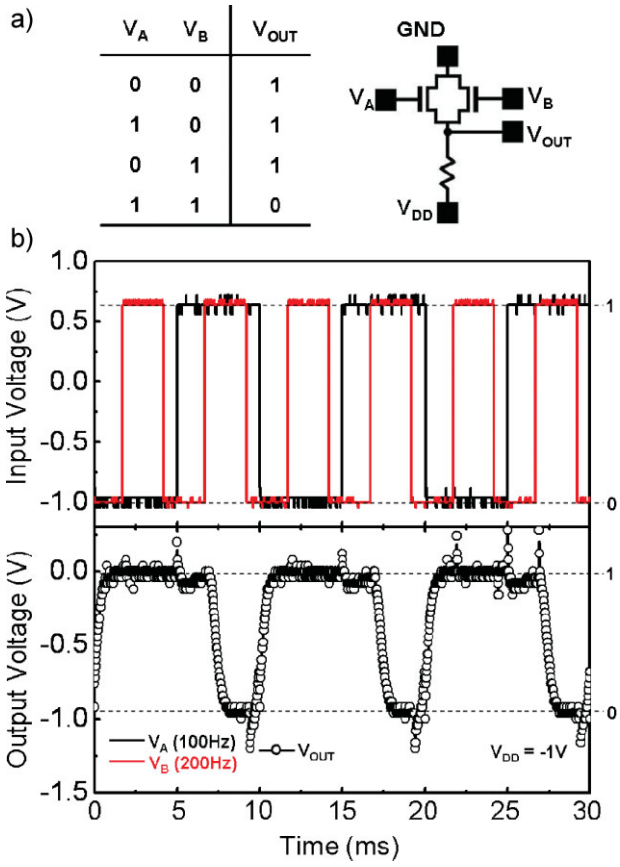

Figure 5. NAND logic gate based on printed gel-OTFTs and a printed resistor. The substrate was SiO_2(300 nm)/Si. a) Logic sequence and circuit diagram. b) Dynamic response of the NAND gate. The red and black lines in the top panel represent two input voltages, V_A and V_B, respectively. The open circles in the bottom panel show the output response. Transistor dimensions: $L = 25$ μm, $W = 500$ μm.

significantly larger than the load-resistor and V_{OUT} remained at the "1" state. The value of V_{OUT} was fully switched between the applied V_{DD} and ground within 2 ms. Successful fabrication of a NAND gate is a key result, given that by combining inverters and NAND gates, a wide variety of logic circuits can be constructed.

To illustrate this point and to demonstrate a higher level of transistor integration, we printed a *D* flip-flop circuit consisting of 8 NAND gates and 3 inverters (Fig. 6). A flip-flop is a critical building block in virtually every integrated circuit application ranging from microprocessors to radio frequency identification tags and liquid crystal displays. Its basic function is to sample the input voltage state (i.e., "0" or "1") at the moment of a rising edge of the clock signal (or falling edge if the clock input is active low). As shown in the measured output characteristics in Figure 6b, the output (*Q*) of the fabricated flip-flop read the state of data input (*D*) only at the moment of a falling edge of the clock signal (*CLK*). The subsequent changes of the *D* input did not influence *Q* until the next falling clock edge. The measured clock-to-output delay (t_{C-Q}, the response time of *Q* upon the falling edge of clock signal) and setup time (t_{setup}, the time for which the input signal has to be

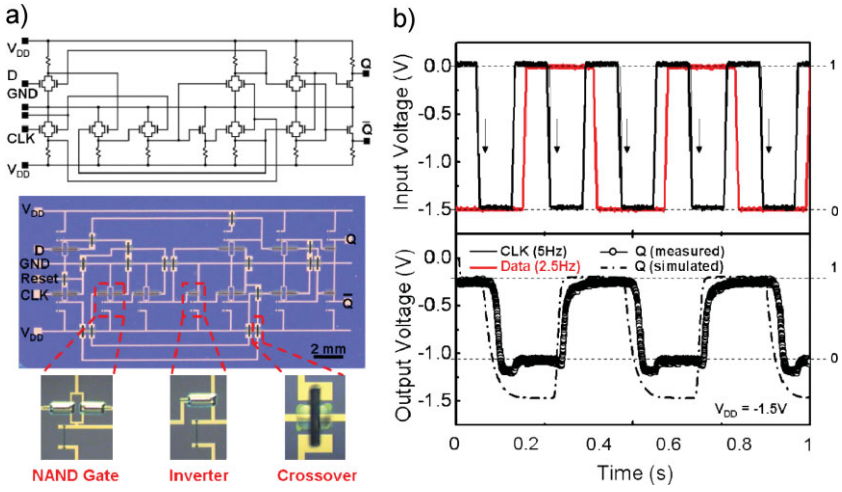

Figure 6. Printed *D* flip-flop circuit. a) Circuit diagram (top) and optical image of the circuit (bottom). The magnified images show the three most important features of the printed circuit. All Au electrodes and interconnects were fabricated by lift-off. Semiconductor, ion gel, and gate electrodes were printed. b) Dynamic response of the device. The red and black lines in the top panel represent the data and clock signals, respectively. The open circles in the bottom panel show the output response. Transistor dimensions: $L = 25\ \mu m$, $W = 500\ \mu m$. The dashed line in the bottom panel indicates the computer simulated output response under the same operation conditions.

stable before the falling clock edge in order for it to be properly sampled) in our devices were both less than 50 ms. The results demonstrate that it is clearly possible to integrate gel-OTFTs into functional circuits.

Further development of circuits based on gel-OTFTs will require the ability to model circuit behavior using commercially available software packages. We have used computer-aided-design tools from Cadence and Synopsys to design and simulate the *D* flip-flop in Figure 6; the details of the simulation process are described in Supporting Information. Figure 6b shows a comparison of the simulated and measured output characteristics. Importantly, one can see that the shape of the computed response matches the measurements well. The largest discrepancy lies in the magnitude of the voltage in the $Q = 0$ (low) state in that the simulation predicts a lower output voltage. The cause of the higher value of the low state may be due to gate leakage in the final output stage. Overall, however, the good match between simulation and measurement in Figure 6 indicates that modeling of gel-OTFT based circuits is possible, which will greatly facilitate the implementation of these devices in more complex applications.

5. Conclusion

We have demonstrated reproducible printing and performance of sub-2 V ion-gel-gated polymer transistors and circuits. The output current of the printed devices scaled as expected with channel width and length, facilitating circuit design, and indicating that the aerosol jet printing process is uniform and reproducible. Furthermore, a low cost printable conductor material, PEDOT:PSS, was found to be compatible with the ion gel dielectric and can be used to form the source, drain, and gate electrodes. Several digital and analog circuits were printed including transistor-loaded inverters with individual bias control on the load transistors to improve switching frequencies up to 10 kHz. A five stage ring oscillator was achieved, operating at 2 V with a propagation delay of 1 ms per stage. A 19 transistor *D* flip-flop circuit was fabricated and tested and the measured results compared well with a software model that incorporated discrete transistor characteristics. To our knowledge, the *D* flip-flop represents the highest level of integration achieved so far with electrolyte-gated transistors. Collectively, these results demonstrate that functional electrolyte-gated transistors can be incorporated into printed circuitry. Attractive features of ion-gel-gated transistors include high output conductance, low operation voltage, and ms switching times, and therefore circuits based on these devices are promising candidates for printed electronics applications. Future work will focus on further increases in switching speeds and minimizing OFF currents.

6. Experimental

Device Fabrication: All printing was accomplished using a commercially available aerosol-jet printing system manufactured by Optomec, Inc. In all-organic transistors, the conductive ink used for the source, drain, and gate electrodes consisted of 90% PEDOT:PSS (#PH 500, 1–1.4 wt% polymer in H_2O, from H.C. Stark) and 10% ethylene glycol. PEN was used as the substrate. Typical channel lengths were 50–100 μm and channel widths were 1000 μm. Semiconductor ink was made from 2 wt% P3HT (Rieke Metals) in a solvent mixture of chloroform and terpinol (9:1 by weight) and was printed in the channel region. After P3HT deposition, a layer of ion gel ink consisting of 9 wt% [EMIM][TFSI] (Solvent Innovation), 1 wt% poly(styrene-*b*-methyl methacrylate-*b*-styrene) ($M_n = 8.9$k-67k-8.9k, polydispersity 1.17, synthesized in house) and 90 wt% ethyl acetate was printed over the channel. In the last step, the gate electrode was printed using the PEDOT:PSS ink. The thickness of the printed PEDOT:PSS ink for the source, drain, and gate electrodes was approximately 40 nm as determined by optical profilometry, and the thickness of the ion gel gate dielectric was ~10 μm.

For circuit demonstrations, photolithographically patterned Au electrodes were used to form the source and drain electrodes and the interconnects. The substrates were oxidized Si wafers (SiO_2 thickness = 300 nm). Circuits were completed by subsequently printing P3HT, ion gel and PEDOT:PSS to form the channel, gate dielectric and gate electrode, as mentioned above. The transistor channel lengths varied from 5 to 200 μm and the channel widths varied from 20 to 500 μm. Resistors (with values ranging from 1–40 kΩ) were also printed using PEDOT:PSS ink. All printing steps were carried out in air while the substrate temperature was maintained at 60 °C to facilitate the ink drying. After printing, all devices and circuits were dried on a hot plate inside a glove box at 105 °C for 1 h.

Electrical Measurements: The electrical characterization of transistors and circuits were carried out in a Desert Cryogenics vacuum probe station. Two Keithley 236 source measurement units and two Keithley 6517 electrometers were used to apply the voltage and measure the current at low frequencies. In order to characterize the dynamic response of transistors and other circuits, Agilent 33220 and 33250 arbitrary-waveform generators were used for input voltage supplies. The output voltage responses were detected by a Tektronix TDS1002B or TDS3014C digital oscilloscope.

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