

Three-Dimensional Simulation and Analysis of Phase Change Memory Cell with Asymmetric Structure

J.J Sun^{1,2}, X.S Miao^{1,2}, X.M Cheng^{1,2, *}

¹ School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, People's Republic of China

² Wuhan National Laboratory for Optoelectronics, Wuhan 430074, People's Republic of China

As one of the most promising next-generation memory technologies, phase change memory (PCM) indeed shows a lot of advantages: high scalability, good compatibility with current CMOS processes, lower power consumption, fast access time etc. However, the large reset current is the critical problem which limits the application of PCM [1,2]. In this paper, we propose an asymmetric structure for PCM cell which is confirmed to be effective in decreasing the reset current based on our 3-dimensional electric-thermal simulations using Finite Element Analysis method.

As shown in Fig.1, the difference between the asymmetric and T-type symmetric structures is that, the upper opening and the bottom opening are not along the same axis (the central axis of cell) any more in the asymmetric structure. Offset is defined to be the distance between upper opening axis and the cell central axis. Fig.2 shows the cross-section temperature distribution in symmetric and asymmetric cells. With the upper contact opening offsetting, the phase change area deviates from the axis of phase change hole and becomes near the upper opening. Simulation results show that stimulated by same electric pulse, the peak temperature obtained in asymmetric cell with 10nm feature size is higher than that in conventional symmetric one by nearly 40%. Compared both structures, the key point is that in asymmetric cell the current path and heat dissipating condition are different from those in symmetric cell, which leads to the remarkable improvement in the electric-thermal conversion efficiency. Simulation results also suggest a proper offset value which is equal to the feature size is necessary for obtaining best electric-thermal conversion performance in asymmetric PCM cell.

References

- [1] M.H.R. Lankhorst, B.W. Ketelaars, R.A.M. Wolters. Nat.Mater. 4, (2005) 347..
- [2] H. X. Yang, L. P. Shi, R. Zhao, H. K. Lee, J.M. Li, K.G. Lim and T. C. Chong. IEEE International Memory Workshop. (2009) 68

* Corresponding author: email: xmcheng@mail.hust.edu.cn

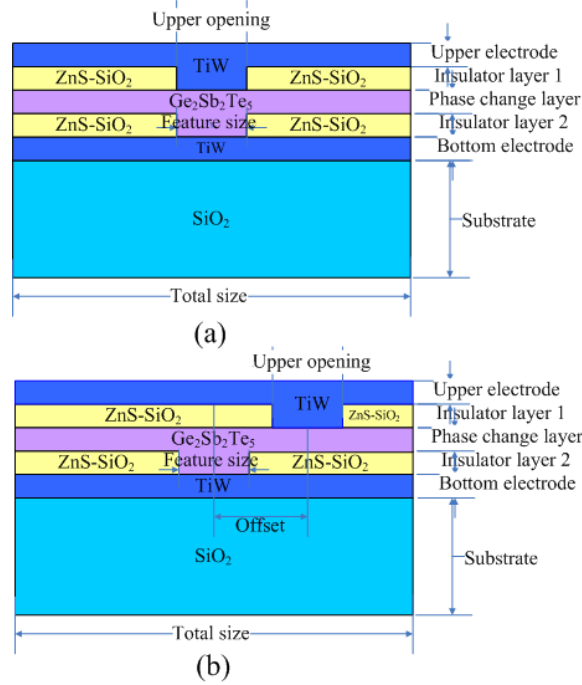


FIG.1 Cross section of PCM cells with (a) symmetric T-type structure and (b) asymmetric structure. Both cells are cylinder in our model

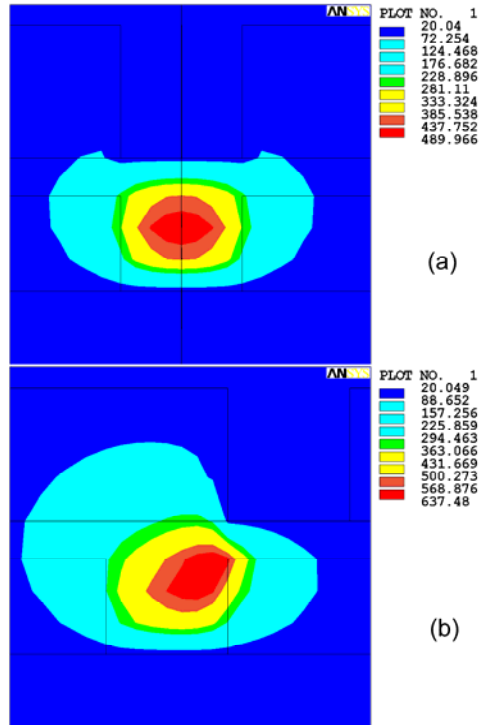


FIG.2 Cross section temperature distributions in (a) symmetric cell and (b) asymmetric cell with 32nm offset. (Feature size of both: 32nm)

Optimization of spin-torque switching using AC and DC pulses

T. Dunn^{1*}, A. Kamenev^{1,2}

¹*Department of Physics, University of Minnesota,
200 Union Street SE, Minneapolis, MN 55455*

²*Fine Theoretical Physics Institute, University of Minnesota,
200 Union Street SE, Minneapolis, MN 55455*

We present a theoretical description of spin-torque switching using AC and DC spin-currents. Using this description we numerically calculate the spin-current protocol which minimizes the energy cost associated with switching. This includes calculations for the optimal AC spin-current strength and frequency, the optimal DC spin-current pulse strength, and the optimal AC and DC switching times. We also provide a general analytic formulation for the spin-current protocol which gives the global minimum Joule heat loss for spin-current pulses composed of purely AC spin-current, purely DC spin-current, and pulses which are composed of an AC spin-current followed immediately by a DC spin-current. This gives rise to a well defined range of parameters where each strategy minimizes the Joule heat loss, see Fig. 1. The results of this optimization are compared with numerical simulations for specific cases.

* Corresponding author: email: dunn@physics.umn.edu

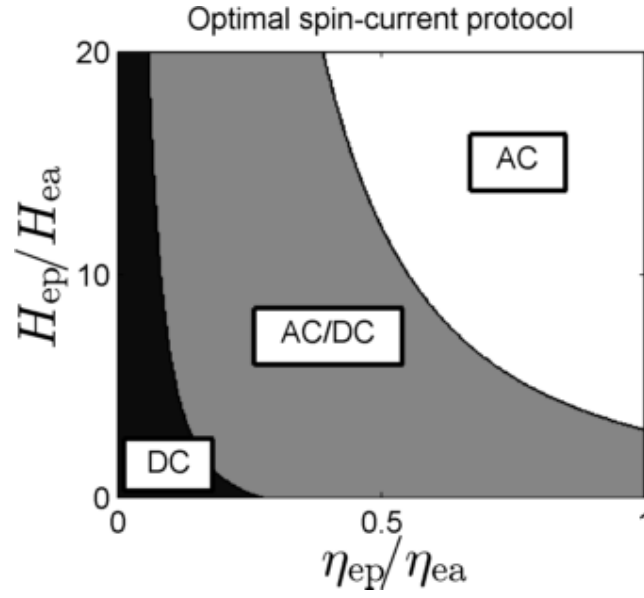


Fig 1: Shows optima spin-current protocol type (purely AC, purely DC, and AC followed by DC) as a function of the relative strengths of the easy-plane and easy-axis anisotropy fields H_{ep} / H_{ea} and easy-plane and easy-axis spin-current polarizations η_{ep} / η_{ea} .

Electric Control of Exchange Bias Training

W. Echtenkamp¹, C. Binek^{1*}

¹*Physics & Astronomy, University of Nebraska-Lincoln, Lincoln, NE, 68588-0299*

Voltage-controlled exchange bias (EB) is investigated in a Cr₂O₃(0001)/PdCo EB heterosystem. Earlier [1], reversible, room temperature isothermal switching of the EB field has been demonstrated in this system. Isothermal switching of EB is achieved when an electric field, E , and magnetic field, H , are simultaneously applied such that $E H$ overcomes a critical threshold. The EB of the system arises from chromia's electrically controllable boundary magnetization (BM). BM is an equilibrium property which emerges at the surface of magnetoelectric antiferromagnets. The BM couples to the bulk antiferromagnetic (AF) order parameter and follows the latter during switching. Here we introduce two new phenomena in electrically controlled magnetism, isothermal voltage-control of EB training and the isothermal voltage-controlled gradual tuning of equilibrium EB. Voltage-pulses are used to reverse the AF order parameter of magnetoelectric chromia, and thus continuously tune the EB of the adjacent PdCo film. Voltage-controlled EB training is initialized by tuning the AF interface into a non-equilibrium state incommensurate with the underlying bulk. As a result, EB training, which originates from triggered rearrangements at the AF interface during consecutively cycled hysteresis loops, can be tuned in a controlled manner between zero and sizable effects. Fig. 1a shows the EB field for the first and last loop of training sequences at a given electric tuning field. Large training effects are initialized at the critical switching field while elsewhere training is absent. We quantify the training effect through best fits of our Landau-Khalatnikov analytic expression [2] to the EB vs loop number as seen in Fig. 1b. The E-field dependence of the fitting parameters is interpreted in terms of the hysteretic E-field dependence of the AF order parameter. Interpretation of these hitherto unreported effects contributes new understanding to electrically controlled magnetism.

References

- [1] X. He, Y. Wang, N. Wu, A. Caruso, E. Vescovo, K.D. Belashchenko, P.A. Dowben, C. Binek *Nature Mater.* 9 (2010), 579-585
- [2] C. Binek, S. Polisetty, Xi He, A. Berger, *Phys. Rev. Lett.* 96 (2006), 067201

* Corresponding author: email: cbinek2@unl.edu

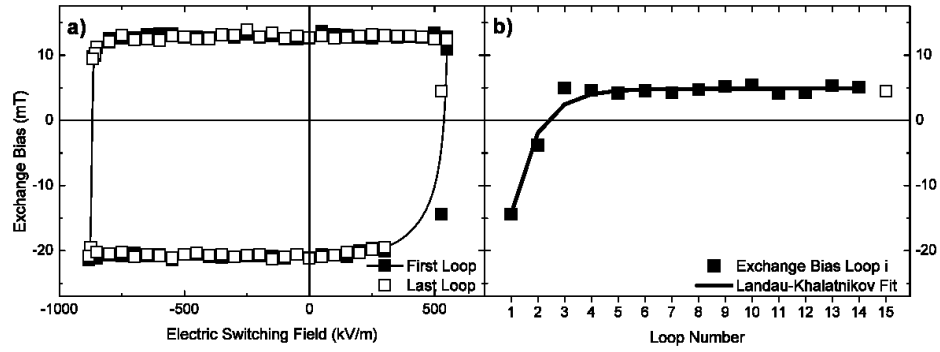


Figure 1: (a) EB field for first and last (solid and open squares) training loop vs. E (b) One exchange bias training series. The initial and equilibrium EB values are also illustrated in (a). The solid line is the best fit of the Landau-Khalatnikov expression

On-chip Multi-terminal Spin-Transfer Torque MRAM

X. Fong^{1*}, and K. Roy

¹*School of Electrical and Computer Engineering, Purdue University,
465 Northwestern Ave, West Lafayette, IN 47907*

Spin-transfer torque MRAM (STT-MRAM) is prevented from achieving its full potential due to design issues that may be attributed to its bi-directional write current requirement and shared read and write current paths [1]. Failure mitigation techniques have been proposed [2]-[4] but they may become ineffective at scale MTJ technologies due to different resistive characteristics [5] and asymmetries in MTJ characteristics [6].

These design issues may be overcome by multi-terminal STT-MRAM (MTSTT), such as the dual-pillar STT-MRAM (DPSTT, which decouples read and write current paths [7]) and complementary polarizers STT-MRAM (CPSTT, which uses complementary spin polarizers [8]), because they expand the design space of STT-MRAM by adding one more terminal to the basic structure. MTSTT require two access transistors (ATx's) but the footprint of MTSTT bit-cells may be smaller than conventional STT-MRAM after designing for process variations because each ATx in MTSTT may be much smaller than the ATx in conventional STT-MRAM. For example, the CPSTT (Fig. 1) based memory cell stores data in one free layer (FL) and writes data by steering current through one of two complementary polarized pinned layers (PL). Thus, ATx are never *source degenerated* and has unidirectional write current unlike in conventional STT-MRAM. The availability of complementary polarized PL's allow the use of self-referencing differential sensing scheme that is robust against process variations and has short sensing delays. Also, content-addressable memory functionality may be implemented in CPSTT without modifications to the memory cell due to its fully-differential nature. Our analysis (Fig. 2) shows that CPSTT memory cells may have up to 25% lower write power at iso-write margin and cell area, improved sensing margins and read disturb failures.

References

- [1] X. Fong, S. H. Choday, K. Roy, IEEE Trans. Nanotechnol. 11 (2012) 172-181.
- [2] G. Jeong *et al*, IEEE J. Solid-State Circuits 38 (2003) 1906-1910.
- [3] Z. Sun *et al*, IEEE Trans. VLSI 20 (2012) 2020-2030.
- [4] X. Fong, Y. Kim, S. H. Choday, K. Roy, to appear in IEEE Trans. VLSI (2013).
- [5] M. Gajek *et al*, Appl. Phys. Lett. 100 (2012) 132408-1-132408-3.
- [6] Y. Zhang *et al*, DATE (2012) 1313-1318.
- [7] N. N. Mojumder *et al*, ACM JETC 9 (2013) 14.
- [8] X. Fong, K. Roy, IEEE EDL 34 (2013) 232-234.

* Corresponding author: email: xfong@purdue.edu

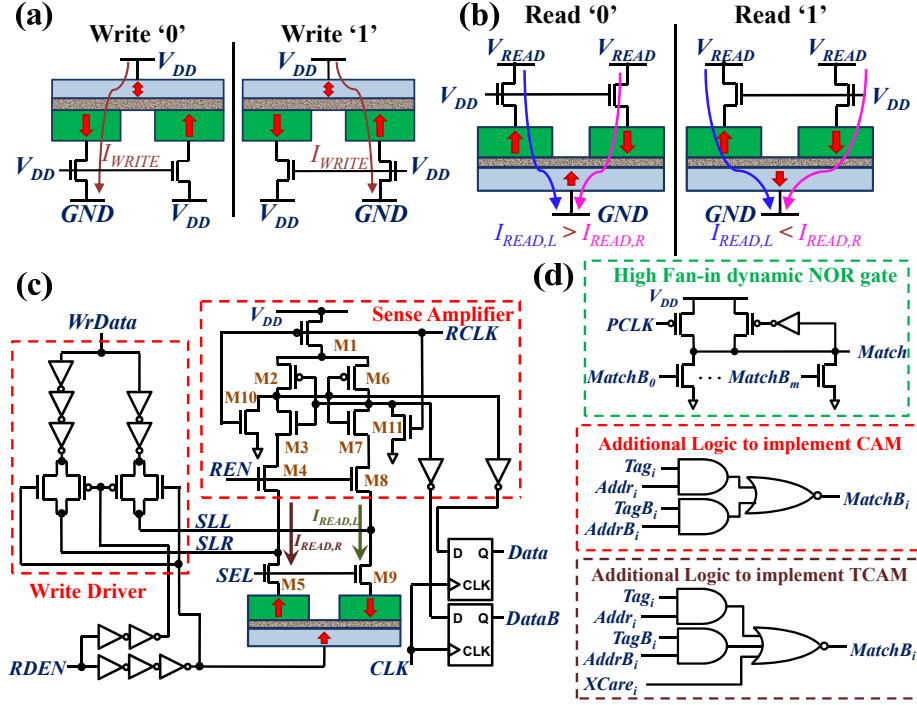


Fig. 1. (a) Write and (b) read operation principle of CPSTT memory cell and (c) the peripheral circuitry for memory array operation. (d) Content-addressable memory (CAM) implementations may be achieved using additional logic in the read sense amplifier, which is shared along a column, without modifications to the CPSTT memory cell as compared to 6T1SRAM based CAM.

Barrier Height	$56k_B T$
Write Pulse Width	2ns
FL size (1T1MTJ)	$10 \times 10 \times 1.5 \text{ nm}^3$
FL size (CPSTT)	$10 \times 22.5 \times 1.5 \text{ nm}^3$
1T1MTJ $I_C('0'), I_C('1')$	9 μ A, 17 μ A
CPSTT $I_C('0'), I_C('1')$	14 μ A, 14 μ A
TMR	$\sim 160\%$ @ $t_{MgO} = 1.15 \text{ nm}$
RAp @ $V_{MT} = 0 \text{ V}$	$\sim 7.5 \Omega \cdot \mu\text{m}^2$ @ $t_{MgO} = 1.15 \text{ nm}$

t_{MgO} (nm)	CPSTT Write Power (μ W)	1T1MTJ Write Power (μ W)
0.9	9.626	13.05
0.95	10.95	14.32
1.00	14.36	15.98
1.05	17.20	17.99
1.10	19.66	20.13
1.15	21.80	22.23

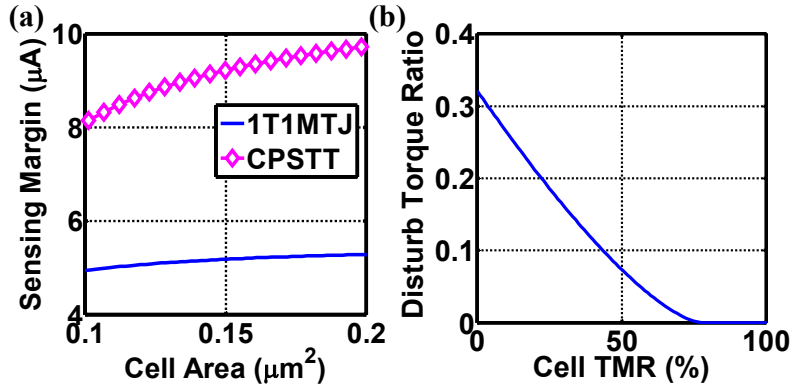


Fig. 2. Numerical analysis using the parameters shown in the top left table shows that CPSTT has better write power efficiency than 1T1MTJ STT-MRAM at iso-write margin (10%) and iso-cell area ($\sim 0.1308 \mu\text{m}^2$). (a) Sensing margin of CPSTT is about 2x that of 1T1MTJ while (b) torque per read current is also lower in CPSTT.

Determination of Specific Contact Resistance of Ge₂Sb₂Te₅ Phase Change Materials by Spacer Etched Nanowires

Ruomeng Huang^{1*}, Ruiqi Chen¹, Behrad Gholipour², Kian Shen Kiang¹, Kai Sun¹,
Yudong Wang¹ and CH "Kees" De Groot¹

¹*School of Electronics and Computer Science, ²Optoelectronics Research Centre
University of Southampton, Southampton, United Kingdom SO17 1BJ*

Phase change materials (PCM) based memory device is considered as one of the most promising candidates for next-generation non-volatile solid-state memory [1]. The set and reset states in this device correspond to a low resistance and a high resistance of the cell, which in-turn correspond to the crystalline and amorphous states of the phase change material, respectively. The total resistance of a phase change memory cell, however, consists of the resistance from the PCM and the interfacial contact resistance of the PCM to the electrodes. Although a large amount research has been done on characterization of PCM resistance, little attention is paid to study the contact resistance. Here in this work, the contact resistance of Ge₂Sb₂Te₅ to titanium nitride (TiN) electrode has been characterized in both set and reset states using a nanowire structure obtained from spacer etch. This spacer etch is a novel technique and can be used as a low-cost alternative to E-beam lithography for sub-hundred nanometre nanowire fabrication. Unlike bottom-up technology, it is compatible with current CMOS process and the geometry and location of the nanowires can be precisely controlled. In this case it allows us make long structures with small contact area to separate the resistive contribution of bulk and interface.

Three different lengths (20 μm , 25 μm and 30 μm) of Ge₂Sb₂Te₅ nanowires with same cross-section area (50 nm \times 100 nm) were fabricated by space etching process. A high-insulating silicon dioxide layer was first patterned by photolithography and etched to form a step with a depth of 100 nanometers. A 100 nm layer of Ge₂Sb₂Te₅ was deposited by sputtering and anisotropically etched using an ion beam, leaving a spacer of Ge₂Sb₂Te₅ next to the oxide structure (Fig.1a-1c). TiN electrodes with a thickness of 200 nm were then patterned on both sides of the nanowire by lift-off (Fig.1d). The electrical characterization reveals the resistivity of the as-deposited Ge₂Sb₂Te₅ nanowire material to be 0.54 $\Omega\cdot\text{m}$. The specific contact resistance between the TiN electrode and amorphous Ge₂Sb₂Te₅ was extracted to be $9.37 \times 10^{-6} \Omega\cdot\text{m}^2$. Then nanowires were then thermally switched to crystalline state with resistivity of $3.37 \times 10^{-4} \Omega\cdot\text{m}$ and specific contact resistance of $7.07 \times 10^{-9} \Omega\cdot\text{m}^2$. Even for these very long wires, the $R_{\text{off}}/R_{\text{on}}$ ratio of 1.60×10^3 is partially determined by the contact resistance (Fig.2). These results indicate that for real memory cell layout, the contact resistance is the dominant factor in Ge₂Sb₂Te₅ phase change memory devices.

* Corresponding author: email: rh3g09@ecs.soton.ac.uk

References

- [1] S. Raoux, W. Welnic, and D. Ielmini, "Phase change materials and their application to nonvolatile memories," *Chemical Reviews*, vol. 110, pp 240-267, 2010.

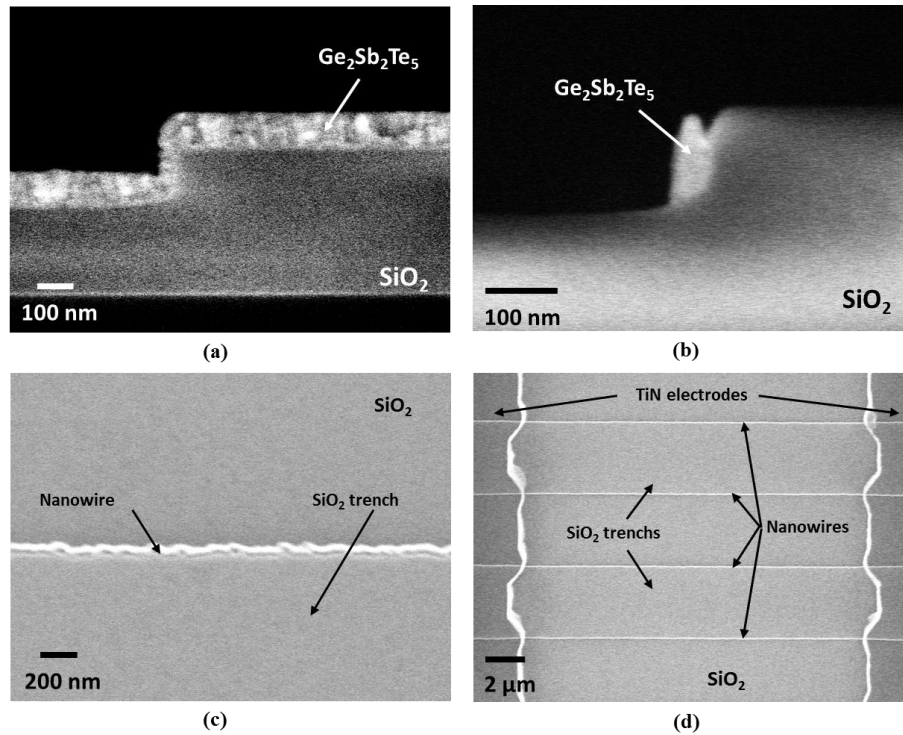


Fig.1 Cross-section SEM of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ samples (a) before spacer etch, (b) after spacer etch, (c) top view of a single spacer etched $\text{Ge}_2\text{Sb}_2\text{Te}_5$ nanowire and (d) SEM image of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ nanowire device with a length of 20 μm .

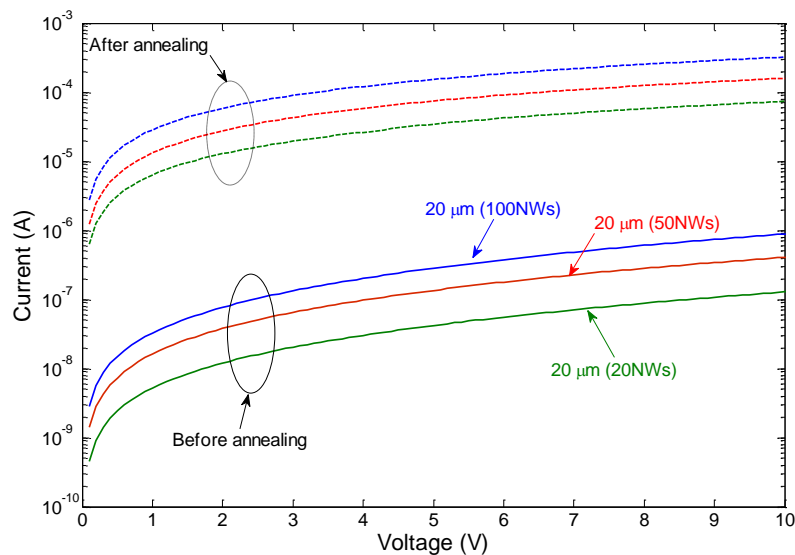


Fig.2 I-V characteristics for spacer etch $\text{Ge}_2\text{Sb}_2\text{Te}_5$ nanowire in both crystalline and amorphous phases with variable nanowire numbers.

Thickness dependence of the spin current pumping from CoFeB into Ta

Mahdi Jamali, Angeline Klemm, and Jian-Ping Wang ^{1*}

¹*Electrical and Computer Engineering Department, University of Minnesota, 200
Union Street SE, Minneapolis, MN 55455*

In recent years, the spin pumping where the spin current is injected from a magnetic material into a nonmagnetic material due to magnetization precession has been intensively investigated [1, 2]. The precessional magnetization induced spin current from ultra-thin film of Co₂₀Fe₆₀B₂₀ into Ta has been investigated. The frequency spectrum of the output dc-voltage at magnetic fields of ± 200 , ± 400 , and ± 600 is shown in Fig. 1(a) for a CoFeB thickness of 1.6 nm. As can be seen, by increasing the bias magnetic field, the frequency of the ISH voltage peak position is shifted toward the higher frequency which is consistent with the frequency response of a ferromagnetic resonance (FMR). Furthermore, by changing the polarity of the magnetic field, the polarity of the output dc-voltage altered which is in line with the spin pumping measurements in Permalloy [3]. In addition, in contrast to the previous report of the spin pumping characterization, the spin pumping at positive fields has more than two times larger amplitude than the negative field. We further performed the measurement at different magnetic fields for various thicknesses of the CoFeB in MgO/CoFeB/Ta sandwich. The spin pumping frequency as a function of the magnetic field is shown in the Fig. 1(b). It is clear that by reducing the thickness of the CoFeB from 10 nm down to 1.6 nm, the spin pumping frequency shows a red-shift behavior. Furthermore, interestingly the dependence of the frequency over the magnetic field changes from a quadratic to a linear behavior. Our experimental results suggest that the reduction of the effective demagnetization field due to the interfacial anisotropy is responsible for the enhancement of the spin pumping nonreciprocal behavior and frequency response of the spin pumping spectrum.

References

- [1] M. V. Costache, M. Sladkov, S. M. Watts, C. H. van der Wal, and B. J. van Wees, Phys. Rev. Lett. **97** (2006), 216603.
- [2] K. Ando, S. Takahashi, J. Ieda, H. Kurebayashi, T. Trypiniotis, C. H. W. Barnes, S. Maekawa, and E. Saitoh, Nat. Mater. **10** (2011), 655.
- [3] E. Saitoh, M. Ueda, H. Miyajima, and G. Tatara, Appl. Phys. Lett. **88** (2006), 182509.

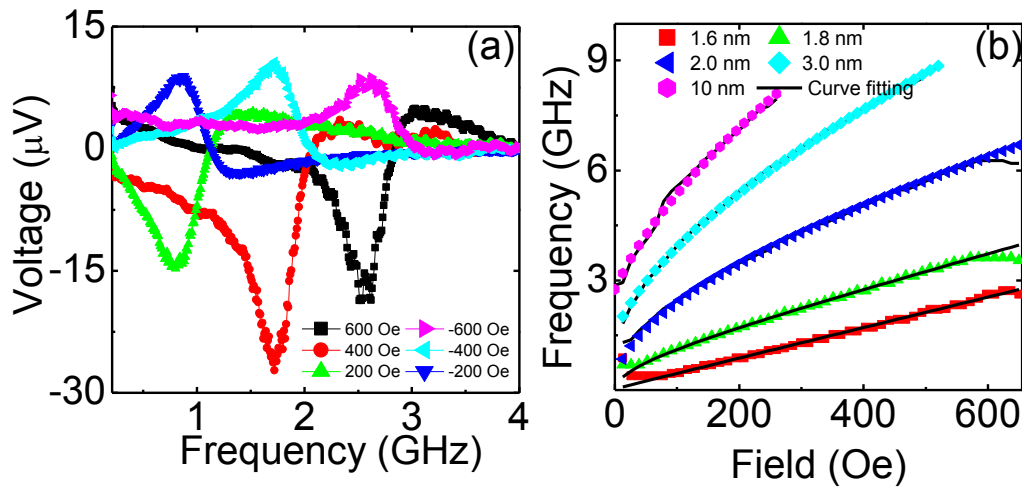


Fig. 1: (a) The frequency spectrum of output dc-voltage measured at magnetic fields of ± 200 , ± 400 , and ± 600 Oe for the device with a CoFeB thickness of 1.6 nm that annealed at 300° C. (b) The frequency spectrum of the output dc-voltage at different magnetic fields for samples with thickness of 1.6, 1.8, 2.0, 3.0, and 10 nm together with their corresponding curve fitting.

Sub-200 ps STT switching in thermally stable magnetic tunnel junctions with perpendicular magnetic anisotropy

Hui Zhao, Yisong Zhang, Andrew Lyle, Yang Lv, Mahdi Jamali and Jian-Ping Wang ^{1*}

¹*Electrical and Computer Engineering Department, University of Minnesota, 200 Union Street SE, Minneapolis, MN 55455*

Ultrafast spin transfer torque (STT) switching in the sub-ns regime is one of the key issues for STT random access memory (STT-RAM). One of the crucial limitations for ultrafast switching is the incubation delay induced by pre-switching oscillation [1]. In this work, ultrafast spin transfer torque (STT) switching in an in-plane MgO magnetic tunnel junction (MTJ) with 50 nm × 150 nm elliptical shape was demonstrated. Fig. 1(a) shows the R–H loop of a MTJ sample with 2.0 nm free layer. The switching probability as a function of pulse width is plotted in Fig. 1(b), where each curve represents the setting same pulse amplitude. The labeled voltage is the pulse peak voltage on the device at the pulse duration corresponding to 50% switching probability. We observed 50% switching probability at 165 ps and 98% switching probability at 190 ps. Moreover, the switching probability curves were very steep and did not display a switching probability plateau because of the half precession period jitter as observed in some metallic SVs [1]. Furthermore, the observed sub-200 ps switching implies that incubation delay did not occur as a result of pre-switching oscillation.

The same switching probability measurement was also done for AP-P switching. We plot the pulse amplitude versus pulse width at 50% probability in Fig. 1(c) together with the breakdown voltage, which was measured from 20 MTJs' breakdown point with identical barrier thickness at various pulse widths. With the same applied voltage, the current through the device in the P state is about twice the value in the AP state due to the resistance difference in each state. Therefore, for P-AP switching higher voltages can be reached, thus allowing shorter switching times, as shown in Fig. 1(c).

Acknowledgement: Authors thank the support from DARPA STT-RAM program and NSF Minnesota MRSEC. Authors also are grateful to the discussion and help from Drs. Pedram Khalili Amiri, J.A. Katine and Juergen Langer, Profs. Hongwen Jiang, Kang L. Wang and Ilya N. Krivorotov.

References

- [1] Devolder T, Chappert C, Katine J A, Carey M J and Ito K (2007) Phys. Rev.B75 064402.

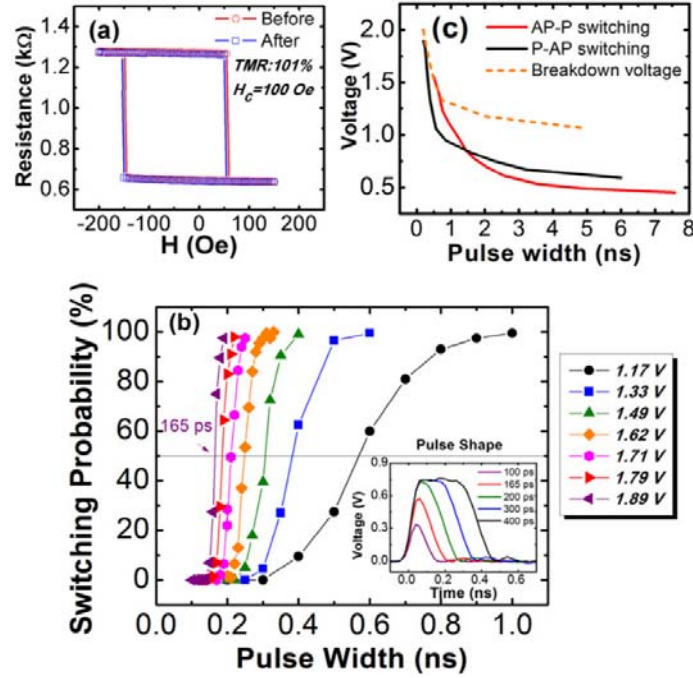


Figure 1. (a) MTJ resistance versus magnetic field loop at room temperature. The red curve is tested before switching probability measurement and the blue curve is obtained after switching probability measurement. (b) Switching probability dependence on pulse width with various pulse amplitudes on P-AP side. Each curve corresponds to the same setting voltage on pulse generator. The inset figure shows the change in pulse shape from 100 to 400 ps with the same setting amplitude. Because of the pulse peak attenuation, the labeled voltage in figure 1(b) is the peak voltage at the pulse duration corresponding to 50% switching probability. (c) Pulse voltage as a function of pulse width at 50% switching probability for AP-P and P-AP switching. And the dashed line is the breakdown voltage at different pulse widths.

Experimental Confirmation of Spin filtering Interface-Resistance

J-W Jung^{1*} and M. Sahashi¹

¹Electronic Engineering Department, Tohoku University, Sendai 980-8579, Japan

Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM) using a magnetoresistance (TMR) effect in magnetic tunnel junctions (MTJs) has offered promising application potential as next-generation non-volatile memory. In an epitaxial Fe/MgO/Fe(001) MTJ, for example, the MgO barrier does not only pass less spin polarized states with $\Delta_5(pd)$, $\Delta_2(d)$, $\Delta_2'(d)$ symmetries among the Bloch states of electron in Fe (001) electrodes but also perfectly spin polarized states with $\Delta_1(sp)$ symmetry due to the coherent tunneling [1]. Recently, Autés et al. have predicted by first principles calculation that MR ratio of Fe/Ag/MgO/Fe(001) MTJ is periodically enhanced as a function of Ag layer interlayer thickness between positive values in excess of 2000 % and negative values of the order of -100 % [2]. Furthermore, the spin-polarized current can pump enough energy into magnetic layer due to spin filtering, which would reduce the current density for magnetization switching due to the improvement in spin transfer torque efficiency. This prediction shows clearly why we focus on spin filter effect using combination between Fe and Ag layers. Although our epitaxial structure design is that for current-perpendicular-to-plane giant magnetoresistance (CPP-GMR), which consisting of two ferromagnetic layers (F) and one nonmagnetic (N) interlayer, it remains an excellent model easily to understand for spin filtering from asymmetric transmission probabilities of spin-up and spin-down electrons as Fe(001)/Ag interface. Remarkably large ΔRA values of $> 4.2\text{m}\Omega\ \mu\text{m}^2$ at $t_F = 5\ \text{nm}$ ($AR_{\downarrow} \sim 8\text{m}\Omega\ \mu\text{m}^2$, $AR_{\uparrow} \sim 1\text{m}\Omega\ \mu\text{m}^2$ and $AR_{F/N}^* \sim 2.2\text{m}\Omega\ \mu\text{m}^2$ against theoretical values of $13\text{m}\Omega\ \mu\text{m}^2$, $1\text{m}\Omega\ \mu\text{m}^2$ and $3.5\text{m}\Omega\ \mu\text{m}^2$, respectively) and MR ratio of 25 % was obtained from combination of high spin asymmetries and enhanced interfacial specific resistance in CPP-GMR devices even by using conventional FeCo alloy and Ag spacer with a thin Fe insertion layer between F and N layers. The improvement of ΔRA values of $6\ \text{m}\Omega\ \mu\text{m}^2$ was also obtained from inserted four thin Fe layer in our CPP-GMR device. We also experimentally investigated the variation of interfacial resistance ($AR_{F/N}$, $AR_{F/N}^*$) and $\gamma_{F/N}$ as a function of Fe concentration for $\text{Fe}_x\text{Co}_{100-x}/\text{Ag}$ interface which is to pave the way for better understanding from comparing with prediction findings at that interface [3].

References

- [1] W. H. Butler, X.-G. Zhang, J. M. MacLaren and T. C. Schulthess, Phys. Rev. B 63 (2001) 054416-1 – 054416-12.
- [2] G. Autés, J. Mathon, and A. Umerski, Phys. Rev. B 63 (2009) 024415-1 – 024415-6.
- [3] M. D. Stiles and D. R. Penn, Phys. Rev B 61 (2000) 3200-3202

* Corresponding author: email: sahashi@ecei.tohoku.ac.jp

	β_F	$\ell_{if}^{(F)}$ (nm)	AR_{\downarrow} (m $\Omega\mu m^2$)	AR_{\uparrow} (m $\Omega\mu m^2$)	$\gamma_{F/N}$	$AR_{F/N}$ (m $\Omega\mu m^2$)	$AR_{F/N}^*$ (m $\Omega\mu m^2$)
w/o insertion thin Fe layer	0.82	12	3.14	0.34	0.81	0.30	0.87
with insertion thin Fe layer	0.82	12	7.98	1.08	0.84	0.65	2.17
Theoretical results (Fe/Ag)	(unknown)		12.86	1.07	0.85	0.97	3.48

Figure 1. The table shows the spin dependent resistance at interface. The upper portion of the table is our calculated results from modified valet and Fert theory with asymmetric small number F/N 5-layers system.

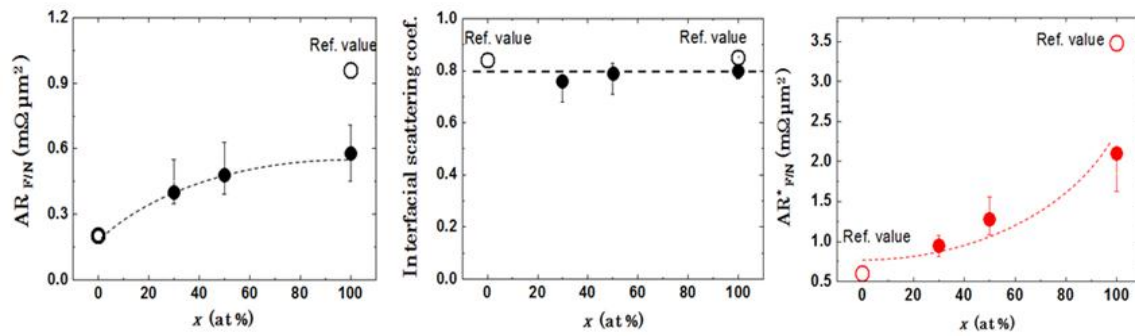


Figure 2. Fe concentration dependence of interfacial resistance, $AR_{F/N}$, interfacial scattering coefficient, $\gamma_{F/N}$, and interfacial specific resistance, $AR_{F/N}^*$, respectively at Fe_xCo_{100-x}/Ag interface.

Spin Transfer Torque Programming and Clock Field Effects for Dipole Coupled Nanomagnetic Arrays

A. Klemm¹, J. Harms¹, A. Lyle¹, D. Martens², J.P. Wang^{1*}

¹*Electrical and Computer Engineering Department, University of Minnesota, 200
Union Street SE, Minneapolis, MN 55455*

²*MRSEC REU Student*

Limitations in complementary metal-oxide-semiconductor technology, such as scalability and power consumption, are increasing the demand for new technologies. One approach is magnetic quantum cellular automata (MQCA) [1,2], which utilizes dipole coupled nanomagnets. Recently, magneto-resistance (MR) read out[3] has been demonstrated. In this study, we demonstrate spin transfer torque programming of individual dipole coupled nanomagnets [4,5], as well as investigate the effects of the clock field and dipole field on STT programming, both of which are essential to demonstrating future logic functions, such as the majority gate.

Magnetic tunnel junction pillars were fabricated that were 50nm X 80nm with top contacts of 50nm or 130nm wide to contact either one or two pillars to study the clocking field. LLG Micromagnetics Simulator(TM) was used to simulate STT switching of the dots.

A magnetic field was used to set the initial state of the magnets followed by a pulsed hard axis clock field to assist with STT programming of the dots. Two cases were considered. The first case is contacting a single dot and the second case of contacting two dots for the purpose of studying the dipole interactions. In the single dot case, the dipole field from neighboring dots reduced the switching current. For the case of contacting two dots, the dipole field from the neighboring dots counteracts STT switching, and the required current for switching more than doubled. We demonstrated the amount of current needed to STT program individual devices with and without a clocking field, and the effect of spacing and number of elements in an array on the required current for programming.

Determining the current and clock field values is imperative for proper operation. This information could be used to aid with the demonstration of STT programming gates and computation by STT switching individual inputs to see a corresponding change in output. The experimental demonstration of an electrical based I/O is a significant advancement toward applications of MQCA logic devices as it will allow easier integration with current technologies.

This work was supported partially by the MRSEC Program of the National Science Foundation under Award Number DMR-0819885 and NSF ECCS (0702264) Parts of this work were carried out in the Characterization Facility, University of Minnesota, which receives partial support from NSF through the MRSEC program.

* E-mail: jpwang@umn.edu

- [1] R. Cowburn and M. Welland, "Room temperature magnetic quantum cellular automata," *Science*, vol. 287, p. 1466, 2000.
- [2] A. Imre, et al., "Majority logic gate for magnetic quantum-dot cellular automata," *Science*, vol. 311, p. 205, 2006.
- [3] A. Lyle, et al., "Probing dipole coupled nanomagnets using magnetoresistance read," *Applied Physics Letters*, vol. 98, p. 092502, 2011.
- [4] A. Lyle, et al., "Integration of spintronic interface for nanomagnetic arrays," *AIP Advances*, vol. 1, p. 042177, 2011.
- [5] A. Lyle, et al., "Spin transfer torque programming dipole coupled nanomagnet arrays," *Applied Physics Letters*, vol. 100, p. 012402, 2012.

Voltage Controlled Magnetic Tunnel Junction Based Logic Architecture

A. Lyle, S. Patil, J. Harms, X. Yao, A. Klemm, D. Lilja, and J.P. Wang*

*Electrical and Computer Engineering Department, University of Minnesota, 200
Union Street SE, Minneapolis, MN 55455*

Magnetic tunnel junction (MTJ) based logic devices are an attractive technology since they are non-volatile, high speed, high density, reprogrammable, and have been successfully integrated with CMOS in commercially available Magnetic Random Access Memory (MRAM)[1,2]. A significant amount of reprogrammable logic circuits based on magneto resistance (MR), MTJ and giant magneto resistance (GMR), have been proposed and demonstrated which realized the primitive Boolean logic operations[3] and more advanced components such as hybrid flip-flops[4] and full adders[5]. However, these previous circuits required every MR element to be read using a sense amplifier. Then the information is passed on to the next stage of circuitry. The need for this intermediate circuitry hinders fan-out function, adds integration complexity, power consumption, area and delay overheads to logic modules.

In this study, we have designed and fabricated a multiple MTJ based logic circuit which computes logic functions while transferring the data to the next logic gate without an intermediate sense amplifier. This MTJ logic circuit can perform Majority, AND, OR, NAND, and NOR operations using spin torque transfer (STT) switching[6,7]. We supplemented the experimental demonstration with SPICE simulations of the MTJ circuit. Simulations verified that fan-out to multiple outputs can be realized using CMOS current mirrors and compared MTJ and SRAM based circuits[8,9].

This work was supported partially by the MRSEC Program of the National Science Foundation under Award Number DMR-0819885 and NSF ECCS (0702264) and the DARPA Non-Volatile program. Parts of this work were carried out in the Characterization Facility, University of Minnesota, which receives partial support from NSF through the MRSEC program

- [1] S. Parkin, J. Xin, C. Kaiser, A. Panchula, K. Roche and M. Samant, *Proceedings of the IEEE* **91** (5), 661-680 (2003).
- [2] M. Durlam, et al., *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International* (2003), pp. 34.36.31-34.36.33.
- [3] S. Jun, *Magnetics, IEEE Transactions on* **33** (6), 4492-4497 (1997).

* E-mail: jpwang@umn.edu

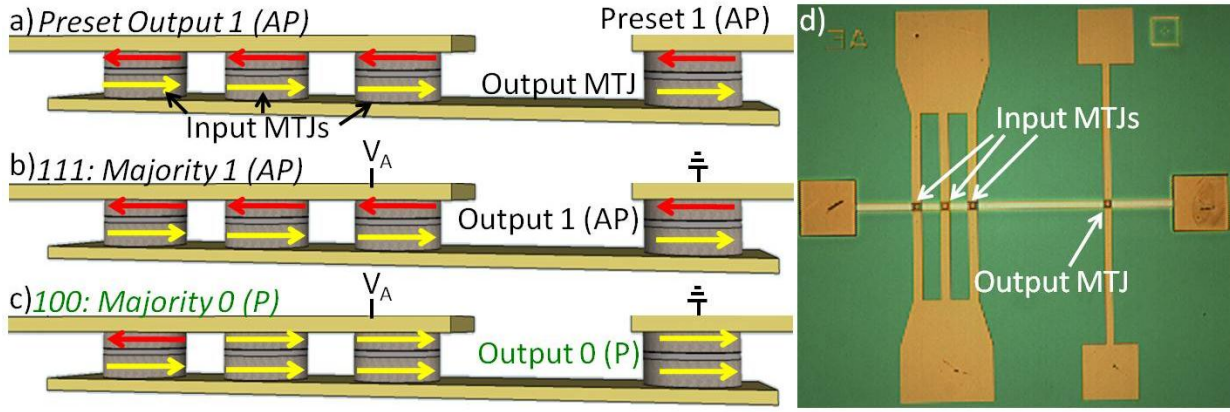


FIG. 1. Working principle of the circuit setup for Majority function: a) presetting circuit and operation for input b) 111 and c) 100 states and d) optical image of the fabricated device

[4] W. Zhao, E. Belhaire, V. Javerliac, C. Chappert and B. Dieny, in *Design and Test of Integrated Systems in Nanoscale Technology*, 2006. DTIS 2006. International Conference on (2006), pp. 323-326.

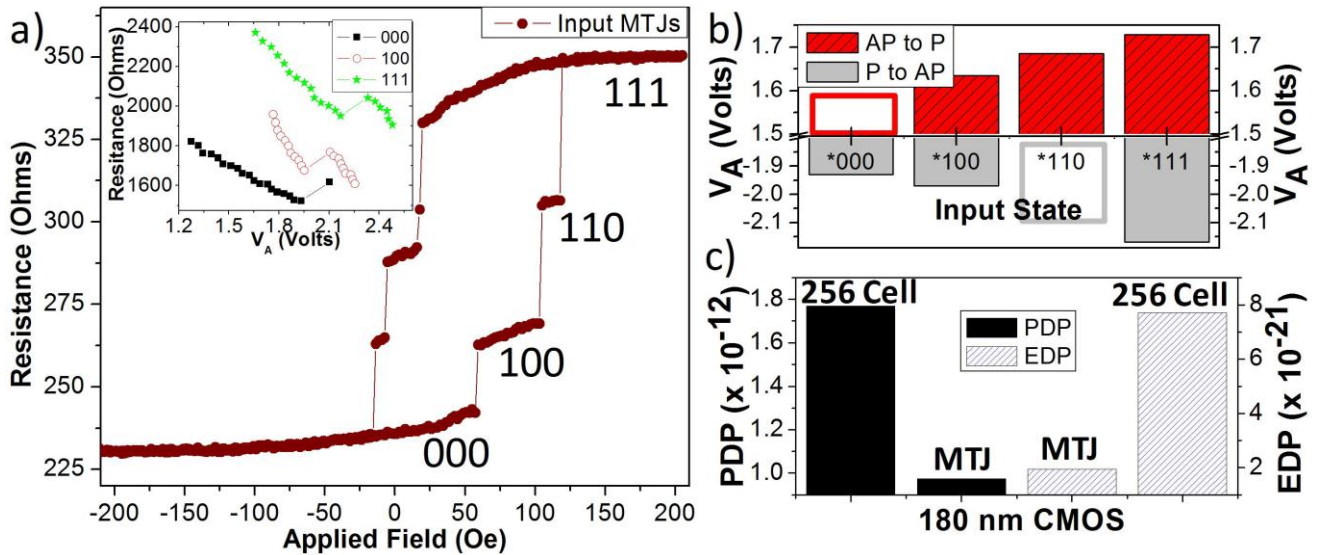


FIG. 2. a) Field switching of the input with the different resistance levels defined as logic states. (Inset shows output P to AP STT switching for different input states), b) voltage required to switch the output for P to AP and AP to P for different input states (Note: unfilled states estimated since field setting could not set all states), and c) simulated power and energy delay product comparison with 256 cell SRAM

[5] H. Meng, J. Wang and J.-P. Wang, *Electron Device Letters*, IEEE **26** (6), 360-362 (2005).

[6] L. Berger, *Physical Review B* **54** (13), 9353 (1996).

[7] J. C. Slonczewski, *Journal of Magnetism and Magnetic Materials* **159** (1-2), L1-L7 (1996).

[8] A. Lyle, J. Harms, S. Patil, X. Yao, D. J. Lilja and J.-P. Wang, *Applied Physics Letters* **97** (15), 152504 (2010).

[9] S. Patil, A. Lyle, J. Harms, D. J. Lilja and J.-P. Wang, in *Computer Design (ICCD), 2010 IEEE International Conference on* (2010), pp. 125-131.

Fabrication independent from lithography resolution for lateral phase-change random access memory

T. Lan^{1,2}, J. Zhou^{1,2}, W. L. Zhou^{1,2}*, X. S. Miao^{1,2}

¹ *Department of Electronic Science and Technology, Huazhong University of Science and Technology, Wuhan 430074, China*

² *Wuhan National Laboratory for Optoelectronics, Wuhan 430074, China*

Abstract: Phase-change random access memory (PCRAM) is a promising candidate for the next-generation nonvolatile memory. Since PCRAM with smaller feature sizes can usually achieve much better performance, many fabrication processes have been proposed to scale it down. Different from the most of these processes which relied on particular costly high resolution lithography, we proposed a cost-effective process based on angle evaporation to fabricate nanoscale lateral PCRAM. PCRAM cell with feature size of $80 \times 100\text{nm}$ were obtained although the resolution of the lithography machine in this process was $1\mu\text{m}$. Their performance is comparable to reported high-cost method. We successfully demonstrated a cost-effective scaling down route for PCRAM cell.

* Corresponding author: email: wlzhou@mail.hust.edu.cn

Design of a High Speed and Low Power Sense Amplifier for Magnetoelectric Random Access Memory (MeRAM)

Hochul Lee^{1*}, J G Alzate², P Khalili Amiri³, K L Wang

¹*Electrical Engineering Department, University of California, Los Angeles, CA 90095, USA*

Spin-transfer torque (STT) is a revolutionary mechanism to switch the states in magnetic tunnel junction (MTJ) devices, and the solid state magnetic memory which uses STT is one of the most promising candidates for commercialization in next generation products. However, its current based write method still requires a large amount of power, limiting the ultimate density [1]. Recently, the demonstration of voltage-induced magnetization reversal has opened a possibility to replace STT by electric-field pulses, giving rise to MeRAM as an emerging memory technology with an unparalleled write energy-efficiency any other non-volatile memories [2].

In this paper, a high speed and low power sense amplifier for magnetoelectric random access memory (MeRAM) is proposed. The sense amplifier circuit is designed based on TSMC 65nm technology and a Verilog-A based compact model for MeRAM which includes both models for current-induced (i.e. STT) and voltage-induced (i.e. VCMA) control of magnetization. The key point of the proposed sense amplifier is that read and write operations are optimized for high speed and low power by utilizing the highly energy-efficient voltage-induced toggle switching mechanism in MeRAM.

While STT switches MTJ states by changing the direction of critical current, in case of the toggle switching in MeRAM, its MTJ states always change after a voltage pulse of the right condition, imposing additional challenges for writing process. By using the proposed sense amplifier shown in Fig. 1, we are able to handle the toggle feature and execute write operation in such MeRAM bit with high energy efficiency (<10fJ). In order to write MTJ, the sense amplifier compares the data stored in MTJ to the new data. If both data are different, the sense amplifier gives a write pulse to MTJ to switch MTJ state. When the data stored in MTJ and the new data are same, the sense amplifier does not apply write pulse to MTJ, and MTJ remains previous state.

Read operation time is 7ns, and MTJ consumes 1.6uA and 3.3uA in case of anti-parallel and parallel state, respectively. These small sensing current is favorable in terms of not only power but also data retention [3]. During the write operation, we use 1.2V write pulse for 1.2ns, and maximum 9.8uA current flows MTJ, which is 50 times smaller than that of STT-RAM. Furthermore, if the data stored in MTJ and the new data are same, the circuit does not consume write power. The proposed sense amplifier maximizes the advantages of MeRAM, low power and high speed, and guarantees reliable circuit functionality with handling toggle feature of MeRAM.

* Corresponding author: email: chul0524@ucla.edu

References

- [1] Sun, J. Z. & Ralph, D. C. Magnetoresistance and spin-transfer torque in magnetic tunnel junctions. *J. Magn. Magn. Mater.* 320, 1227-1237 (2008).
- [2] E K L Wang, J G Alzate, P Khalili Amiri Low-power non-volatile spintronic memory: STT-RAM and beyond. *J. Phys. D: Appl. Phys.* 46 (2013)
- [3] W.S. Zhao a,b,†, T. Devolder a,b, Y. Lakys Design considerations and strategies for high-reliable STT-MRAM. *Microelectronics Reliability* 51 (2011) 1454–1458

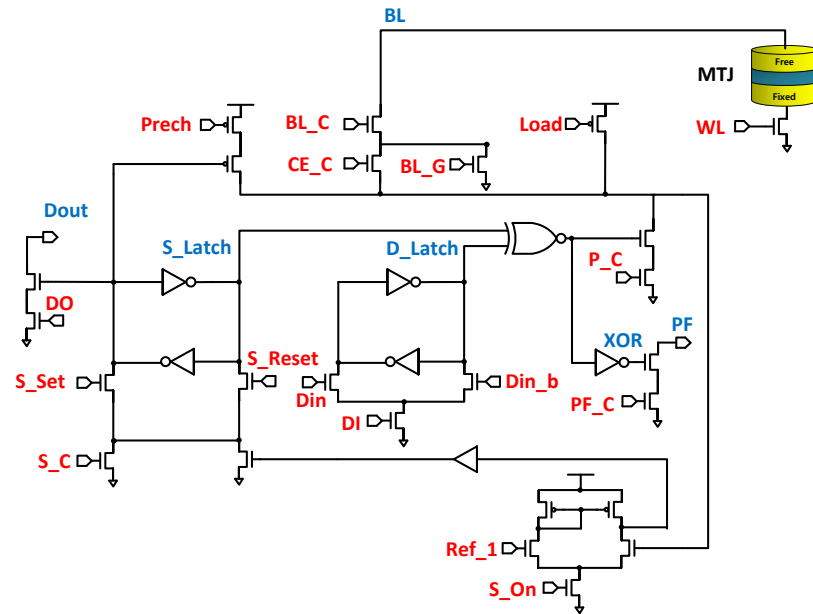


Figure 1. Proposed sense amplifier circuit for magnetoelectric random access memory

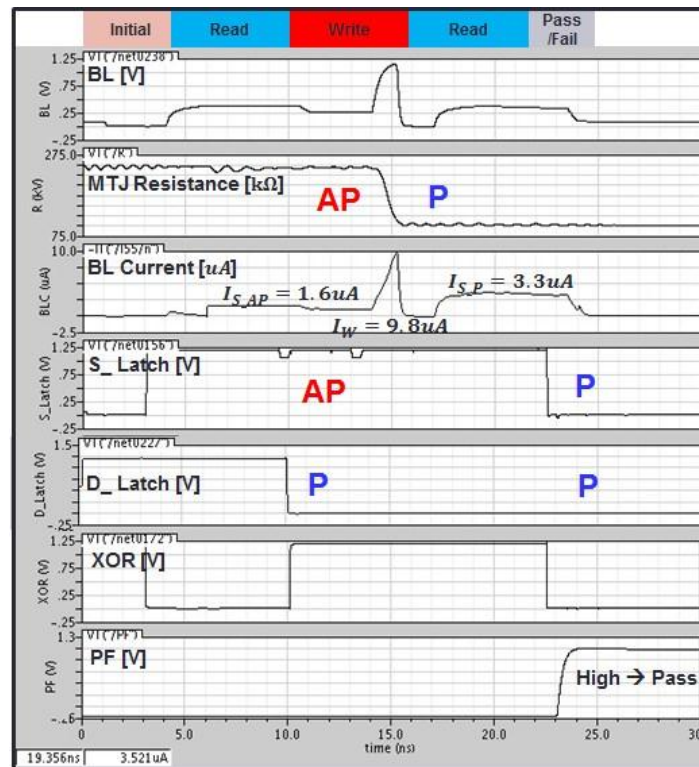


Figure 2. Key signals of sense amplifier and resistance of MTJ during write operation

Improved Memory Window of MONOS Capacitor Memory with GdON as Charge Storage Layer

L. Liu¹, J. P. Xu^{1*}, J. X. Chen¹, P. T. Lai²

¹*School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, People's Republic of China*

²*Department of Electrical & Electronic Engineering, the University of Hong Kong, Pokfulam Road, Hong Kong*

Trap-based MONOS nonvolatile memory has been rapidly developed due to its compatibility with high-density CMOS technology. GdO is considered as a promising gate dielectric candidate and its memory properties have been investigated and reported [1]. In this work, the nitrided GdO is prepared and compared with GdO as charge storage layer (CSL) to demonstrate validity of nitrogen incorporation into GdO for improving the memory characteristics. Fig. 1 is the TEM images of the fabricated MONOS capacitor memory with a stacked gate structure consisting of 2.5-nm thermal SiO₂ as tunneling layer, 6-nm high-*k* GdON or GdO as CSL (deposited by reactive sputtering of Gd₂O₃ in Ar/N₂ or Ar ambient respectively), 13-nm Al₂O₃ as blocking layer (deposited by ALD method), and Al evaporated as gate electrode.

Experimental results in Fig. 2(a) indicate that the GdON sample exhibits a large memory window of 7.7 V, 5.5 V and 3.1 V at P/E voltages of ± 15 V, ± 12 V, and ± 8 V respectively, indicating that a large quantity of electron traps with deeper levels could be generated by the N incorporation, giving high electron trapping capability. In Fig. 2(b), the GdON sample exhibits a large memory window for the initial 100 μ s, indicating high P/E speeds, and then the window gradually reaches saturation, demonstrating the stability of the program/erase states. For the GdO sample, larger negative shift of V_{FB} than that of the GdON sample in erasing state indicates that there could be more pre-existing hole traps in CSL, making excess holes injected during erasing [2]. So, it can be suggested that the GdON CSL is beneficial to suppressing the over-erase phenomenon (probably due to role of nitridation). The gradually increasing trend of the erasing window with P/E cycles (Fig. 2(c)), which results in little degradation of memory window after 10⁵ P/E cycles, could be due to newly-generated deep hole traps near the interface induced by the stress during the P/E operation [3]. For the retention properties, the GdON sample has a larger initial memory window of 5.6 V and an extrapolated 10-year memory window of 2.3 V, as compared with 3.0 V and 0.8 V of the GdO sample respectively (Fig. 2(d)). The large degradation rate at program state implies that those electrons trapped at the shallower levels near the GdON/SiO₂ interface are easier to leak out through the thin tunneling layer. It is expected that improved retention characteristics could be obtained if a suitable dual tunneling layer of high-*k*/SiO₂ is incorporated in the device.

* Corresponding author: email: jpxu@mail.hust.edu.cn

References

- [1] J. C. Wang, C. T. Lin, P. C. Chou, C. S. Lai, Microelectronics Reliability, 52 (2012) 635-641.
- [2] W. D. Brown and J. E. Brewer, New York: IEEE Press, 1998, 193-195.
- [3] Y. Q. Wang, W. S. Hwang, G. Zhang, G. Samudra, Y. C. Yeo, W. J. Yoo, IEEE Transactions on Electron Devices, 54 (2007) 2699- 2705

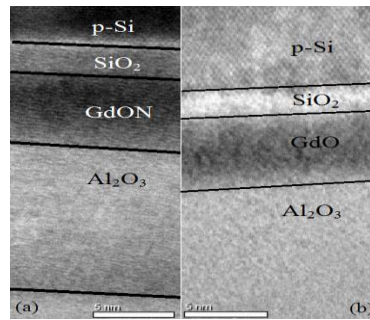


Fig. 1 TEM images of the stacked gate structure of Al/Al₂O₃/GdON/SiO₂/Si (a) and Al/Al₂O₃/GdO/SiO₂/Si (b)

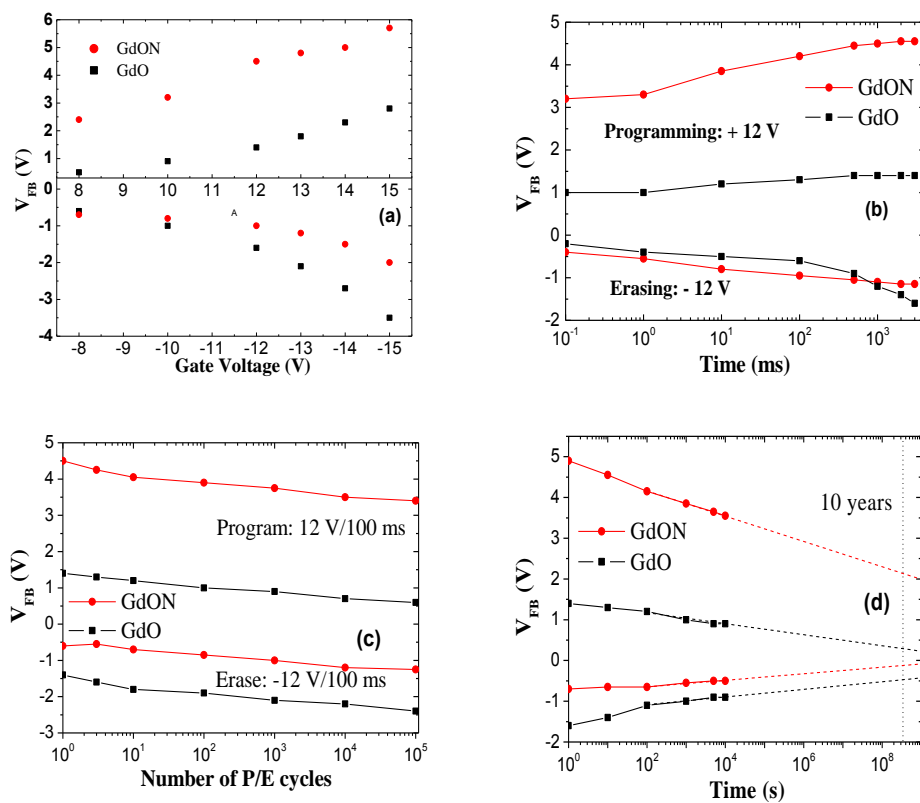


Fig. 2 The flat-band voltage (V_{FB}) under different P/E voltages for 1 s (a), change of V_{FB} with P/E time at ± 12 V voltages (b), endurance under the P/E cycles performed at ± 12 V for 100 ms/100 ms (c) and retention characteristics after removing 1-s P/E voltages at ± 12 V (d) for the two devices.

Analysis of Multilevel Capability of a Filamentary Resistive Memory Cell

T. Liu^{1*}, Y. Kang¹, T. Potnis¹, S. El-Helw¹, M. Orlowski¹

¹*Electrical and Computer Engineering Department, Virginia Polytechnic Institute and State University, 1185 Perry Street, Blacksburg, VA 24061*

Conductive bridge random access memory (CBRAM) is being extensively explored as a promising candidate for the next generation nonvolatile memory [1]. The resistive switching of CBRAM devices is based on the electrochemical formation and rupture of a metallic nanofilament. The multilevel cell (MLC) can be implemented by controlling the ON-state resistance (R_{ON}) of CBRAM. The R_{ON} - I_{CC} relation is universally valid for numerous anode/electrolyte/cathode material systems. Remarkably, the R_{ON} dependence on I_{CC} spans two physical regimes based on electron tunneling and radial growth mechanisms [2], [3].

The R_{ON} - I_{CC} plot of MLC is shown in Fig. 1 for our Cu/TaO_x/Pt devices. The data are fitted by $R_{ON} = 0.17/I_{CC}$, in which the voltage constant K is 0.17 V. After the compliance current is reached, the voltage across the filament V_{CF} drops abruptly to a value significantly lower than V_{SET} and is determined by the final resistance of the cell R_{ON} . This experimental observation implies that there is a minimum voltage $V = I_{CC}R_{ON}$ below which the filament growth comes to a halt. Fig. 2 shows the SET voltage dependence on the voltage sweep rate v . The linear increase of V_{SET} on $\ln(v)$ is only valid for large enough sweep rates. When v is less than 0.01 V/s, the SET voltage stays more or less constant and a minimum SET voltage is reached. Comparing this minimum V_{SET} to the voltage constant in Fig. 1, we find $K = V_{SET(min)} = 0.17$ V. This circumstance is universal to all $R_{ON} = K/I_{CC}$ relations in resistive switching cells reported in literature [4]. The constant K corresponds to the saturated SET voltage, below which the device cannot be switched ON in a reasonably long time.

The domain of validity for the R_{ON} - I_{CC} relation has also been identified. Once the lower resistance limit R_{min} is reached, the voltage drop on the filament cannot support further decrease of R_{ON} . Here R_{min} comprises the resistances of filament, electrodes, contacts, and interconnects. The limitation implies that the R_{ON} - I_{CC} relation can be justified only for $I_{CC} < K/R_{min}$ and not for arbitrarily high I_{CC} . The measured lower bound of R_{ON} on our Cu/TaO_x/Pt devices is several hundred ohms. Therefore the device resistance saturates for the compliance current above 1 mA instead of following the K/I_{CC} behavior. This constitutes a critical constraint for the design and operation of a multilevel cell.

References

- [1] J. J. Yang, D. B. Strukov, and D. R. Stewart, *Nature Nanotechnol.* 8 (2013) 13-24.
- [2] S. Menzel, U. Boettger, and R. Waser, *J. Appl. Phys.* 111 (2012) 014501.

* Corresponding author: email: tongliu@vt.edu

- [3] T. Liu, Y. Kang, S. El-Helw, T. Potnis, and M. K. Orlowski, Mater. Res. Soc. Symp. Proc. 1562 (2013) 552.
- [4] G. Palma, E. Vianello, G. Molas, C. Cagli, F. Longnos, J. Guy, M. Reyboz, C. Carabasse, M. Bernard, F. Dahmani, D. Bretegnier, J. Liebault, and B. De Salvo, Jpn. J. Appl. Phys. (2013) 04CD02.

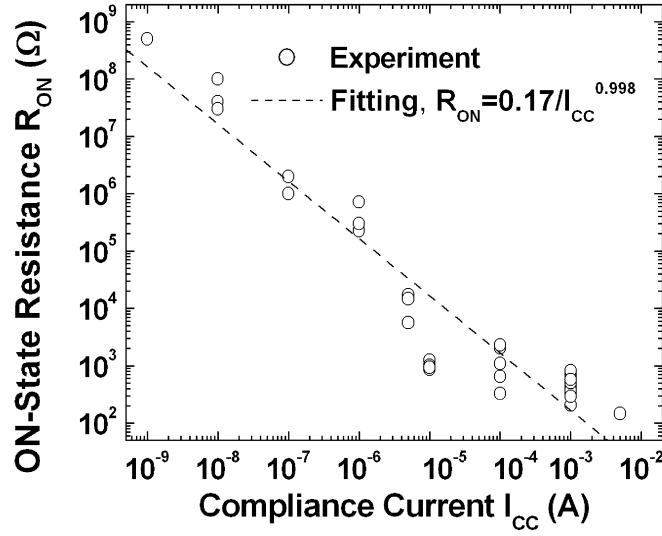


Fig. 1. Dependence of R_{ON} on compliance current for Cu/TaO_x/Pt devices.

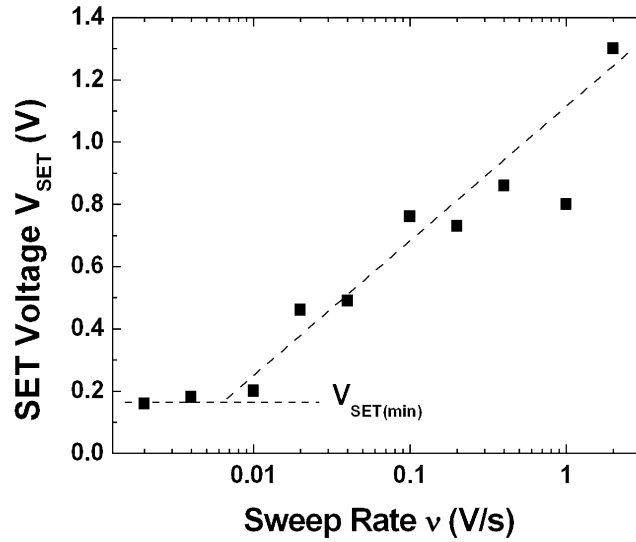


Fig. 2. Dependence of V_{SET} on voltage sweep rate for Cu/TaO_x/Pt devices.

A Serial Load Circuit Model for Low Resistance State in Resistance Switching Memory

Yang Lu¹, Xiang Yang¹ and I-Wei Chen^{1*}

¹*Department of Materials Science and Engineering, University of Pennsylvania
3231 Walnut Street, Philadelphia, PA 19104-6272*

Resistive random access memory (RRAM) stores “0” and “1” through two different resistance levels: high resistance state (HRS) and low resistance state (LRS). It is regarded as a promising candidate for the next generation memory technology capable of excellent memory performance such as fast switching speed, low operating voltage and high density 3D integration [1]. In applications, an extraneous load resistance is often utilized to protect RRAM from hard breakdown and to control resistance values [2]. An easily adjustable, sufficiently large LRS resistance (R_{LRS}), which includes the load resistance, is generally required to achieve low power consumption and uniform device performance. Although several models have been proposed to elucidate the LRS characteristics during switching [3-4], there is still a need for a simple relation that predicts R_{LRS} as a function of applied voltage and load. In this work, we present a serial load circuit model for such purpose. The model divides R_{LRS} into three parts: film resistance, internal load (including bottom electrode resistance R_{be} and spreading resistance R_s) and external load R_{ex} . To validate the model, four-point and two-point measurements with and without an external load are performed on a recently developed nanometallic RRAM [5], and fittings are performed for all the data with the same model parameters. Comparison of the two-point and four-point resistance reveals an R_s that is area insensitive (**Figure 1a**). Meanwhile, R_{ex} is found to efficiently tune the nanometallic film resistance over many orders of magnitude (**Figure 2a**). Model fitting of the voltage and R_{ex} dependence determines R_{be} and confirms a constant switching voltage V^* (**Figure 1b**) [6]. With these parameters known, the model can correctly predict R_{LRS} as a function of voltage and R_{ex} (**Figure 2b**). Because of the tunability of film resistance, at large voltages R_{LRS} asymptotically approaches the total load, $R_{be} + R_s + R_{ex}$, which has a weak size dependence. The model can be easily applied to explain multi-level switching without current compliance and to interpret LRS characteristics of other types of RRAM. It also provides design and operation guidelines for nanometallic RRAM devices.

References

- [1] Waser R, Aono M. *Nature materials*, 2007, 6(11): 833-840.
- [2] Yang X, Chen I W. *Scientific reports*, 2012, 2.
- [3] Xu N., et al. *VLSI Technology, 2008 Symposium on. IEEE*, 2008.
- [4] Ielmini D, Larentis S, Balatti S. *Integrated Reliability Workshop Final Report (IRW), 2012 IEEE International. IEEE*, 2012: 9-15.
- [5] Choi B J; Chen A B K; Yang X; Chen I W. *Advanced Materials* 23.33 (2011): 3847-3852.
- [6] Chen A B K; Choi B J, Yang X, Chen I W. *Advanced Functional Materials*, 2012, 22(3): 546-554.

* Corresponding author: email: iweichen@seas.upenn.edu

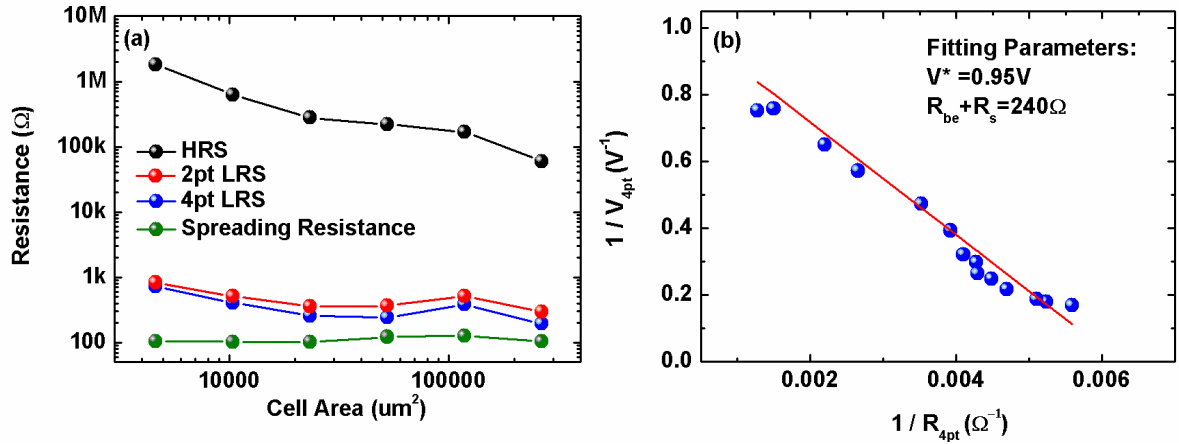


Figure 1. (a) Size dependence of HRS and LRS measured by four point and two point measurements. Their difference (120 Ω) is spreading resistance which is area independent. (b) Model fitting based on serial load circuit model.

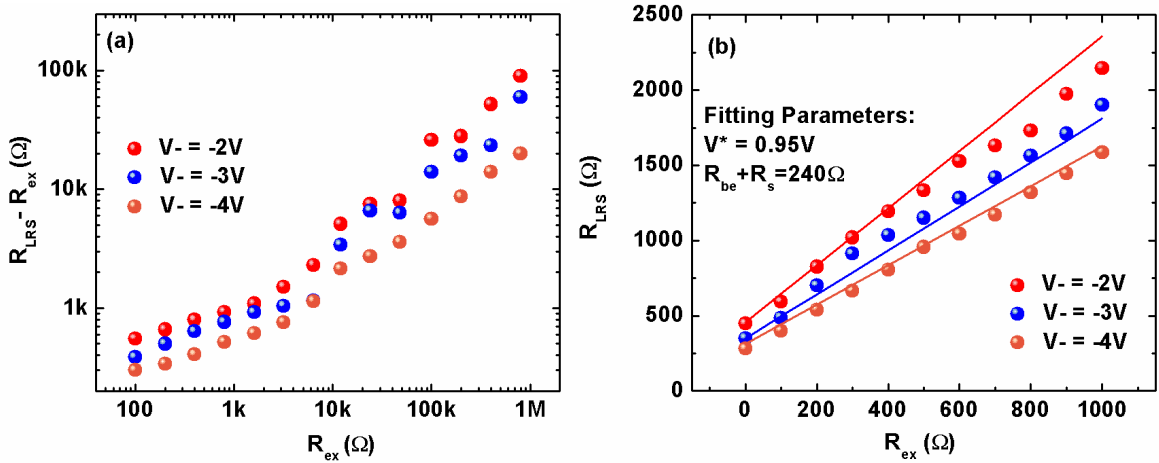


Figure 2. (a) $R_{LRS} - R_{ex}$ versus R_{ex} compared under different sweeping voltages. With increasing R_{ex} , film resistance plus internal load ($R_{LRS} - R_{ex}$) increases from 200 Ω to 100 k Ω . (b) Model fitting using the same parameters extracted from **Figure 1(b)**.

Spin-Transfer Torque Switching Above Room-Temperature

Hui Zhao, Yisong Zhang, Andrew Lyle, Yang Lv and Jian-Ping Wang

Dept. of Electrical and Computer Engineering, University of Minnesota, Minneapolis

The temperature dependent spin transfer torque (STT) switching measurement is crucial for spin transfer torque random access memory (STT-RAM) application since the device works in a heated environment. In this work, we investigate the MgO MTJ performance from 25 °C to 80 °C. The particular temperature range is chosen to imitate the real working environment of STT-RAM application. The thermal stability and critical current density are studied. In particular, we report the STT switching current mean and distribution from 1 ns to 0.1 s at various temperatures. The effect of the environmental temperature on critical current highly depends on the switching time due to different switching mechanisms. Critical current reduction with temperature is only found in long pulse regime ($>1\mu\text{s}$) caused by thermal activation switching. The distribution of critical current does not have strong dependence on temperature, but increases rapidly with the decrease of switching time.

Figure 1 (a) and (b) show the critical current density value at 50% switching probability in the short time regime and long time regime, respectively. It's clear that in the ns time scale, the critical current densities at three temperatures overlap with each other, while in the long time regime ($>1\mu\text{s}$), there is an obvious critical current density reduction with the increase of temperature. The longer the switching time, the more the critical current decreases. The result verifies the classic STT switching theory. In the long time regime, the free layer reversal happens by STT assisted thermal activation. Therefore, the environmental temperature has more contribution during thermal agitation. On the other hand, in the short time regime, it's a dynamic precessional switching process determined by the spin momentum transfer through STT, relatively independent from environmental temperature. We also estimate the thermal stability factor at three temperatures by the data in Fig. 2(b) according to Ref. [1]. The fitted thermal stability factors are 47 (at 25°C), 46 (at 50°C), and 41 (at 70°C) for Sample A and 32 (at 25°C), 30 (at 50°C), and 28 (at 70°C) for Sample B.

The measured 100 ms, 10 μs and 10 ns STT switching probability CDF curve of Sample A under three temperatures are shown in figure 2 (a). The derivative of CDF curve, the probability density function (PDF), are plotted in figure 2 (b). Here we can see not only the median point of critical current density reduces with the increase of the temperature as mentioned before, but the whole switching PDF also shifts together to the left when the sample is heated. And this shift is more obvious for long pulses too. The width of the switching PDF keeps almost constant at all temperatures. The switching PDFs are fitted according to Ref. [2], indicated by the solid curve in figure 2 (b). The mean and standard deviation (1σ) of critical switching current in Sample A from 10 ns to 0.1 s are summarized in figure 2 (c) and (d). The standard deviation increases dramatically as the pulse width reduces. We can also see that the decreased energy barrier, as a result of elevated environmental temperature, has more impact on

determining the median point rather than the variation of critical current in the long pulse regime.

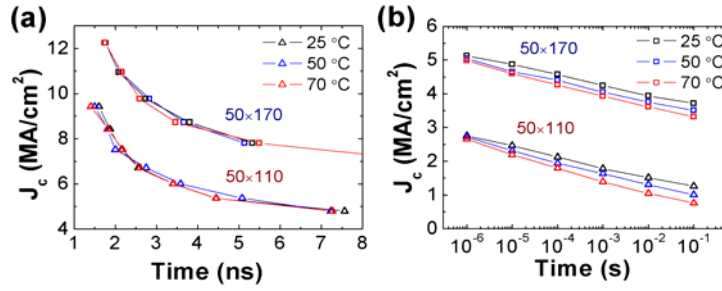


Figure.1. (a) and (b) Critical current density at 50% switching probability versus pulse widths at short time scale (1-8 ns) and long time scale (1 μ s-0.1 s).

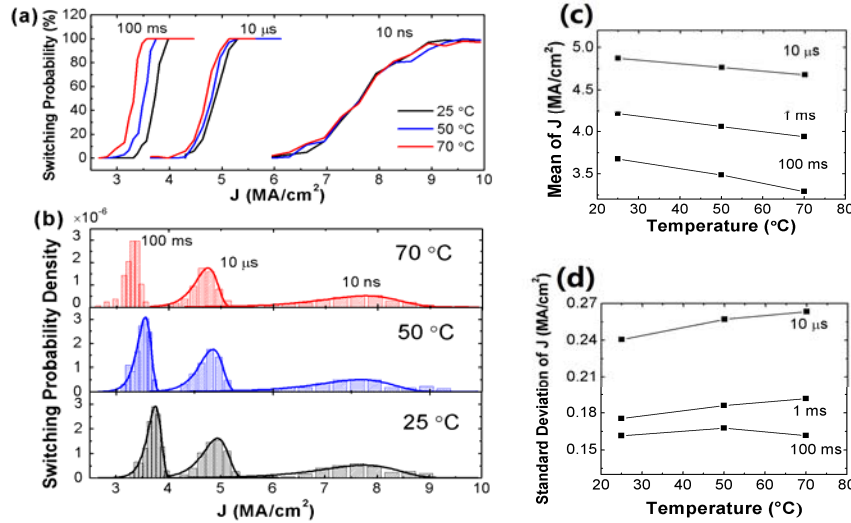


Figure.2. (a) Switching probability as a function of current density measured in Sample A at 100 ms, 10 μ s and 10 ns. (b) Switching probability density of sample A. The bars are experimental data and solid curves are fitted data. (c) and (d) Mean and Standard deviation of critical current density as a function of temperature measured in Sample A.

Acknowledgement: Authors thank the support from DARPA STT-RAM program and NSF Minnesota MRSEC. Authors also are grateful to the discussion and help from Drs. Pedram Khalili Amiri, J.A. Katine and Juergen Langer, Profs. Hongwen Jiang, Kang L. Wang and Ilya N. Krivorotov.

References

- [1] Sun, J. Z. Physical Review B 62.1 (2000): 570.
- [2] Li, Z., and S. Zhang. Physical Review B 69.13 (2004): 134416.

Reactive molecular dynamics of switching in conductive bridge random access memory

N. Onofrio^{1*}, D. Guzman¹, A. Strachan¹

¹*School of Materials Engineering, Purdue University, West Lafayette, IN 47906*

In the search of new memory devices, conductive bridge random access memory [1] (CBRAM) have been of particular interest due to their low power consumption, fast write/read capability, high endurance and scaling limits reaching nanometers [2]. These devices consist of a metal-insulator-metal structure and switch between high and low conductivity states with the application of voltage due to the formation and dissolution of a metallic conductive bridge. We present the first molecular dynamics (MD) simulations of switching in nanoscale devices based on Cu as the active electrode and amorphous SiO₂ electrolyte. The interactions between atoms are described by the reactive force field [3] *ReaxFF* and the charges are calculated self-consistently at each step of the simulation using the *charge equilibration* formalism [4]. We developed a rigorous method to describe the voltage applied between two electrodes via a modification of the atomic electronegativity in the electrode atoms identified on-the-fly during the simulation via cluster analysis.

Our simulations described the ionic dissolution of the active electrode into the solid electrolyte, the electric field-driven diffusion of the dissolved ions and their electro-deposition into the inactive electrode. We observed the creation of (single and multi) conductive filament growing sequentially from the active and/or from the inactive electrode and we have been able to switch and open the devices (see snapshots on **Figure 1**). Preliminary results suggest an avalanche effect in the copper diffusion leading to the switching process. The mechanical stress on the solid electrolyte is investigated as well as the localization of the growing filament.

These simulations provide key information regarding the atomic processes that govern the formation and dissolution of the conductive filament and consequently switching and we believe will eventually help in the design of improved devices and in the assessment of their ultimate scalability.

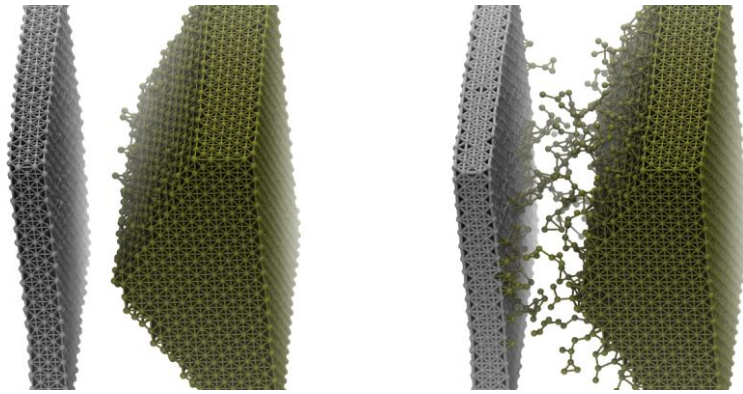


Fig. 1. Snapshot of a copper/a-SiO₂(hidden)/copper device in its initial (left) and switched (right) state (after 0.5 ns under 8 V potential). The separation between the tip of the active and the inactive electrode is 1 nm.

References

- [1] R. Wasner, R. Dittmann, G. Staikov and K. Szot, *Adv. Mat.*, 21, (2009), 2632-2663
- [2] V. V. Zhirnov, R. Meade, R. K. Cavin and G. Sandhu, *Nanotechnology*, (2011), 22, 254027
- [3] A. C. T. van Duin, S. Dasgupta, F. Lorant and W. A. Goddard III, *J. Phys. Chem.*, (2001), 105, 9396
- [4] A. K. Rappe and W. A. Goddard III, *J. Phys. Chem.*, (1991), 95, 3358

Investigation of dielectric for dual floating gate MOSFET

B. Sarkar*, S. Jayanti, N. Di Spigna, B. Lee, V. Misra, P. Franzon

*Department of Electrical and Computer Engineering, North Carolina State University
Raleigh, NC 27606, USA*

Flash memories have been vastly studied to enhance program and erase characteristics [1-2]. Similarly, one of the key issues of DRAM has been to overcome leaky capacitor [3]. While several attempts have been made to improve the performance of flash and DRAM separately, but an energy efficient circuit could be realized where both of them are combined in a single transistor. In this regard, dual floating gate transistors are seen as a potential memory candidate where the benefits of reduced circuit area and computational architecture can be achieved [4]. Depending upon the voltage applied to gate of the transistor, it can be used to store dynamic bit and non-volatile bit simultaneously.

Dual floating gate MOS capacitors were fabricated with following gate stack: n-Si/SiO₂(7 nm)/TaN(4 nm)/IMD/TaN(4 nm)/HfAlO(21 nm), where IMD stands for intermediate dielectric. TaN/W serves as gate. At lower gate bias, electrons from bottom floating gate are injected into top floating gate, thereby reducing the flatband voltage (V_{FB}), which corresponds to dynamic operation. Whereas at higher gate bias, electrons from substrate tunnel into floating gates and get redistributed resulting in increased V_{FB} , which is equivalent of storing a non-volatile bit. Fig. 1 shows the change in V_{FB} w.r.t pulse voltage with various IMD of same equivalent oxide thicknesses. Al₂O₃, which has higher barrier height and lower k-value, was observed to show negligible dynamic window. This can be attributed to low dielectric thickness, which fails to retain the charge on top floating gate after dynamic program. On the other hand, HfO₂, which has relatively higher k-value, showed a narrow dynamic window because of higher oxide thickness which limits the charge transfer between floating gates. Interestingly, HfAlO showed higher dynamic window than HfO₂ and Al₂O₃. Al₂O₃ content of HfAlO provides suitable barrier height, whereas HfO₂ content provides higher oxide thickness.

Following the results from MOS capacitor, dual floating gate transistor was fabricated with 4.5 nm HfAlO serving as IMD. Fig. 2(a) shows the CV measurement of the transistor at 1MHz frequency. Anti-clockwise hysteresis is observed till $\pm 9V$ sweep confirming dynamic operation of the device, whereas hysteresis is clockwise at $\pm 15V$ sweep which shows non-volatile mode of operation. Fig. 2(b) shows the increase in drain current after applying dynamic programming pulse at gate signifying a reduction in threshold voltage (V_T) after the programming. Fig. 2(c) shows the IV characteristics of the transistor for non-volatile programming and erasing. Significant change in V_T is observed which is similar to conventional flash memories.

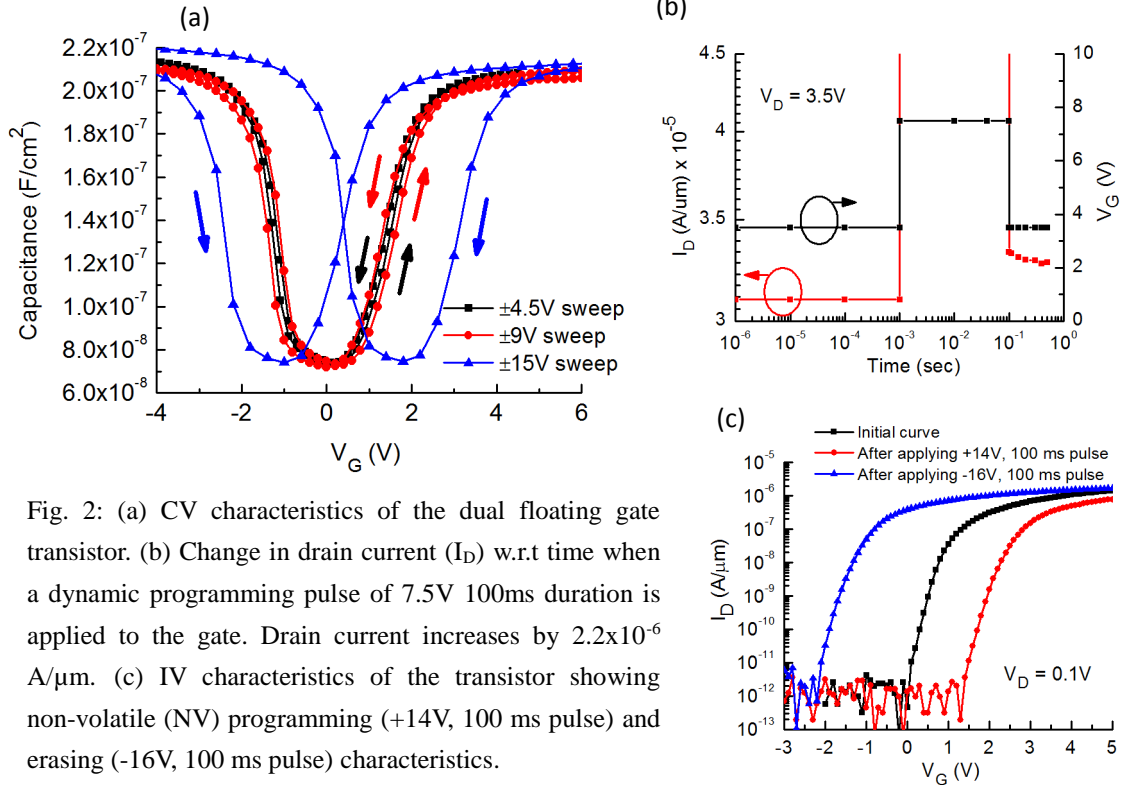
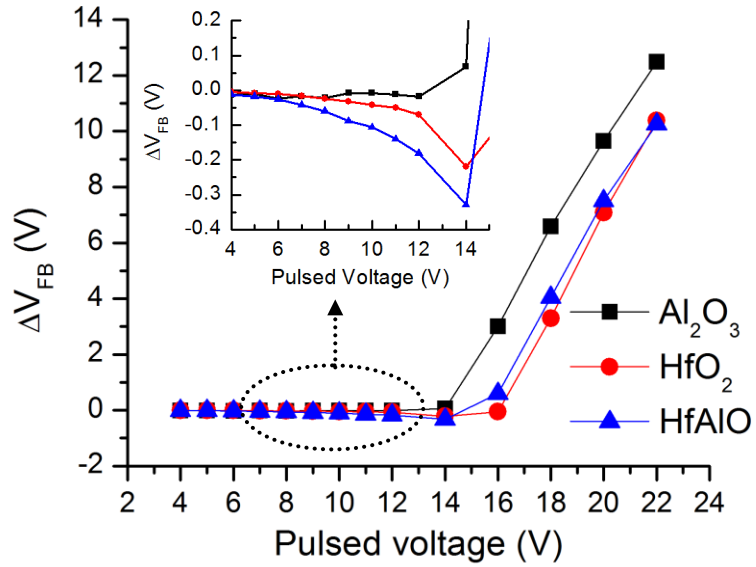
In conclusion, various dielectrics were investigated to find a potential candidate for intermediate dielectric of dual floating gate MOSFET. Transistor was then fabricated which showed to have dynamic and non-volatile bit storage capacity.

* Corresponding author: email: bsarkar@ncsu.edu

References

- [1] S. Jayanti, X. Yang, R. Suri, V. Misra, IEEE International Electron Devices Meeting (IEDM), pp. 106-109, 2010
- [2] P. Blomme, M. Rosmeulen, A. Cacciato, M. Kostermans, C. Vrancken, S. Van Aerde, T. Schram, I. Debusschere, M. Jurczak, J. Van Houdt, Symposium on VLSI Technology (VLSIT), pp. 129-130, 2010
- [3] M. G. Ertosun, NOVEL CAPACITORLESS SINGLE-TRANSISTOR DRAM TECHNOLOGIES, PhD thesis, Department of Electrical Engineering, Stanford University.
- [4] N. Di Spigna, D. Schinke, S. Jayanti, V. Misra, P. Franzon, IEEE/IFIP 20th International Conference on VLSI and System-on-Chip (VLSI-SoC), pp. 53-58, 2012

Fig. 1: Change in V_{FB} w.r.t pulsed voltage in dual floating gate MOS capacitor with various IMD. Al_2O_3 shows negligible dynamic window, whereas HfO_2 shows narrow dynamic window. Higher dynamic window is observed with $HfAlO$. All the IMD shows excellent non-volatile window.



SpinRAM as a Storage Class Memory

Alexander Shukh^{1*}

¹*Spingate Technology, Minneapolis, MN 55378*

Magnetic random access memory employing a spin torque transfer switching mechanism and magnetic materials with perpendicular anisotropy (STT-MRAM) might replace DRAM in the near future. Existing perpendicular magnetic materials suggest that STT-MRAM can be scaled down to technology node $F=8$ nm. Functional samples of the STT-MRAM with magnetic tunnel junctions (MTJ) of 20-30 nm in diameter were demonstrated recently [1, 2]. The demonstrated STT-MRAMs have 1T-1MTJ cell design and cell size predetermined by area of the selection transistor that can be about $6F^2$. The STT-MRAM has a density and endurance problems which are limited by a selection transistor and high density of a spin-polarized current, respectively. Furthermore, there is an issue with an error rate.

The above problems can be solved by using proposed SpinRAM technology [3-5]. The SpinRAM employs a hybrid write mechanism and 1T-nMTJ cell design. The hybrid write mechanism utilizes a simultaneous application to MTJ of the spin-polarized current and bias magnetic field directed along a hard magnetic axis of a free layer. The schematic view of the memory cell employing the hybrid write is shown in Fig.1. Use of the bias current cannot cause an increase of the write energy per bit due to a reduction of the spin-polarized current and possibility to write simultaneously to several MTJs located along a biased line. Moreover, the hybrid write mechanism can provide a substantial error rate reduction.

Fig.2 illustrates a schematic view of the 2D SpinRAM. It has a crossbar architecture with selection transistors located along a perimeter of MTJ array. This architecture provides the cell size of $4F^2$. The transistors can be built with larger technology node than that of the MTJs to prevent their saturation during writing. The SpinRAM can be easily arranged into 3D-architecture. The 3D SpinRAM can effectively compete with NAND flash and hard disk drives (HDD) for enterprise applications in density and price/bit. For example, the enterprise HDD areal density of 500 Gb/in² can be achieved by 2D SpinRAM built with the technology node $F=18$ nm. The 3D SpinRAM can provide the same density using two layers of MTJs with $F=25$ nm. Number of the MTJ layers can be reduced twice by using multi-bit perpendicular MTJ [6]. The SpinRAM represents a novel type of storage class memories.

References

- [1] M. Gajek, J.J.Nowak, J.Z.Sun, P.L.Trouiloud, E.J.O'Sullivan, D.W. Abraham, M.C.Gaidis, G.Hu, S. Brown, Y.Zhu, R.P.Robertazzi, W.J.Gallagher, D.C.Worledge, Appl.Phys.Letters 100, 132408 (2012).
- [2] E.Kitagawa, S.Kashiwada, M.Yakabe, C.Kamata, T.Ouchiai, Y.Kato, T.Daibou, N.Shimomura, J.Ito, H. Yoda, Abstracts of 12th Joint MMM-INTERMAG Conference, FF-02 (2013).
- [3] A.M. Shukh, Patent No. US 8,406,041 (2013).
- [4] T.A.Agan, A.M.Shukh, Patent Application Publication No. US 2012/0281465 (2012).
- [6] A.M.Shukh, Patent No. US 8,331,141 (2012).

* Corresponding author: email: ams@spingatetech.com

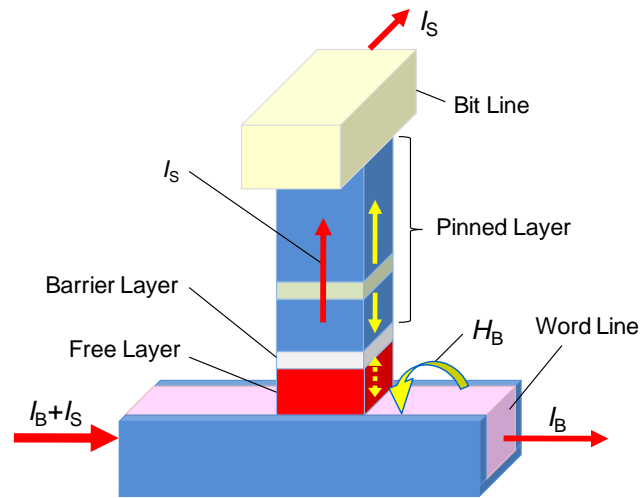


Fig.1. Schematic view of a perpendicular MTJ with a hybrid write mechanism.

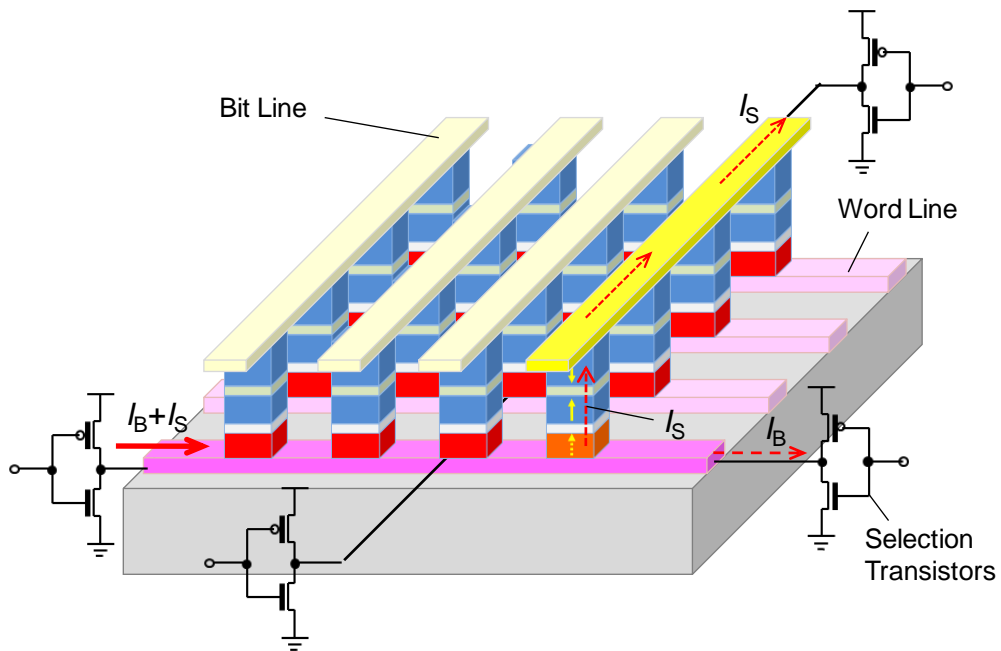


Fig.2. Schematic view of 2D SpinRAM employing the hybrid write mechanism.

Tuning the Néel Temperature of Magnetoelectric Chromium Oxide for Voltage-Controlled Spintronics

M. Street^{*}, Ch. Binek

¹*Electrical and Computer Engineering Department, University of Minnesota, 200
Union Street SE, Minneapolis, MN 55455*

²XXX

*Department of Physics and Astronomy and Nebraska Center for Materials and
Nanoscience, Jorgensen Hall, University of Nebraska-Lincoln, Lincoln, Nebraska
68588, USA*

This research is part of an effort to utilize voltage-controlled boundary magnetization in the magnetoelectric (ME) antiferromagnetic (AFM) material Cr₂O₃ for voltage-controlled ultra-low power nonvolatile magnetic random access memories and spintronic device applications with memory and logical functionality. We exploit the electric switchable interface magnetic moment of magnetoelectric antiferromagnets [1,2]. The net magnetic moment at the interface can be useful to electrically manipulate the magnetic states of an adjacent exchange-coupled ferromagnetic (FM) material [1]. Using a FM Pd/Co multilayer deposited on the (0001) surface of Cr₂O₃, reversible, room-temperature isothermal switching of the exchange bias field between positive and negative values by reversing the electric field while maintaining a permanent magnetic field has been achieved [1]. This FM layer acts as the state variable in a discrete logical system. However, to use voltage-controlled boundary magnetization as a key spintronic material for devices operating at room temperature, the Néel temperature T_N of the magnetoelectric antiferromagnet must be increased substantially above the bulk value of $T_N=307$ K of pure Cr₂O₃. First principles calculations show that substitutional boron doping of Cr₂O₃ can increase T_N by roughly 10% per 1% O site substitution by B [3]. From this, we will attempt to boron dope Cr₂O₃ samples via a gaseous molecular decaborane (B₁₀H₁₄) background atmosphere. In this poster, we diagram the characterization of pure chromium oxide grown on sapphire (0001) via pulsed laser deposition (PLD). In addition we present results of our preparatory investigations which explore the variation of the structural and magnetic properties of Cr₂O₃ on doping with Al₂O₃ such as T_N reduction and increase of the spin-flop field before ultimately focusing on boron doping.

^{*}Corresponding author: email: mstreet@huskers.unl.edu

References

- [1] Xi He, Y. Wang, N. Wu, A. N. Caruso, E. Vescovo, K. D. Belashchenko, P. A. Dowben, Ch. Binek, Nature Materials 9 (2010) 579-585
- [2] P. Borisov, A. Hochstrat, Xi Chen, W. Kleemann, Ch. Binek, Phys. Rev. Lett. 94 (2005) 117203
- [3] S. Mu, A. L. Wysocki, K. D. Belashchenko, Phys. Rev. B 87 (2013) 054435

Logic-in-memory based Big-data Computing by Nonvolatile Domain-wall Nanowire Devices

Yuhao Wang, and Hao Yu*

*School of Electrical and Electronic Engineering
Nanyang Technological University, Singapore 639798*

Domain-wall nanowire, also known as racetrack memory [1], is a newly introduced non-volatile memory device in which multiple bits of information are stored in single ferromagnetic nanowire. Shown in Fig. 1(a), each bit is denoted by the magnetization direction, and adjacent bits are separated by domain walls. The magnetization in the domains can be altered or detected at sandwich-like magnetic tunneling junction. By applying a current through the shift port at the two ends of the nanowire, the domain walls are able to move left or right while the bits in the domains are preserved.

In this paper, domain-wall nanowire device is studied for a non-volatile memory-based big-data computing platform, where all three parts, general purpose logic, special logic and data storage are all implemented by domain-wall nanowire devices. Specifically, reconfigurable general purpose logic is implemented by non-volatile look-up table (LUT); special logic like shift or XOR, shown in Fig. 2(a), exploits the nature of domain-wall devices and is attainable by the proposed architecture.

Evaluation and validation of the proposed platform is in twofold. Firstly, a compact domain-wall nanowire circuit-level behavior model is developed with SPICE-level accuracy [2] and is implemented as a SPICE-like simulator nvmspace [3], which enables device level transient analysis for accurate special logic performance evaluation. Secondly, the circuit and system level model for domain wall nanowire based memory are provided for the performance evaluation of LUT based general logic as well as XOR based special logic. Our experiment results show that 90% leakage reduction can be achieved by the non-volatile domain-wall nanowire based big-data computing platform.

References

- [1] S. S. Parkin and et.al., Magnetic domain-wall racetrack memory, *Science*, 2008
- [2] Y. Shang, W. Fei, and H. Yu, Analysis and Modeling of Internal State Variables for Dynamic Effects of Nonvolatile Memory Devices, *TCAS-I*, vol.59, no.9, pp1906-1918, September 2012
- [3] NVMSpace-SPICE for Non-volatile memory. [online] Available: <http://www.nvmspace.org>

* Corresponding author: email: haoyu@ntu.edu.sg

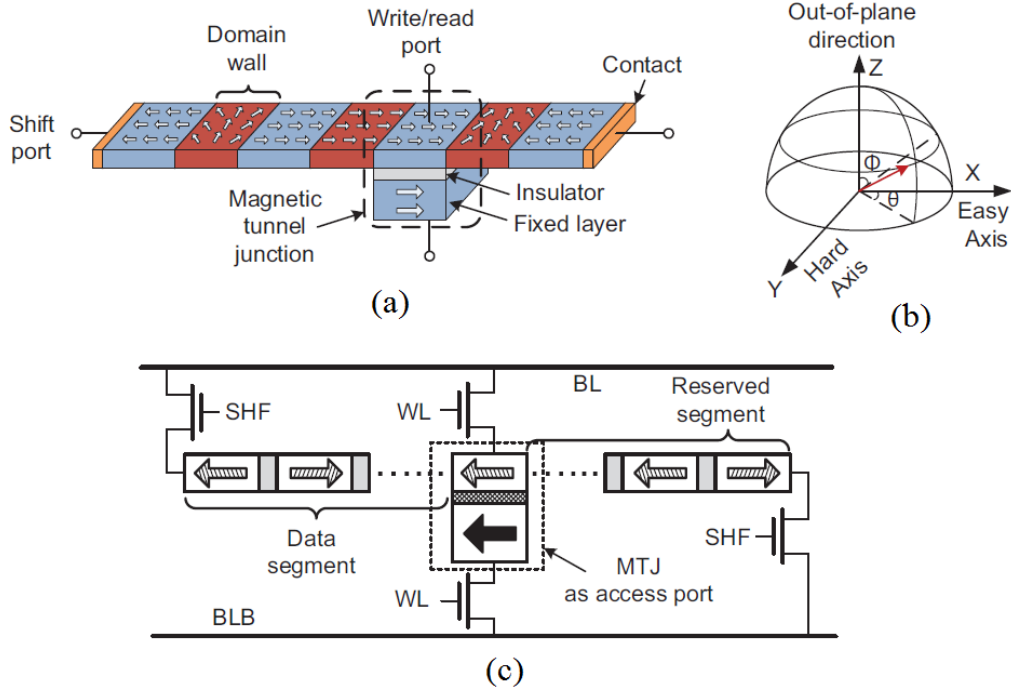


Figure 1. (a) the schematic of domain-wall nanowire structure with access port and shift port (b) magnetization of free-layer in spherical coordinates with defined magnetization angles for SPICE-level modeling (c) the domain wall nanowire based memory macro-cell in the LUT array

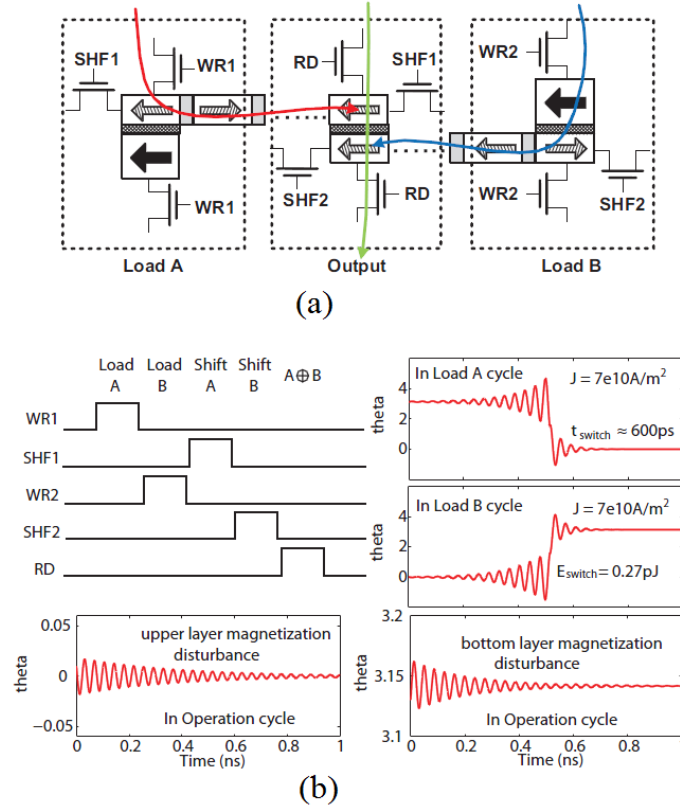


Figure 2. (a) the proposed XOR-logic based on two domain wall nanowires (b) the timing diagram and transient analysis of the constructed logic by nvm-spice

Growth and Characterization of Magnetoelectric

Fe₂TeO₆ Thin Films

Junlei Wang¹, J. Colon Santana², N. Wu¹, P.A. Dowben¹, Ch. Binek^{1*}

¹*Department of Physics and Astronomy, Nebraska Center for Materials and Nanoscience, University of Nebraska, Theodore Jorgensen Hall, 855 N 16th St, Lincoln NE 68588*

²*Department of Electrical Engineering, W. Scott Engineering Center, University of Nebraska, Lincoln NE 68588*

Motivated by the prospective of voltage-controlled interface magnetization [1] in future ultra-low power post-CMOS technology, we report on the first success in growth of a functional thin film of the magnetoelectric antiferromagnet Fe₂TeO₆, a representative in a class of materials where dissipationless switching of boundary magnetization is feasible through pure voltage-control. This provides experimental evidence of the theoretical prediction [2] that boundary magnetization is a universal property of magnetoelectric antiferromagnets. Single phased Fe₂TeO₆ powder sample was prepared by solid state reaction. Magnetic characterization of the powder provides initial insights in the critical behavior of the antiferromagnetic to paramagnetic transition. Highly (110) textured Fe₂TeO₆ thin films are grown by pulsed laser deposition. Magnetic DC susceptibility measurements of Fe₂TeO₆ thin film samples reveal antiferromagnetic long-range order and also its in-plane magnetic anisotropy. X-ray photoemission spectroscopy provides evidence for a Te-O termination at the (110) surface. We interpret the unexpected termination in terms of a surface reconstruction. Finally, measurements of X-ray magnetic circular dichroism combined with photoemission electron microscopy (XMCD-PEEM) provide a lower bound to the spin and angular magnetic moment of the surface Fe-ions. Our XMCD-PEEM data reveal the functionality of Fe₂TeO₆ as a magnetoelectric antiferromagnet with voltage-controllable boundary magnetization.

References

- [1] X. He, Y. Wang, N. Wu, A.N. Caruso, E. Vescovo, K.D. Belashchenko, P.A. Dowben, Ch. Binek, *Nature Mater.* **9** (2010) 579.
- [2] K.D. Belashchenko, *Phys. Rev. Lett.* **105** (2010) 147204.

* Corresponding author: email: cbinek@unl.edu

Probing boundary magnetization through exchange bias in heterostructures with competing anisotropy

Yi Wang^{1*}, Christian Binek¹

¹*Department of Physics and Astronomy, University of Nebraska-Lincoln,*

Cr₂O₃ (chromia) is a magnetoelectric antiferromagnet with a bulk T_N of 307 K. It has been utilized for electrically controlled exchange bias (EB) which enables voltage controlled spintronic applications such as non-volatile ultra-low power MRAM devices. Electrically controlled EB takes advantage of voltage-controllable boundary magnetization (BM) occurring as a generic property in magnetoelectric single domain antiferromagnets [1]. In the perpendicular Cr₂O₃(0001)/CoPd EB system the EB-field shows an order parameter type T-dependence close to T_N reflecting the T-dependence of the BM. At about 150K a decrease of the EB-field sets in with decreasing temperature suggesting canting of the BM. To evidence this mechanism we use EB as a probe. Specifically, we investigate EB in Permalloy(5nm)/ (0001)Cr₂O₃ (100nm) with Permalloy and chromia having competing anisotropies. We measure easy axis magnetic hysteresis loops via longitudinal magneto-optical Kerr effect for various temperatures after perpendicular and in-plane magnetic field-cooling. The T-dependence of the EB field supports the canting mechanism. In addition to the all thin film EB system, we explore a Permalloy(10nm)/Cr₂O₃(0001 single crystal) heterostructure where magnetoelectric annealing allows selecting Cr₂O₃ single domain states. Here the effect of T-dependent canting of the BM is compared with findings in the complementary perpendicular EB system. Understanding the T-dependence of BM is critical for the development of chromia based ultra-low power MRAMs where dissipationless writing of high/low resistance states of a perpendicular magnetic tunnel junction is envisioned.

References

- [1] Xi He, et al., Nature Material. **9**, 579-585 (2010)

* Corresponding author: email: wang.yi@huskers.unl.edu

Characteristics of MONOS Nonvolatile Memory with High- k LaYON as Charge Storage Layer

J. P. Xu^{1*}, L. Liu¹, J. X. Chen¹, P. T. Lai²

¹*School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, People's Republic of China*

²*Department of Electrical & Electronic Engineering, the University of Hong Kong, Pokfulam Road, Hong Kong*

The challenges for nonvolatile MONOS memory are achieving high program/erase (P/E) speeds at low operating voltage, large memory window, good endurance and 10-year data retention simultaneously. Since high- κ dielectrics as charge storage layer (CSL) trap electrons in spatially isolated energy levels and possess discrete traps, the use of high- k films could improve the memory characteristics [1]. In this work, two stacked gate structures are fabricated, with 3-nm thermal SiO₂ as tunneling layer, 10-nm high- k LaYON or LaYO as CSL (deposited by reactive co-sputtering of La₂O₃ and Y targets in Ar/N₂/O₂ or Ar/O₂ ambient respectively), 12-nm Al₂O₃ as blocking layer (deposited by ALD method), and Al evaporated as gate electrode, to investigate properties of LaYON and LaYO as the CSL of MONOS memory devices.

Experimental results in Fig. 1 indicate that the stacked gate structure with LaYON CSL exhibits a large memory window of 5.1 V, 5.0 V, 4.5 V and 3.6 V at P/E voltages of ± 15 V, ± 12 V, ± 10 V and ± 8 V, respectively. The window becomes 3.5 V, 3.0 V, 1.8 V and 0.5 V under the same P/E voltages for the device with LaYO CSL. The better program characteristics of the device with LaYON as CSL are ascribed to nitrogen incorporation in the CSL which leads to higher density of traps with deeper levels [2] and thus higher trapping efficiency. Moreover, the nitrogen incorporation near the LaYON/SiO₂ interface could effectively block the inter-diffusions of Si, O, La and Y atoms and give a stable LaYON/SiO₂ interface [3], thus reducing the interface traps and enhancing the efficiency of the trapped electrons in CSL tunneling back to the substrate under a negative voltage, and giving rise to better erase characteristics. The introduction of Y and N into La₂O₃ can increase its permittivity [4], resulting in a higher electric field across the SiO₂ under an operating voltage, and thus the higher program/erase speeds for the device with LaYON as CSL, as shown in Fig. 2(a). Compared with the device with LaYO CSL, the device with LaYON CSL can achieve better endurance properties with a memory window of 4.5 V after 10⁵ P/E cycles at ± 12 V for 100 μ s/1 ms and improved retention characteristics with an extrapolated 10-year memory window of 4.0 V after removing 1-ms P/E voltages of ± 12 V, as shown in Figs. 2(b) and 2(c), which is probably due to the stronger La-N and Y-N bonds, more stable atomic structure and less traps near/at the LaYON/SiO₂ interface in the device with LaYON CSL. Therefore, LaYON dielectric is a potential candidate as the CSL of MONOS non-volatile memory devices.

* Corresponding author: email: jpxu@mail.hust.edu.cn

References

- [1] Wang Y. Q., Gao D. Y., Hwang W. S., Shen C., Zhang G., Samudra G., Yeo Y. C., IEEE IEDM Tech. Dig. (2006) 1-4.
- [2] S. T. Chang, N. M. Johnson, S. A. Lyon, Appl. Phys. Lett. 44 (1984) 316.
- [3] T. M. Pan, S. J. Hou, C. H. Wang, J. Appl. Phys. 103 (2008) 124105.
- [4] Zhao Yi, Kita K., Kyuno Kentaro, Toriumi Akira, IEEE ICSICT-2006 (2007) 427.

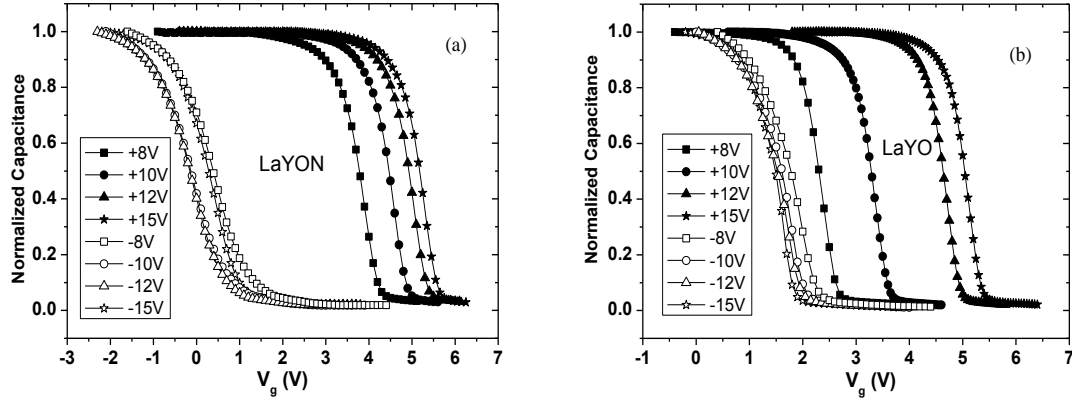


Fig. 1 C-V curves of the two devices with LaYON (a) and LaYO (b) as CSL at different P/E voltages for 1 s.

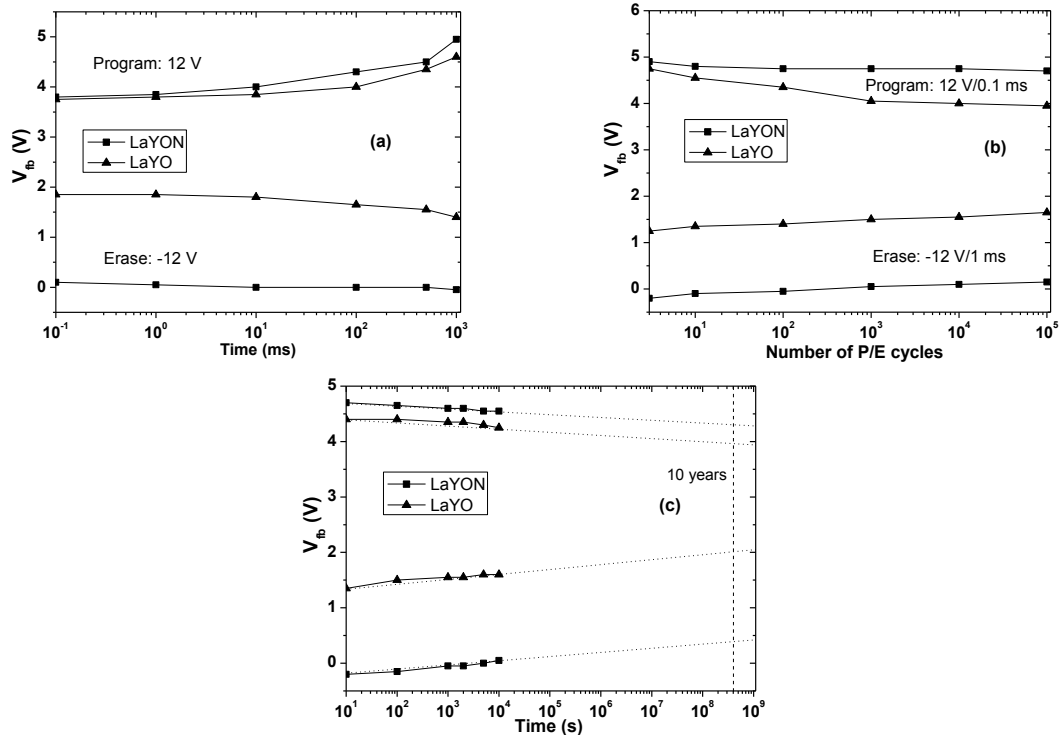


Fig. 2 Change of flat-band voltage V_{fb} with P/E time at P/E voltage of ± 12 V (a), endurance characteristics with P/E of each cycle performed at ± 12 V for 100 μ s/1 ms (b) and retention characteristics after removing 1 ms P/E voltages of ± 12 V (c) for the two devices.

Voltage-Time Invariance in Nanometallic RRAM

Xiang Yang¹, Byung Joon Choi¹, Albert B. K. Chen¹, I-Wei Chen^{1*}

¹*Department of Materials Science and Engineering, University of Pennsylvania
3231 Walnut Street, Philadelphia, PA 19104-6272*

Nanometallic RRAM (**Figure 1**) is a recently developed digital memory which implements information storage by tuning electron localization length through a trapping/detrapping process [1]. Nanometallic RRAM is typically composed of an amorphous insulating matrix and atomically dispersed metals with optional metal inclusions, and it exhibits superior memory properties such as >10 year retention [2-4], >10⁵ cycle endurance, <1 μ W power operation [5], multi-level switching [6], and extreme uniformity [2]. The lack of ionic participation in nanometallic switching is already evident from the small current/voltage responses [7]. In this work, we present threshold (set/reset) voltage data to further distinguish nanometallic RRAMs from typical ionic/filamentary RRAMs: they are independent of temperature, thickness and metal concentration in nanometallic RRAM—but not in other RRAMs. We also demonstrate that, in small area (2 \times 2 μ m²) devices, the threshold voltage is an intrinsic property independent of pulse width ranging from 1 s to 20 ns (**Figure 2**). This is in sharp contrast with the reports on other RRAM in which the switching voltage typically increases by many folds when the switching time decreases from 1 μ s to 1 ns. These results lead us to conclude that nanometallic switching proceeds by a purely energy-controlled athermal electronic process, with a critical energy/energy barrier that is insensitive to input power, duration or temperature. More generally, the RC delay of the load resistance and the cell or parasitic capacitance in the circuit sets a lower limit for excitation-voltage's pulse width (**Figure 2**), above which the threshold voltage of nanometallic RRAM remains constant. Such voltage-time invariance is a hallmark feature of nanometallic RRAM, and we believe it should continue to hold from the ns to the ps range if the RC delay of the circuit can be commensurably reduced.

References

- [1] A. B. K. Chen, S. G. Kim, Y. Wang, W.-S. Tung, I-W. Chen, *Nature Nanotech.* 6 (2011) 237-241.
- [2] B. J. Choi, A. B. K. Chen, X. Yang, I-W. Chen, *Adv. Mater.* 23 (2011) 3847-3852.
- [3] A. B. K. Chen, B. J. Choi, X. Yang, I-W. Chen, *Adv. Funct. Mater.* 22 (2012) 546-554.
- [4] X. Yang, B. J. Choi, A. B. K. Chen, I-W. Chen, *ACS Nano* 7 (2013) 2302-2311.
- [5] X. Yang, I-W. Chen, *Sci. Rep.* 2 (2012) 744.
- [6] X. Yang, A. B. K. Chen, B. J. Choi, I-W. Chen, *Appl. Phys. Lett.* 102 (2013) 043502.
- [7] B. J. Choi, I-W. Chen, *Appl. Phys. A.* (2003) DOI: 10.1007/s00339-013-7776-2.

* Corresponding author: email: iweichen@seas.upenn.edu

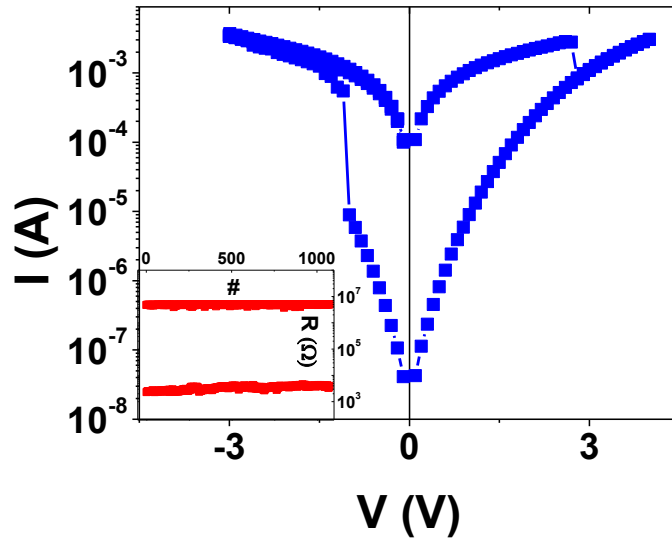


Figure 1. I - V characteristics of Mo/Si₃N₄:Pt/Pt memory. Inset: HRS and LRS resistance values for consecutive 1,000 pulse-switching cycles.

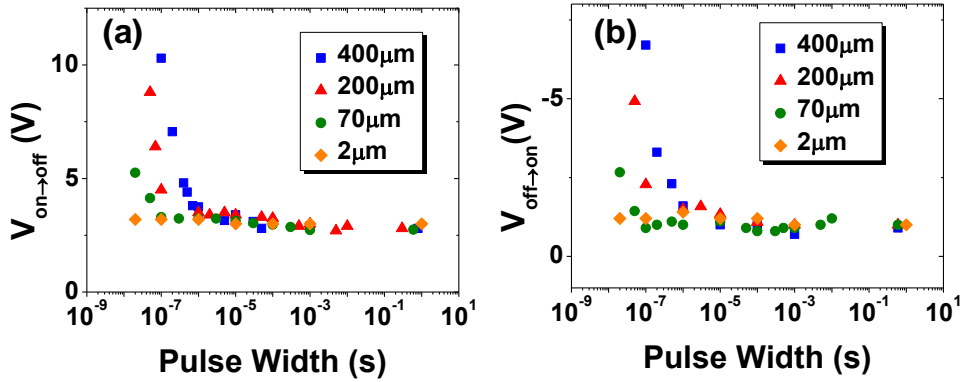


Figure 2. (a) Threshold voltage of square-shaped pulse required for switching, $V_{\text{on} \rightarrow \text{off}}$, vs. (square-shaped) pulse width. (b) $V_{\text{off} \rightarrow \text{on}}$ vs. (square-shaped) pulse width for devices of various lateral sizes.

Structural variety of amorphous GeTe ultrathin films

N. N. Yu^{1,2}, H. Tong^{1,2}, X. S. Miao^{1,2*}

¹ School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, China

² Wuhan National Laboratory for Optoelectronics, Wuhan 430074, China

We demonstrate the drastic effect of film thickness on the local order of Ge sites in amorphous GeTe (a-GeTe) thin films by Surface Enhanced Raman scattering study [1]. The relative intensity of the two prominent peaks around 125cm⁻¹ and 160cm⁻¹ changes greatly along with the film thickness decreased from 100nm to 3nm [2]. We suggest that this change originates from the variation of the fraction of Ge sites in two different environments, namely, tetrahedral- and defective octahedral-like sites [3]. *Ab initio* Molecular Dynamics simulations are performed to show the structural difference between bulk a-GeTe and a-GeTe ultrathin film. Comparison of the local order parameter [4] for Ge atoms of the two models indicates that more Ge atoms are tetrahedrally coordinated in ultrathin film, which is consistent with the experimental observation of Raman spectroscopy.

Unlike the structure of amorphous bulk model having configurations of many octahedral-like Ge sites, which recall the local environment of crystalline GeTe, the presence of substantial Ge atoms in tetrahedral coordination in amorphous GeTe ultrathin film illustrates the larger difference of local order with the rhombohedra structure of crystalline phase. This may give a microscopic explanation of the ultimate limit of the fast phase transition due to the increased crystallization temperature for ultrathin films of phase change materials [5] and gives insights on the development of materials showing potential of scalability.

References

- [1] M. C. Lin, L. W. Nien, C. H. Chen, C. W. Lee and M. J. Chen, “Surface enhanced Raman scattering and localized surface plasmon resonance of nanoscale ultrathin films prepared by atomic layer deposition”, *Appl. Phys. Lett.* 101, 023112 (2012).
- [2] K. S. Andrikopoulos, S. N. Yannopoulos, G. A. Voyiatzis, A. V. Kolobov, M. Ribes and J. Tominaga, “Raman scattering study of the a-GeTe structure and possible mechanism for the amorphous to crystal transition”, *J. Phys.: Condens. Matter.* 18, 965 (2006).
- [3] R. Mazzarello, S. Caravati, S. A. Uverti, M. Baernasconi and M. Parrinello, “Signature of tetrahedral Ge in the Raman spectrum of amorphous phase-change materials”, *Phys. Rev. Lett.* 104, 085503 (2010).
- [4] S. Caravati, M. Bernasconi, T. D. Kuhne, M. Krack and M. Parrinello, “Coexistence of tetrahedral- and octahedral-like sites in amorphous phase change materials”, *Appl. Phys. Lett.* 91, 171906 (2007).
- [5] S. Raoux, J. L. Jordan-Sweet, A. J. Kellock, “Crystallization properties of ultrathin phase change films”, *J. Appl. Phys.* 103, 114310 (2008).

* Corresponding author: email: miaoxs@hust.edu.cn

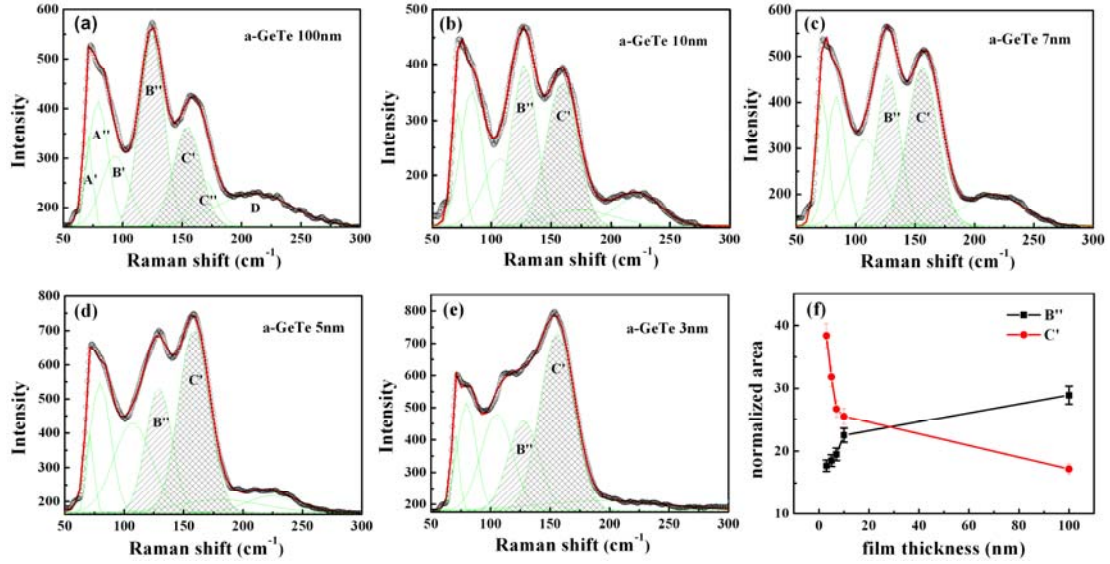


Fig. 1. The Raman spectra (open symbols) of a-GeTe films with different thickness: (a) 100nm, (b) 10nm, (c) 7nm, (d) 5nm, (e) 3nm. A representative fitting (lines) with 7 Gaussian bands to resolve the fine structure, the area of B'' and C' peaks are denoted by oblique and crossline shadow, respectively. (f) The normalized area of peak B'' and C' as a function of film thickness.

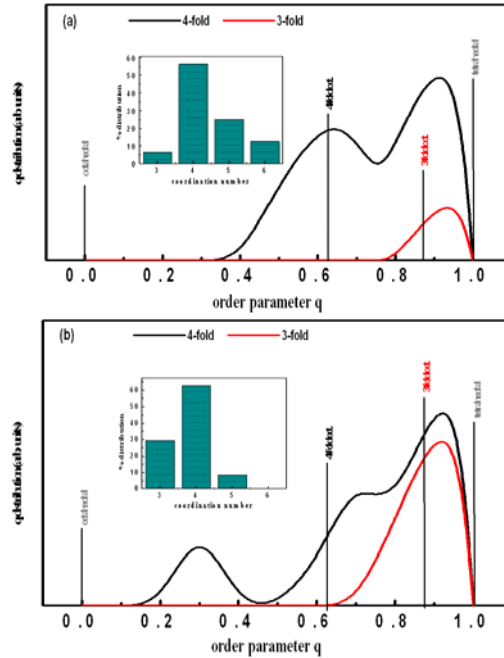


Fig. 2. Distribution of the local order parameter q for Ge atoms with different coordination (4-fold and 3-fold coordinated) of a-GeTe bulk (a) and ultrathin (b) model. Insets in (a) and (b) are the coordination number distributions of Ge atoms of each model.

A super low variable cost Flash Translation

Layer for NAND Flash memory

Zhiyong Zhang¹, Yu Zong²

¹*Beijing Microelectronic Technology Institute, Beijing, China*
zhiy66@163.com

²*Beijing Microelectronic Technology Institute, Beijing, China*
zongyv@sina.com

Flash memory has been widely used in mobile and embedded systems because of non-volatility, low power consumption, shock resistance, lightweight, small size, and fast access speed. However, flash memory has two disadvantages. One is that data cannot be overwritten before erase in advance. The other is that each erasable unit of flash memory has the limitation of possible number of erase operations: generally 100,000 program/erase cycles. So in NAND Flash-based storage systems, an intermediate software layer called a Flash Translation Layer (FTL) is usually employed to hide the erase-before-write characteristic of NAND Flash memory. This paper presents a novel Flash Translation Layer that is specially designed for embedded mass storage systems based on Multi-Level Cell NAND Flash memory, but which have very variable capacity. For example, in some systems based on 8-bits MCU, such as MCS-8051, the internal RAM resource is so inadequate which has only 256 bytes that it can't afford the traditional FTL algorithm.

Keywords – FTL; Low variable cost; NAND Flash;

Simulation study on the information storage mechanism of STT-MRAM

Hu Zuoqi^{*}, Liang Wen, Xu Jian, Yu Fafa, Cao Hua, Lu Jingjing, Miao Xiangshui
*School of Optical and Electronic Information,
Huazhong University of Science and Technology, Wuhan 430074, China*

Spin transfer torque magnetic random access memory(STT-MRAM) [1-3] is a new type of memory that reversing the magnetic moment of nano-magnet by spin-polarized current directly to realize data storage. Based on the LLGS equation [4, 5], the information storage mechanism of STT-MRAM is studied, and the precession reversal of the magnetic moment in the free layer of magnetic tunnel junction(MTJ) is simulated in this paper. As simulation results clearly showed, the time needed to reverse the magnetic moment, the current density and the magnetic moment's motion track are influenced by the saturation magnetization, thickness, shape and damping of the free layer. Under the condition of reasonable parameter values, the writing time can be controlled in the range of 1~5 ns, while the programming current density at the level of 10^6 A/cm².

References

- [1] E. Chen, D. Apalkov, Z. Diao, A. Driskill-Smith, D. Druist, D. Lottis, V. Nikitin, X. Tang, S. Watts, S. Wang, IEEE. Magnet. 46(2010) 1873-1878.
- [2] Y. Xie, IEEE. Design & Test. 28(2011) 44-51.
- [3] S. Natarajan, S. Chung, L. Paris, A. Keshavarzi, Solid-State Circuits Magazine, IEEE 1(2009) 34-44.
- [4] D. V. Berkov, J. Miltat, J. Magn. Magn. Mater. 320(2008) 1238-1259.
- [5] G. Consolo, G. Gubbiotti, L. Giovannini, R. Zivieri, Appl. Math. Comput. 217(2011) 8204-8215.

^{*} Corresponding author: email:hu_zuoqi@mail.hust.edu.cn

The magnetic properties of perpendicular exchange coupled composite $L1_0$ -FePt/[Co/Ni]_N films

Bin Ma^{1*}, H. H. Guo¹, H. G. Chu¹, Z. Z. Zhang¹, Q. Y. Jin¹, H. Wang², and J. P. Wang²

¹*Department of Optical Science and Engineering, Fudan University, 220 Handan Road, Shanghai 200433, China*

²*Electrical and Computer Engineering Department, University of Minnesota, 200 Union Street SE, Minneapolis, MN 55455, USA*

This is the sample abstract for abstract submission to NVMTS 2013 to be held in Minnesota, USA from Aug 12th- Aug 14th, 2013. Please prepare your abstract in English according to the following guidelines.

Perpendicular exchange coupled composite (ECC) films comprise $L1_0$ -FePt as the hard layer to store the data, and Co based multilayers as the soft layers to assist the magnetization reversal of $L1_0$ -FePt. The $L1_0$ -FePt was firstly deposited on the heated MgO (100) substrate at 500-550 °C, and (001) orientation is revealed by the x-ray diffraction. After it cooling down to room temperature, [Co/Ni]_N was then deposited on FePt. Both easy axes of the hard and soft layers are perpendicular to the film plane, as well as their magnetization. Perpendicular ECC FePt/[Co/Ni]_N films have higher thermal stability than that of FePt/Fe. This is due to the easy axis of Fe layer is in the film plane, and its magnetization tilts from the normal direction without applied field [1]. By insert a thin Pt layer between the FePt and [Co/Ni]_N, magnetization reversal of the composite changes from incoherent rotation to assisted domain-wall motion with the thickness of Co/Ni multilayer increases from 2.4 nm to 8 nm. When the soft layer is thin, the insertion of Pt interlayer can decrease the switching field of the composite by reducing the exchange coupling between FePt and [Co/Ni]₃. However, reduction of the exchange coupling will increase the switching field of FePt/[Co/Ni]₁₀, as it weakens the assistance of the soft layer. In order to prevent the formation of ledge-type ECC structure [2], an Ag interlayer is inserted in the $L1_0$ -FePt layer. Well isolated grain structure is observed for all [FePt-Ag]/[Co/Ni]_N films with N varied from 3 to 30, and the average grain size keeps constant.

References

- [1] D. Suess, J. Lee, J. Fidler, T. Schrefl, Magn. Magn. Mater., 321, 545 (2009).
- [2] T. P. Nolan, B. F. Valcu, H. J. Richter, IEEE Trans. Magn., 47, 63 (2011).

* Corresponding author: email: magnmb@fudan.edu.cn