Thermo-piezoelectric Si$_3$N$_4$ cantilever array on CMOS circuit for high density probe-based data storage

Young-Sik Kim$^a$*, Seongsoo Jang$^a$, Caroline Sunyong Lee$^b$, Won-Hyeog Jin$^a$, II-Joo Cho$^a$, Man-Hyo Ha$^a$, Hyo-Jin Nam$^a$, Jong-Uk Bu$^a$, Sun-II Chang$^c$, Euisik Yoon$^c$

$^a$ Microsystem Group, Device & Materials Laboratory, LG Electronics Institute of Technology, Seoul, Republic of Korea
$^b$ Hanyang University, Ansan, Republic of Korea
$^c$ University of Minnesota, USA

Received 1 March 2006; received in revised form 15 September 2006; accepted 5 October 2006
Available online 20 November 2006

Abstract

A novel wafer level transfer method of silicon nitride cantilever arrays on a conventional CMOS wafer has been developed for the high density usage of probe based data storage device. The cantilevers are so called thermo-piezoelectric cantilevers consist of poly silicon heaters for writing and piezoelectric sensors for reading. The cantilevers were fabricated with a commercial p-type Si wafer instead of a SOI wafer used for this application before. The wafer level transfer method presented here, consists of only one direct bonding of the wafer with cantilevers and the one with CMOS circuits. Thirty-four by thirty-four array of cantilevers were successfully transferred with this method.

With a thermo-piezoelectric silicon nitride cantilever transferred with this method, 65 nm of data bits were recorded on a PMMA film. We also obtained piezo-electric reading signals from the transferred cantilevers.

© 2006 Elsevier B.V. All rights reserved.

Keywords: Atomic force microscopy; PZT cantilever; Electrical coupling; High speed; PZT actuator; Piezoresistor; Thermo-piezoelectric cantilever; Wafer-level transfer

1. Introduction

Probe-based data storage devices have been studied extensively to overcome the storage density limits of hard disk drives and semiconductor memories [1–5]. Thermo-piezoelectric read/write mechanism where data bits are written with a resistively heated AFM tip and read with a piezoelectric PZT sensor, was suggested as one of the probe-based data storage devices, as shown in Fig. 1(a) [6–8]. During the write cycle, a resistively heated tip can make indentations on a polymer media and during the read cycle, a piezoelectric sensor detects the indentations from the piezoelectrically generated charges while the cantilever bends over the indentations on the polymer media. The generated charges are amplified and converted to voltage signal by the charge amplifier, as shown in Fig. 1(b).

Thermo-piezoelectric read/write system has several advantages over the thermo-mechanical read/write system. First, the power consumption is less. In reading, piezo-electrical sensing uses self-generated charges from the cantilever deflection so that power consumption is negligible while thermo-mechanical sensing detects the resistance variation caused by the temperature change of the heated cantilevers, consuming much power. And as the heated cantilevers scan over the polymer media during the reading cycle of the thermo-mechanical system, the media should withstand the heat and this precludes the use of polymers with low glass-transition temperature ($T_g$), which determines the bit formation temperature as well as the thermal stability of the data bits. The thermo-piezoelectrical system, however, does not have this restriction and can lower the writing power by selecting polymers with low glass-transition temperature.

Second, the electronics is simpler. The thermo-mechanical read system requires additional circuits to compensate the initial resistance difference between cantilevers caused by the process variation. In piezoelectric sensing, such an offset problem does not exist since the initial charge status is all the same for each can-
Fig. 1. Principle of PZT sensing of thermo-piezoelectric cantilever: (a) reading mechanism of a thermo-piezoelectric Si$_3$N$_4$ cantilever. (b) Self-generated charge in PZT sensor is collected to feedback capacitor (Cf) by charge amplifier and is converted to voltage.

tilever. Finally, the reading speed can be faster with piezoelectric sensor than thermal sensor since the charges are generated within nanoseconds while a few microseconds are needed to heat the cantilever.

A piezoresistive sensor can be another choice, but the sensitivity of the thermal sensor is better than that of the piezoresistive sensor because thermal effects in semiconductors are stronger than strain effects. Vettiger et al. reported that $\Delta R/R$ sensitivity of about $10^{-5}$ nm$^{-1}$ has been achieved with a thermal sensor whereas conventional piezoresistive cantilevers have sensitivity about $10^{-6}$ nm$^{-1}$ [1,2].

For the high density probe-based data storage applications, cantilevers should act in arrays. The cantilevers should be uniform in thickness and stress so that the initial bending and the spring constant of them, which determines the pressing force of the tip on the polymer media, have minimal variation. And the cantilevers can be integrated with ASIC circuit which accesses the individual cantilever for read/write and control. And after the integration of the cantilevers with the ASIC circuit, the tips on the cantilevers can be contacted with the media.

Previously, Vettiger et al. proposed a new micro-device transfer/interconnect method (DTM) compatible with the BEOL CMOS technology. However, this technique consists of two bonding processes; in the first step, cantilevers are formed out of a SOI wafer and the tips are formed on the surface. These cantilevers are transferred onto a glass wafer and the bulk silicon is removed. In the second step, the cantilevers on the glass wafer are transferred onto the CMOS wafer. The SOI wafer is used to control the thickness of the cantilevers [9,10].

The device silicon layer of the commercial SOI wafers has initial thickness variation and this affects the thickness uniformity of the cantilevers. In our previous studies, silicon nitride cantilevers, integrated with heater tips and piezoelectric sensors, were developed with nitride buried SOI wafer. The uniformity of the initial bending and the mechanical stability of the cantilevers can be improved by using the nitride film [7].

In this research, a novel wafer-level transfer method of two-dimensional cantilever arrays on a conventional CMOS circuit has been developed for the high density probe-based data storage devices. The cantilevers and the tips are formed with silicon nitride on a conventional p-type silicon wafer and poly silicon heaters and piezoelectric sensors are integrated with the cantilevers. With one step bonding process, the cantilevers are directly transferred to the CMOS wafer. Our new fabrication process provides simple wafer level transfer method of uniform and mechanically stable cantilever array.

2. Fabrication

Wafer level transfer of cantilever arrays to the CMOS wafer is explained here.

The CMOS wafer consists of arrays of charge amplifier circuits which amplify the signals from the thermo-piezoelectric cantilevers. The wafer was fabricated with 0.8 μm and 2P2M(2-poly-2-metal) process, provided by a standard CMOS foundry in Electronics and Telecommunications Research Institute (ETRI), Korea.

Fig. 2(a) shows the fabricated CMOS wafer by using 0.8 μm conventional CMOS technology. The circuitry for read and write channel per each cantilever are illustrated in Fig. 2(b). The read channel includes a charge amplifier and a latched comparator per one cantilever and the write channel includes a switch transistor per cantilever. The latched comparator converts analog output signals from the charge amplifier to digital output signals and stores the data signals. Using an array of this circuit, fully parallel reading operation can be achieved. The output signal can be acquired from the stored data signals in latched comparators by a column time-multiplexed addressing scheme similar to those implemented in DRAMs.

![Fig. 2. The fabricated CMOS wafer with Charge amplifier circuitry (a) microscope image of 32×32 cantilever array fabricated in 5 in. wafer. (b) Block diagram of read/write circuit per one cantilever.](image-url)
The wafer-level transfer process of two-dimensional cantilever array on a conventional CMOS wafer is illustrated in Fig. 3. Some of the process steps were adopted from DTM [7,8] and the mould-and-transfer method [11,12].

First, inverted pyramidal pits are formed by KOH anisotropic etching on a single crystal silicon wafer with Si$_3$N$_4$ thin film as a masking layer (Fig. 3I(a)). And 300 nm of thermal oxide is grown for the sharpening the tips. Low pressure chemical vapor deposition (LPCVD) Si$_3$N$_4$ thin film is deposited for the tips and cantilevers (Fig. 3I(b)). Si$_3$N$_4$ thin film formed by LPCVD method has superior thickness uniformity and mechanical stability compared to the device silicon layer of a SOI wafer. It is noted that the uniformly formed tips are directed opposite to the wafer surface. On the silicon nitride film, 300 nm of LPCVD poly silicon film are grown and patterned to form the heaters (Fig. 3I(c)). Phosphorus is implanted with a dose of $5 \times 10^{14} \text{ cm}^{-2}$ at the heater region and with $1 \times 10^{16} \text{ cm}^{-2}$ at the electric contact region of the poly silicon, both at the energy of 70 keV. Then, the wafer is subjected to a furnace annealing in N$_2$ ambient at 900°C for 30 min.

LPCVD oxide film of 200 nm thick is deposited over the patterned wafer to prohibit the inter-diffusion between PZT and silicon layer. And PZT capacitors are formed as described in the previous works [6–8].

The bottom electrodes are formed by sputtering of thin titanium (Ti) adhesion layer followed by a 120 nm of platinum (Pt) layer. The PZT layer is formed by sol–gel process. The PZT film is annealed at 650°C for 1 min using the rapid thermal annealing (RTA) process. The resulting PZT film is 300 nm thick and its composition is near the morphotropic phase boundary. On the top of the PZT film, RuO$_2$ film is sputter-deposited as the top electrode. The PZT sensor and cantilever structure are patterned using an inductively coupled plasma reactive ion etching system and a reactive ion etching system, respectively (Fig. 3I(d)).

For the electrical connection to the CMOS wafer, bumps are formed by e-beam evaporation and lift-off process. The bump layer consists of a pad layer of Ti (50 nm)/Pt (200 nm)/Au (200 nm) stack and 3 μm thick Au:Sn (80:20) layer which will be eutectically bonded to the CMOS wafer. At this stage the cantilever arrays are ready to be transferred.
On the CMOS wafer, Metal 3 layer (Fig. 3II) of Ti (20 nm)/Pt (100 nm)/Au (300 nm) stack is patterned with lift-off process. The Metal 3 layer acts as the platform for the eutectic bonding process. Using this layer, Metal 2 (Fig. 3II, Al) of the CMOS wafer and bumps on the cantilever wafer are electrically connected.

And then, 2 µm of photosensitive polyimide layer is spun and patterned and cured (Fig. 3II). Then the cantilever array part and the CMOS part are assembled (Fig. 3III(a)) using the wafer level bonding method. The two wafers are pressed with 10 bar at 300 °C for 20 min for the eutectic bonding of Au:Sn.

After the wafer-level bonding the sacrificial silicon layer (Fig. 3III(a)) is grinded to about 50 µm and then etched away with XeF$_2$ gas with the thermal oxide at the bottom of the cantilevers as the etch stop layer (Fig. 3III(b)).

Finally, oxide at the bottom of the tip is selectively removed in BOE and polyimide is removed in O$_2$ plasma (Fig. 3 III(c)).

3. Results and discussion

Thirty-four by thirty-four thermo-piezoelectric Si$_3$N$_4$ cantilever array was successfully transferred on a CMOS wafer by the wafer level transfer-method mentioned above. The outermost two rows and columns of the array are sacrificial cantilevers to guarantee identical fabrication environment for the 32 × 32 active cantilevers. With these dummy cantilevers, the fabrication yield can be increased.

Fig. 4 shows the transferred cantilever arrays on a CMOS wafer after the bonding and removing of the sacrificial silicon. Each array contains 1024 cantilevers. Integration density is 100 cantilevers/mm$^2$ and 300 electrical interconnects/mm$^2$ were made within a cantilever array (3.4 mm × 3.4 mm). The tips are protected until the last step so that they remain sharp through this wafer level bonding process. The electrical contact resistance is well below 0.5 Ω. Die-shear test has been performed to check the durability of the wafer level bonding. The die shear strength of the bumps was 2–5 kg f/mm$^2$ and this is well above the internationally accepted IC industry’s standard of 1 kg f/mm$^2$.

The inserted figure is an enlarged view of the free standing cantilevers with PZT sensors for reading and silicon nitride tips with poly-Si heater for writing data bits. The cantilever is typically 70 µm long and 45 µm wide and 300 nm thick.

Fig. 5(a) is a slanted view of the transferred cantilevers in Fig. 4. Fig. 5(b) is a closed view of one of the free-standing cantilevers. The cantilevers are bonded to the CMOS wafer with a gap of about 2.25 µm and they are tilted upward by about 1.8°. One side of the pyramidal tip is 5 µm and the tip height is about 3.5 µm.

The size of the tips determines the thermal mass of the heater and thus the thermal time constant of the system. To reduce the power consumption and to increase the speed of writing the tips should be as small as possible. When the tip becomes smaller the cantilevers needs to be bent to the direction that keeps the distance between the CMOS wafer and the polymer media to avoid the face to face contact of them during the read and write operation.

The bending of the cantilevers can be controlled mainly by adjusting the deposition condition of LPCVD silicon nitride film. The residual tensile stress of the silicon nitride film can
be adjusted from less than 100 MPa to 1.2 GPa by changing the stoichiometry of the film. The initial bending of the cantilevers as well as the height of the tips should be very uniform and be well under control in order to minimize the variation in loading force of all the cantilevers in an array. This is a crucial factor to the read/write characteristics and the wear of the tip and media. Previous investigations on wear problem suggest that the uniformity of the cantilever bending across a whole chip should be less than 500 nm [1,3], when the spring constant of the cantilever is 1–0.5 N/m.

**Fig. 6** shows the deviation of deflection of 60 cantilevers from randomly selected areas out of the 34 × 34 cantilevers array. The standard deviation of the deflection is about 100 nm and the maximum deviation is about 300 nm. With the spring constant of the cantilever being 1 N/m, the deviation of the cantilevers meets the requirements mentioned above. There were some areas where the variation is relatively larger than others. It was observed that in some areas polyimide was not fully removed after the final O₂ plasma ashing as shown in **Fig. 6(b)**. These polyimide residues can contribute the abnormal deflection of cantilevers.

Signals from the piezoelectric charges were successfully recorded with the transferred cantilevers. External charge amplifier circuitry was used instead of the integrated CMOS circuit because the overall system for the measurement has not been

**Fig. 7.** Reading signal when deflected one of transferred cantilever array to 100 nm.

**Fig. 8.** (a) Data bits written by single transferred thermo-piezoelectric Si₃N₄ cantilever and (b) profile of data indentation.
built at this stage. Fig. 7 shows the signals from the charge amplifier when the transferred cantilever in the $34 \times 34$ array deflected by 100 nm.

A series of data bits were written on a PMMA media with one of the cantilevers transferred by the wafer level bonding method, as shown in Fig. 8(a). The data bit indentation is about 5.4 nm deep and has a diameter of 65 nm, as shown in Fig. 8(b). The polymer around the indentation has been piled up to about 3.8 nm above the initial surface. These topographic pile-ups are regions susceptible to wear during the operation. The presence of pile-ups also limits the writing density. However, this phenomenon of polymer pile-up can be used for erasing of written bits [1]. Sills et al. reported that the height of pile-ups was reduced with the use of a modulus-matched buffer layer between the polymer film and the substrate [13].

4. Conclusion

Using the proposed wafer-level transfer technology, $34 \times 34$ thermo-piezoelectric silicon nitride cantilever array on a CMOS circuit was successfully fabricated. This cantilever fabrication method avoids the use of expensive SOI wafers and can finish the integration with the CMOS wafer with only one direct bonding process. So the process scheme is simple and has merits in the cost of ownership.

The initial bending of the cantilevers was very uniform and controllable because the cantilevers were made of silicon nitride film. Piezoelectric reading and thermo-mechanical writing were successful with the transferred cantilevers. Further studies are in progress to read and write data bits using this cantilever array with CMOS control circuit and to build the overall system.

Acknowledgement

This work is supported by “The program for the Development of the Next Generation Ultra-High Density Storage” of the Ministry of Commerce, Industry and Energy.

References