A Low-Power 2.4-GHz Current-Reused Receiver Front-End and Frequency Source for Wireless Sensor Network

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***Abstract*—In this paper, we present a receiver front-end and a frequency source suitable for wireless sensor network applications, in which power consumption is severely restricted under several milliwatts. For such an extremely low-power receiver, current-reusing and frequency multiplying schemes are proposed for both the RF front-end and frequency source. The proposed front-end achieves a conversion gain of 30.5 dB and a noise figure of 10.2 dB at the 10-MHz intermediate frequency (IF), taking only 500-μA bias current from a 1.0-V supply voltage. The measured phase noise of the fabricated frequency source is −115.83 dBc/Hz at 1 MHz offset from a 2.2-GHz center frequency, taking 840 μA from a 0.7-V supply. The front-end performance is compared with the previously reported low-power front-ends operating in similar frequency ranges.**

***Index Terms*—Current-reused technique, flicker noise, frequency multiplier, impedance matching, input matching network, mixer noise, phase noise, pinch-off clipper, receiver front-end, UHF receivers, voltage-controlled oscillators, wireless sensor network.**

I. Introduction

RECENTLY, industrial and medical sectors have drawn wide attention in the research of wireless sensor networks (WSN) for pollution monitoring, biological/chemical detection, breath/heart detection, etc. [1]–[3]. Because a wireless sensor network consists of many distributed and disposable sensor nodes that operate continuously over duration greater than one year with only a single battery, each sensor node requires a highly integrated, low-cost single-chip transceiver with high energy efficiency. Especially, an extremely low-power receiver with a low-supply voltage is indispensable for the purpose of a low-power WSN transceiver, since the receiver should be continuously turned on, waiting for a wake-up signal and receiving data. On the contrary, a transmitter operates for a short moment to transmit data gathered by peripheral sensors, even though the power level required in a transmitter is a higher order of magnitude due to the large distance of several tens of meters between two sensor nodes. To design low-power single-chip receivers, the direct conversion receiver (DCR) architecture has been investigated and widely used in WSN, because DCR is excellent in terms of power efficiency, system integrity, and channel selectivity, which are the major issues in WSN. On the other hand, the super-heterodyne system is not well suited for on-chip integration due to external image-rejection filters. A low-IF receiver also requires good matching for image channel rejection, which is difficult to obtain with small RF devices [4], [5]. Despite much effort in DCR research, however, several factors still remain as problems to be resolved for its use in low-power WSN. The most important one to be considered is the tradeoff between power consumption and system performance such as bit-error rate (BER), sensitivity, and operating frequency. First, power reduction in DCR seriously hampers the receiver performance because of its inherent drawback of high sensitivity to flicker noise and the insufficient gain of the RF front-end. Second, it is not easy to lower the operating frequency below 1 GHz, considering the small antenna size and channel selectivity. However, as the operating frequency is increased, receivers require more and more power to achieve a high gain and sufficiently low noise performance in spite of the reduced ratio of operation frequency to small unity-gain frequency (f_T) of MOSFET. Considering the abovementioned problems, it is very difficult to achieve the required WSN system performance with extremely low power consumption using the DCR architecture.

In this paper, we present a receiver architecture suitable for very low-power WSN application. To address the DCR's own drawbacks such as low gain and high sensitivity to flicker noise, the current-reused folded-cascode front-end is proposed and analyzed. In addition, a low-power frequency source with a differential frequency multiplier is also proposed to reduce power consumption in a voltage-controlled oscillator (VCO) and frequency divider, which consume a major fraction of the overall power and area for a frequency synthesizer.

In Section II, we will briefly describe the receiver characteristics of WSN. In Section III, the circuit topology and operation principles of the proposed frequency multiplier and VCO are presented. In Section IV, we will deal with the proposed current-reused front-end architecture and its characteristics. In Section V, measurement results of the fabricated front-end and frequency source are presented and compared to the previously reported works to verify our proposed concept and circuit topology. Finally, a summary and conclusion follow in Section VI.

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II. System Characteristics

This work focuses on the design of a receiver to be used in indoor environments such as the factory, home, and office. Therefore, RF signal attenuation and scattering as well as free-space loss should be carefully considered to build the link budget because of the many objects that can absorb and reflect RF signals in indoor environments. In this work, a carrier frequency of 2.4-GHz ISM band is chosen considering to use in all parts of Europe and the USA. Therefore, the antenna size in this frequency band can be substantially reduced compared to its size in a low-frequency band below 1 GHz. A relatively low data rate of 100 kb/s and a high BER of 10^{-3} are appropriate for WSN because sensor nodes detect and transmit data of slowly varying physical quantities.

A. Architecture and Modulation Scheme

Several factors must be considered carefully when determining the modulation scheme of WSN: 1) power efficiency, both in the receiver and transmitter; 2) signal quality; and 3) simplicity of the modulation and demodulation circuits. From the viewpoint of the transmitter, nonlinear power amplifiers (PAs) (class-E and class-F) are well suited for high power efficiency [6]. A binary frequency shift keying (BFSK) modulated signal can be easily amplified by such nonlinear PAs with low spectral regrowth in a transmitter. In addition, a BFSK modulation scheme simplifies the modulation and detection circuit complexity. A BFSK signal, which has high demodulated frequencies, can easily circumvent the flicker noise problem of DCR, because a simple high-pass filter can reject low-frequency flicker noise without degrading the transmitted data [7]. For a given BER, a BFSK modulation scheme demands 3 dB higher SNR than binary phase shift keying (BPSK). Nevertheless, BFSK is widely used in low data rate applications, because the BER can be improved by decreasing the data rate [4].

B. Link Budgets and Receiver Specifications

The maximum path losses between two sensor nodes is given by [8]

$$L_{\text{path}}(R) = 10\log\frac{(4\pi)^2 \cdot R^n}{\lambda^2} + L_{\text{atten}} \qquad (1)$$

where R is the maximum distance between two sensor nodes, λ is the wavelength of 2.4 GHz, and n and L_{atten} are the scattering exponent and the attenuation parameter, respectively. The optimum distance between two nodes and the transmission power of PA are determined such that overall power consumption in a multi-hop network is minimized. Assuming that the scattering exponent and attenuation parameter are relatively large values of 4 and 10 dB, respectively, in an indoor application (about 2 and 0 dB in free space) [8], the maximum transmit distance is about 20 m at the PA output power of 10 dBm [9], [10].

To satisfy a BER of 10^{-3} at a 100 kb/s data-rate (or 100 kHz channel BW), the SNR at the noncoherent FSK demodulator should be larger than 11 dB. The noise figure (NF) of the receiver is given by

$$\text{NF (dB)} = \text{P}_{\text{in,min}}\,\text{(dBm)} + 174\,\text{(dBm)} - \text{SNR (dB)} - 10\log_{10}\text{BW} \qquad (2)$$

TABLE I
WSN Specifications

Item	[5]	[11]	This work
Frequency (GHz)	0.433	0.9	2.4
Modulation	BFSK	BFSK	BFSK
Nodes distance	-	30 m	20 m
Transmit power	-	-	10
Data rate (kbps)	20	100	100
Rx sensitivity (dBm)	-100	-80	-90
BER	10^{-3}	10^{-3}	10^{-3}
NF of receiver (dB)	25	25	20

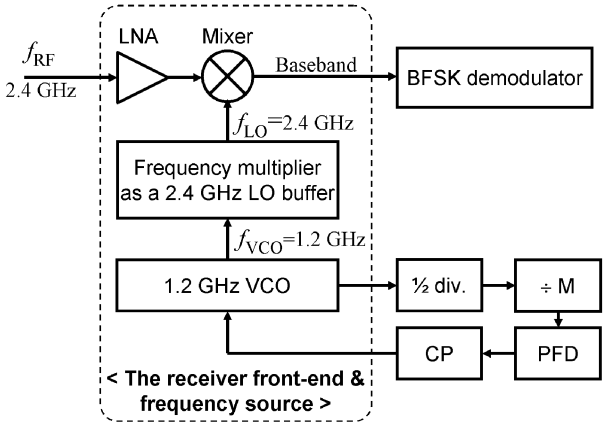


Fig. 1. Receiver architecture suitable for a low-power application. (The dotted line indicates the boundary of the fabricated chip.)

where $\text{P}_{\text{in,min}}$ is the sensitivity of the receiver and 174 dBm is a 50 Ω source resistance noise. Considering the restricted power dissipation under several milliwatts in a receiver, we have determined the receiver sensitivity to be −90 dBm. Therefore, a receiver noise figure of 20 dB is adequate with a 4 dB margin and corresponds to an SNR of 11 dB and a BW of 100 kHz. Table I shows the summary of the specifications of the proposed WSN compared with those of previously reported papers.

III. The Proposed Frequency Source

Fig. 1 shows the proposed receiver architecture to reduce power consumption in the frequency divider and VCO, which are the largest power consumers in UHF receiver. In a conventional DCR architecture, the VCO should operate at the same frequency as the RF signal to directly translate the RF signal into a baseband signal. After all, as the operating frequency goes higher, the power dissipated in a VCO and a frequency divider drastically increases. To address this problem, the VCO operates at half the frequency of the input signal (f_{RF}) applied to the mixer. Then, the frequency multiplier doubles the VCO output frequency (f_{VCO}) to create the same RF frequency for DCR. Therefore, in the frequency source using a VCO with a frequency multiplier, the frequency divider can work only at half of the RF frequency of 2.4 GHz, resulting in great power reduction. Even though the phase noise of the multiplied signal is increased as much as 6 dB compared with its original signal [15], this is not a problem in WSN. This is because WSN can allow poor phase noise performance compared with other wireless protocols such

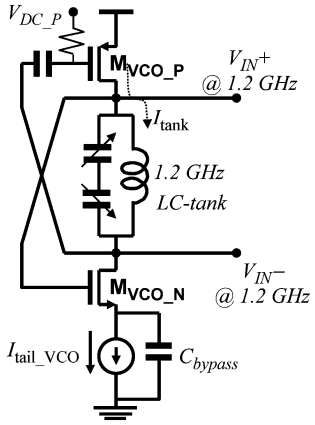


Fig. 2. Circuit implementation of a 1.2-GHz VCO ($M_{VCO_P} = 225/0.18\,\mu$m, $M_{VCO_N} = 225/0.18\,\mu$m, $L = 12$ nH).

as WLAN, CDMA, etc. In addition, the frequency multiplier also plays an important role of a conventional local oscillator (LO) buffer to prevent injection-locking problems. This means that the proposed receiver architecture requires no additional blocks and effectively reduces overall power consumption.

A. Voltage-Controlled Oscillator

While phase noise is considered the most important specification in high data-rate wireless applications such as GSM, CDMA, and WLAN, it is strongly required to design the VCO with maximum oscillation amplitude under a given bias current in low-power WSN applications. This is because the wide-channel spacing of WSN can minimize the reciprocal mixing phenomenon caused by phase noise, and sufficiently large oscillation amplitude should be supplied to the mixer for enough voltage gain of the mixer. Generally, oscillation amplitude ($V_{\rm OSC}$) is given by

$$V_{\rm OSC} = A_1 R_{\rm tank} \tag{3}$$

where $R_{\rm tank}$ is a equivalent parallel resistance of the *LC* tank, and A_1 is the first harmonic coefficient of the periodic current waveform that passes through the *LC* tank [12]. Therefore, the design issue of a low-power VCO is how to maximize the Fourier coefficient for the first harmonic. Under the same average current, making a narrow pulse current with a high peak value is a trivial solution for large oscillation amplitude. Fig. 2 shows the VCO configuration, which has a narrow pulsewidth and high peak value by reducing the conduction angle of the switching MOSFETs [22]. As the gate bias of M_{VCO_P} (V_{DC_P}) increases, a narrow pulse current ($I_{\rm tank}$) can be obtained due to the small conduction angle. Fig. 3 shows the simulated current waveforms of the 1.2-GHz VCO. In spite of only a 500-μA bias current of $I_{\rm tail\_VCO}$, the peak current passing through the *LC* tank is 1.86 mA, which is more than 3 times the bias current. The conduction angle is less than 0.35, which is relatively smaller than conventional VCO topologies. These simulation results ensure that the VCO can achieve larger oscillation amplitude even with only sub-mA bias current.

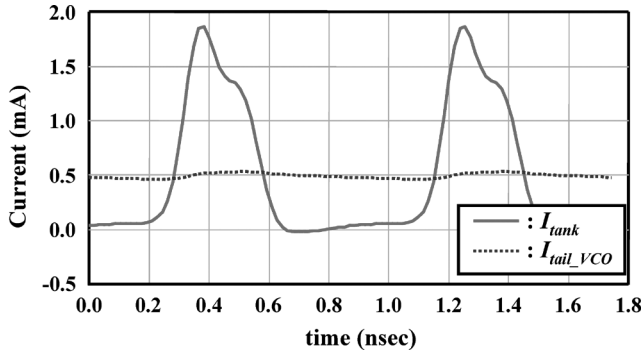
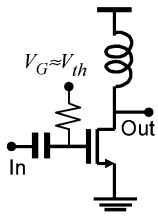


Fig. 3. Simulation result of the proposed VCO.



(a)

In	Harmonics of out	
	1st	2nd
$\sin(\omega_0 t+0)$	$\sin(\omega_0 t+\pi)$	$\sin(2\cdot\omega_0 t+\pi)$
$\sin(\omega_0 t+\pi)$	$\sin(\omega_0 t+0)$	$\sin(2\cdot\omega_0 t+\pi)$
$\sin(\omega_0 t+\pi/2)$	$\sin(\omega_0 t+3\pi/2)$	$\sin(2\cdot\omega_0 t+0)$
$\sin(\omega_0 t+3\pi/2)$	$\sin(\omega_0 t+\pi/2)$	$\sin(2\cdot\omega_0 t+0)$

(b)

Fig. 4. (a) nMOS pinch-off clipper. (b) Phase of first and second harmonic output signals according to input signals.

B. The Proposed Frequency Multiplier

A pinch-off clipper, which is biased such that the gate DC bias (V_G) is set around the threshold voltage ($V_{\rm th}$), is widely used to increase second-order harmonics for frequency doubling, as shown in Fig. 4(a) [13]. Fig. 4(b) shows the phases of the first and second harmonics of the output signals when input signals with different phases are applied to the nMOS pinch-off clipper. Note that the LO buffer (the frequency multiplier in the proposed receiver scheme) should apply differential signals on the switching stage of a single-balanced (SB) mixer to remove RF feedthrough. Referring to Fig. 4(b), we can see that quadrature signals have to be applied to the nMOS pinch-off clipper to make differential output signals [14], [15]. However, to generate quadrature signals from differential VCO output signals, additional circuits such as a passive poly-phase filter or an active g_m-*C* filter should be employed between the VCO and frequency multiplier. But this is not desirable for low-power application because a passive poly-phase filter causes significant signal losses and an active g_m-*C* filter substantially increases power consumption.

Fig. 5 shows the concepts of the proposed current-reused differential frequency multiplier. To generate differential second harmonic outputs, we used the pMOS pinch-off clipper together with the nMOS one, as shown in Fig. 5(a). The second harmonic output of the pMOS inherently has an opposite phase compared with that of the nMOS regardless of the phase of the input signals. Therefore, in the proposed frequency multiplier, we can easily generate differential second harmonics by applying in-phase or differential inputs. In addition, in order to minimize power consumption, we have stacked the pMOS

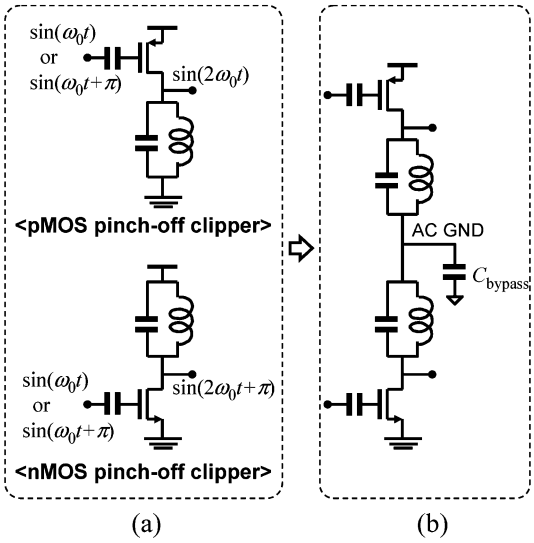


Fig. 5. Concepts of the proposed frequency multiplier. (a) Phase of second harmonics of nMOS and pMOS pinch-off clippers. (b) Current-reused frequency multiplier for power reduction.

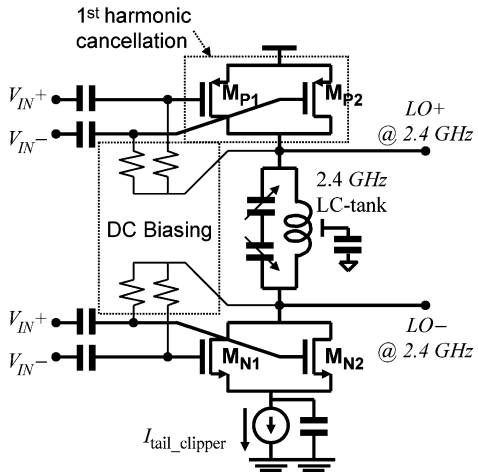


Fig. 6. Circuit topology of the proposed 2.4-GHz current-reused differential frequency multiplier ($\mathrm{M_{P1}} = \mathrm{M_{P2}} = 200/0.18\ \mu$m, $\mathrm{M_{N1}} = \mathrm{M_{N2}} = 220/0.18\ \mu$m, $L = 7$ nH).

pinch-off clipper above the nMOS one to reuse the DC bias current and inserted a large bypass capacitor (C_{bypass}) between the two pinch-off clippers to provide a reliable AC ground, as shown in Fig. 5(b).

Fig. 6 shows the circuit schematic of the proposed frequency multiplier. We use a tail current source to stabilize the DC bias current. In an inverter-type amplifier similar to the proposed frequency multiplier, the DC bias of output drain nodes should be located around half of V_{DD} to maximize voltage gain. To achieve this condition, nMOS and pMOS pinch-off clippers are self-biased, as shown in Fig. 6. This self-biasing technique makes the proposed frequency multiplier more immune to the variations of power supply, DC tail current and device mismatch. For reliable AC signal blocking between the gate and drain nodes, a large resistor is inserted. First harmonic cancellation is an important issue in frequency multiplier design,

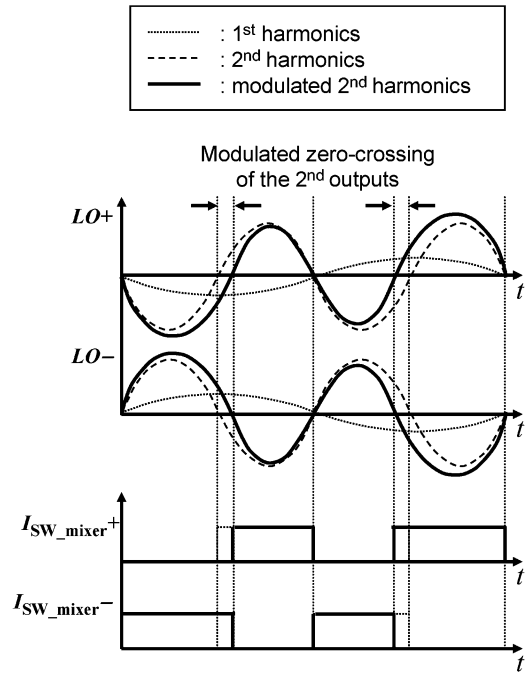


Fig. 7. Modulated second harmonics and switching currents by first harmonics.

because first harmonic can modulate the time of zero-crossing of the second harmonic signal, as shown in Fig. 7. The modulated zero-crossing can change the duty cycle of a switching stage of the mixer, resulting in an asymmetric operation of the switching transistors. To cancel out the first harmonic, we have designed each pinch-off clipper, which consists of a pair of transistors ($\mathrm{M_{P1}}/\mathrm{M_{P2}}$ and $\mathrm{M_{N1}}/\mathrm{M_{N2}}$). Then differential outputs of the VCO $(V_{\mathrm{IN}}+, V_{\mathrm{IN}}-)$ are applied to each transistor, as shown in Fig. 6. As a result, the first harmonics are fully cancelled out, and the second harmonics are added up because the phase differences of the first and second harmonics are 180° and 0°, respectively, as shown in Fig. 4. Fig. 8 shows the simulated output power of the proposed frequency source. When differential VCO output signals are applied to the proposed frequency multiplier, the output power levels of the first and second harmonics are about -55 dBm and -4 dBm, respectively. These results ensure that the proposed frequency multiplier can sufficiently suppress and amplify the first and the second harmonics, respectively. Note that, for the first harmonic to be suppressed properly in the frequency multiplier, the differential outputs of the VCO should have the same amplitude and opposite phase. Device mismatches between MOSFET pairs also degrade the first harmonic cancellation effects, as shown in Fig. 9. Therefore, symmetric design and layout techniques are important considerations.

The proposed frequency multiplier also works as a LO buffer for signal isolation between the VCO and mixer. In addition, the proposed frequency multiplier can reduce LO buffer noise because the *LC* tank can filter out flicker noise and high-frequency noise, which are far from the resonance frequency [16]. A low-noise LO buffer eventually helps to reduce the noise figure of the mixer [17].

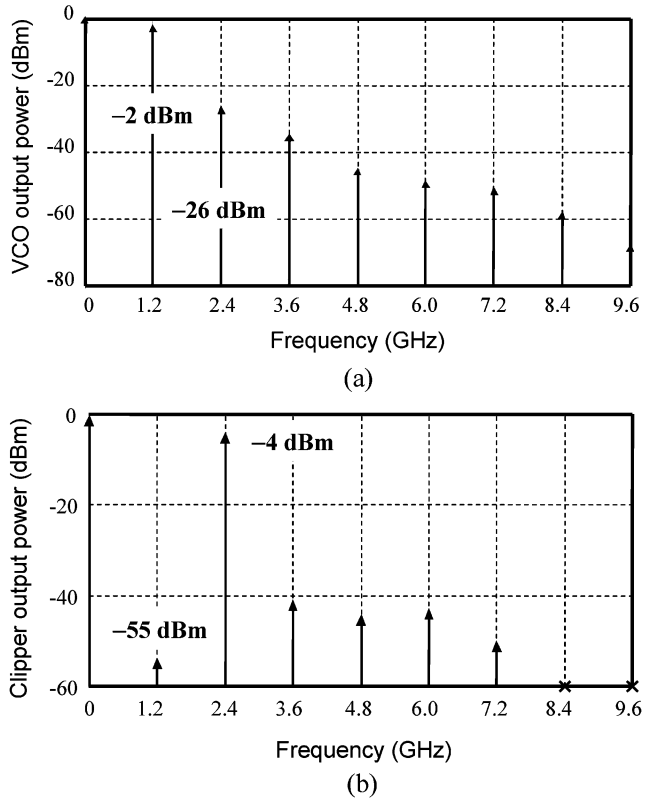


Fig. 8. Power spectrum of (a) VCO output; (b) frequency multiplier output.

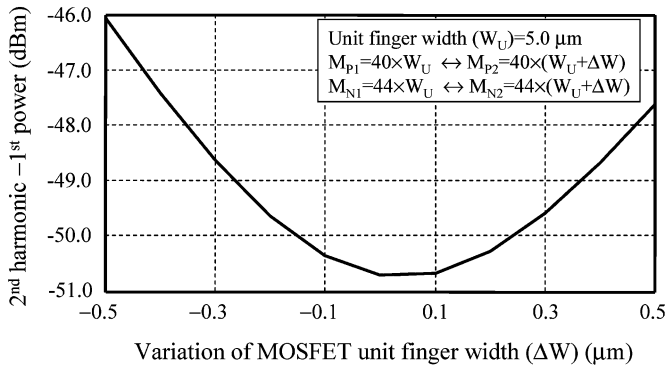


Fig. 9. Device width mismatch versus first harmonic cancellation effect.

IV. The Proposed Receiver Front-End

Fig. 10 shows two configurations of conventional front-end architectures. One is a cascaded low-noise amplifier (LNA) and SB mixer scheme, and the other is a merged LNA and SB mixer scheme. A cascaded LNA and SB mixer can give a high gain and a low noise figure because the large noise contribution of the mixer can be sufficiently suppressed by the high voltage gain of LNA. But this structure consumes high power because it has to drive two parallel stages. On the other hand, the merged LNA and SB mixer has been widely used in sub-milliwatt receivers because it can reduce power consumption effectively by removing the DC current path flowing into the LNA [18], [19]. In this scheme, the lower MOSFET amplifies the input signal in the current domain and feeds it directly into the commutating differential pairs constituting the mixer. However, this has a critical problem, which is a high noise figure. While a sufficiently amplified signal is applied to the mixer input in a cascaded LNA and mixer, the RF input is directly applied to the mixer without any signal amplification in a merged LNA and mixer. Generally, the first stage in a receiver should have low noise figure and high voltage gain to screen the noise contribution of the following stages. Unfortunately, unlike the LNA, the mixer originally has a high noise figure due to the noise modulation caused by its own nonlinear characteristics, even if noise matching is accomplished. Moreover, in a CMOS DCR, flicker noise seriously corrupts the signal quality because the merged LNA and mixer circuit topology does not have enough voltage gain to ignore flicker noise. As a result, these effects significantly hamper the entire receiver performance. In addition, this scheme suffers from strong LO leakage caused by poor isolation.

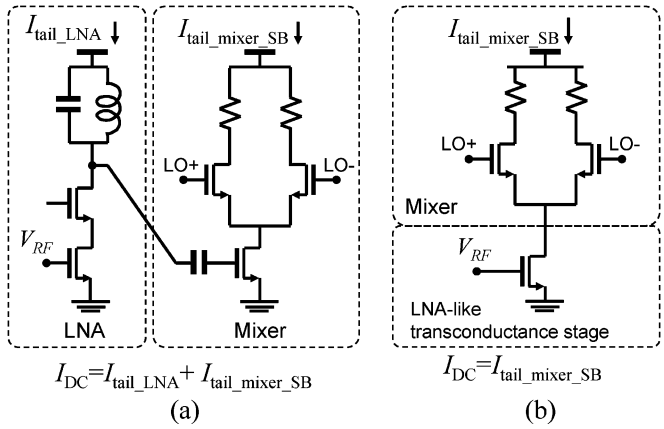


Fig. 10. Conventional front-end configurations. (a) A cascade of LNA and SB mixer. (b) Merged LNA and SB mixer.

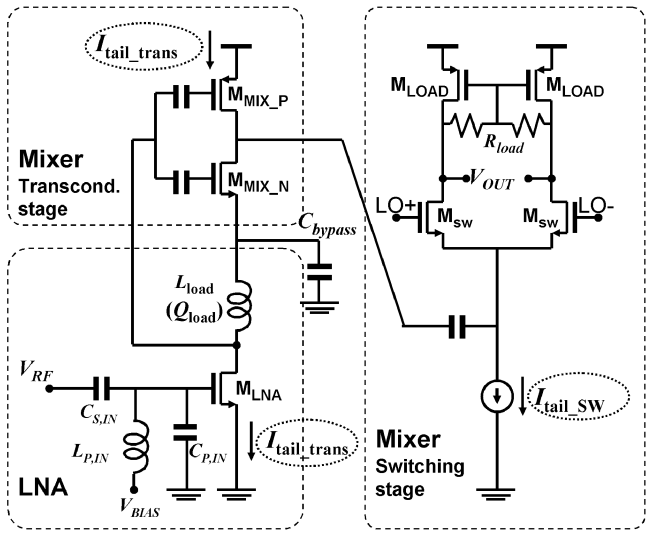


Fig. 11. Proposed current-reused folded-cascode front-end (M_{LNA} = 75/0.18 μm, M_{MIX_N} = 40/0.18 μm, M_{MIX_P} = 195/0.18 μm, M_{SW} = 35/0.18 μm, M_{LOAD} = 480/0.5 μm, R_{load} = 20 kΩ, L_{load} = 4.5 nH, $L_{P,IN}$ = 6.3 nH).

A. Circuit Implementation

To address the abovementioned problems, we propose the current-reused folded-cascode receiver front-end, as shown in

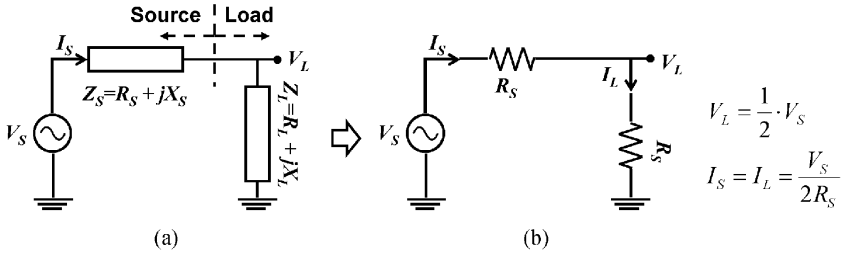


Fig. 12. Simplified matching circuit for voltage and current.

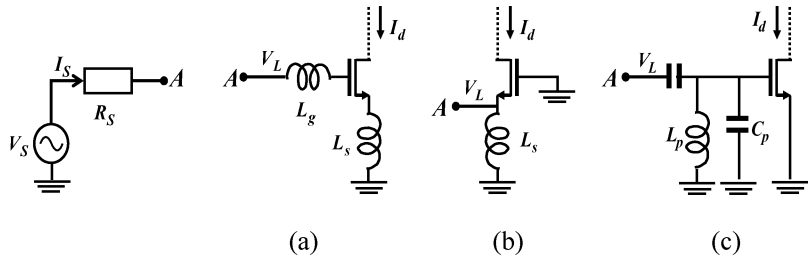


Fig. 13. LNA input matching. (a) CS-LNA with a source-degeneration inductor. (b) CG-LNA. (c) CS-LNA with a shunt inductor.

Fig. 11. To prevent RF performance degradation caused by the absence of an LNA, both an LNA and a mixer are implemented in the proposed front-end. In addition, in order to achieve low power consumption, we removed the DC current path from the power supply to the LNA. Instead, we have stacked a transconductor above the LNA and inserted a large bypass capacitor (C_{bypass}) between the LNA and the mixer, as this will provide a reliable AC ground. In this scheme, the LNA operates by only reusing the DC bias current of the mixer without any additional power consumption. However, if an LNA and a SB mixer are vertically stacked, there may not be much voltage headroom because many transistors would be stacked between VDD and the ground [23]. This is a burden as the system power supply decreases for low-power operation and avoiding MOS breakdown. In order to address this problem, we have employed a folded-cascode mixer instead of a SB mixer, as shown in Fig. 11. As you can see in this figure, the switching current of $I_{\text{tail\_SW}}$ does not flow into the LNA, but the transconductance stage current $(I_{\text{tail\_trans}})$ of the mixer is reused in LNA. This works well because the switching current in the folded-cascode mixer can be much smaller than that in the transconductance stage. This means that almost all the DC bias current of the mixer can flow into LNA so as to reuse the bias current. In addition, we have used an inverter-type transconductance stage instead of a conventional single nMOS transistor to enhance the gain of the mixer [20]. Therefore, with this implementation of the LNA and mixer with the inverter-type transconductance stage, we can achieve better RF performance compared to that of a conventional cascaded LNA and mixer. Also, this consumes no more than the amount of power used in the merged LNA and mixer, since the LNA only reuses the DC bias current of the mixer.

B. Input Matching Network

In sub-milliwatt receiver design for a disposable wireless sensor network, two important issues have to be considered: 1) single-chip integration for a cost-effective system and 2) high transconductance (G_m) of the LNA including the matching network, which is given by

$$G_m = \frac{I_d}{V_S} \tag{4}$$

where V_S is the applied source voltage and I_d is the drain current of the transconductance MOSFET in the LNA. In order to easily calculate the transconductance, all matching networks including source, load, and matching circuit can be simplified, as shown in Fig. 12. If $Z_S = Z_L$ and there is no signal reflection, the load voltage (V_L) and current (I_L) are given by

$$V_L = \frac{Z_L}{Z_S + Z_L}\cdot V_S = \frac{R_S}{R_S + R_S}\cdot V_S = \frac{1}{2}\cdot V_S \tag{5}$$

$$I_L = I_S = \frac{V_S}{Z_S + Z_L} = \frac{V_S}{2R_S} \tag{6}$$

There are a variety of ways to configure the impedance matching circuits in LNA as shown in Fig. 14. According to the types of matching and input node, they show different G_m characteristics. First, consider the common-source (CS) LNA with a source degeneration inductor, as shown in Fig. 13(a). Using (5) and (6), the G_m of this LNA is given by

$$\begin{aligned} G_m &= \frac{I_d}{V_S} = \frac{g_m \cdot v_{gs}}{V_S} = \frac{g_m}{V_S}\cdot\left(I_S \cdot \frac{1}{sC_{gs}}\right) \\ &= \frac{g_m}{sC_{gs}}\cdot\frac{V_S/2R_S}{V_S} = \frac{\omega_T}{\omega_0}\cdot\frac{1}{2R_S} \end{aligned} \tag{7}$$

where ω_0 is operation frequency and ω_T, v_{gs}, g_m, and C_{gs} are the cut-off frequency, gate-to-source voltage, transconductance, and capacitance of MOSFET, respectively. This equation indicates that G_m is proportional to the cut-off frequency and inversely proportional to the operation frequency [24]. However in sub-milliwatt systems, it is difficult to make a high cut-off frequency MOSFET. Therefore, especially in a low-power UHF application, a common-source LNA with a

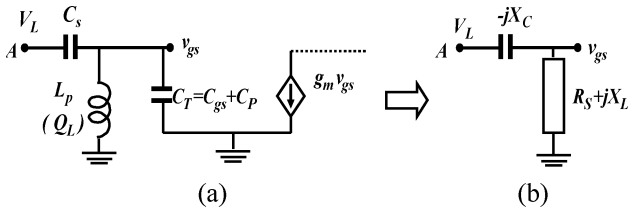


Fig. 14. CS-LNA with a shunt inductor. (a) Equivalent circuit. (b) Matching condition.

degeneration inductor is not suitable to achieve high gain for screening the noise contribution of the mixer. In addition, a common-source LNA requires an off-chip inductor to compensate for the small C_{gs}, resulting in a high-cost WSN. The G_m of the common-gate (CG) LNA is given by

$$G_m = \frac{I_d}{V_S} = \frac{g_m \cdot v_{gs}}{V_S} = \frac{g_m}{V_S} \cdot V_L = g_m \cdot \frac{V_S/2}{V_S} = \frac{g_m}{2} = \frac{1}{2R_S} \tag{8}$$

Comparing (7) and (8), the G_m of the common-gate LNA is smaller than that of the common-source LNA because ω_T is at least larger than ω_0 of 2.4 GHz. Next, the common-source LNA with a shunt inductor is shown in Fig. 13(c). Under the impedance matched condition, this LNA can be redrawn, as shown in Fig. 14. The parallel connected C_T and $L_{\rm P}$ can be translated as series connected resistance (R_S) and inductance (jX_L), as shown in Fig. 14(b). Therefore, the G_m of this LNA is given by

$$v_{gs} = \frac{R_S + jX_L}{R_S + jX_L - jX_C} \cdot V_L = \frac{R_S + jX_L}{R_S} \cdot V_L \tag{9}$$

$$G_m = \frac{I_d}{V_S} = \frac{g_m \cdot v_{gs}}{V_S} = g_m \cdot \frac{V_L}{V_S} \cdot \frac{R_S + jX_L}{R_S} = \frac{1}{2R_S} \cdot g_m(R_S + jX_L). \tag{10}$$

Comparing (7) and (10), the G_m of the CS-LNA with a shunt inductor is independent of the cut-off frequency. Therefore, this has design freedom to determine MOS size and bias conditions. And if $g_m|R_S + jX_L|$ is larger than unity or ω_T/ω_0, higher voltage gain can be achieved compared with CG-LNA or CS-LNA with a degeneration inductor. In (10), X_L is a function of effective parallel resistance of $L_{\rm P}$, which is approximately given by $Q_L\omega_0 L_{\rm P}$. Fig. 15 shows the relationship between $|R_S + jX_L|$ and $Q_L\omega_0 L_{\rm P}$. Therefore, to maximize the transconductance G_m, an inductor with large inductance as well as a high quality (Q)-factor should be used for matching network. However, it should be noted that large inductance with high Q makes a narrowband matching circuit.

Generally, a CS-LNA with a shunt inductor has a poorer noise figure characteristic due to the shunt inductor loss. Nevertheless, this LNA is more suitable for extremely low-power applications rather than a CS-LNA with a source degeneration inductor. This is because the LNA should have an enough gain to suppress the high noise figure of the following mixer.

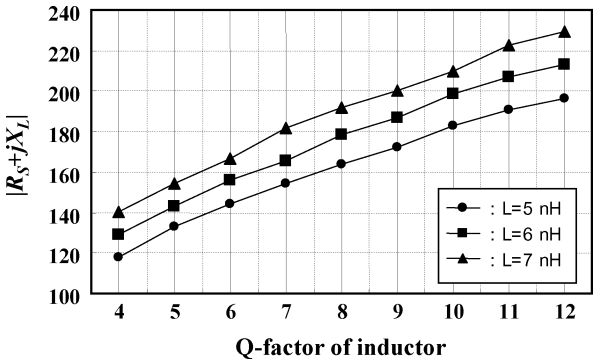


Fig. 15. Q-factor versus input impedance of matching circuit.

C. Noise Immunity Characteristics

The noise figure improvement of the proposed front-end can be explained from two points of view. First, the large voltage gain of the LNA sufficiently suppresses white and flicker noise modulated by the mixer. Second, a folded-cascode mixer is intrinsically less influenced by flicker noise, which is the dominant noise source in direct-conversion receivers. In a fully symmetric differential mixer, the output signal is affected only by flicker noise generated in the switching stage [17], [25]. In a commutating mixer, the flicker noise generated from the switching pair $(\rm M_{SW})$ slowly modulates zero-crossing points in each switching pair. Flicker noise makes the time of the zero-crossing of LO signals advance by [17]

$$\Delta t = \frac{V_n(t)}{S} \tag{11}$$

where $V_n(t)$ is flicker noise voltage and S is the slope of the LO voltage at the switching time. Thus, the frequency spectrum of flicker noise at the mixer output is given by

$$i_{o,n}(f) = \frac{4I_{\rm tail\_SW}}{T}\Delta t = I_{\rm tail\_SW} \cdot \frac{4V_n(f)}{S \times T} \propto I_{\rm tail\_SW} \tag{12}$$

where $I_{\rm tail\_SW}$ is the DC tail current in the switching stag, and T is the period of the LO signal. This equation demonstrates that one way of lowering the mixer flicker noise is to reduce the DC current of the switching stage. Unfortunately, in an SB mixer, the bias current should be large enough to obtain a sufficient voltage gain. This is because the switching current eventually is supplied to the transconductance gain stage. However, in the proposed folded-cascode mixer, the switching current can be drastically reduced without any loss of voltage gain because the transconductance stage and the switching stage are separated in DC biasing. Therefore, compared with an SB mixer, the output noise voltage caused by flicker noise can be decreased as the ratio of

$$\frac{v_{o,n}(f)|_{\rm Folded}}{v_{o,n}(f)|_{\rm SB}} = \frac{i_{o,n}(f)|_{\rm Folded}}{i_{o,n}(f)|_{\rm SB}} = \frac{I_{\rm tail\_SW\_Folded}}{I_{\rm tail\_SW\_SB}} \tag{13}$$

where $I_{\rm tail\_SW\_Folded}$ and $I_{\rm tail\_SW\_SB}$ are the DC bias current in the switching stages of the folded-cascode mixer and the SB mixer, respectively.

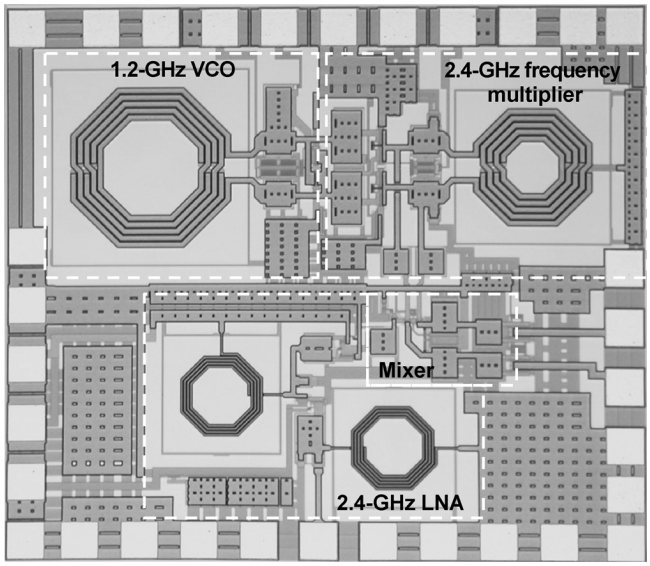


Fig. 16. Fabricated current-reused folded-cascode receiver front-end and LO source (1.6×1.45 mm^2 including pads).

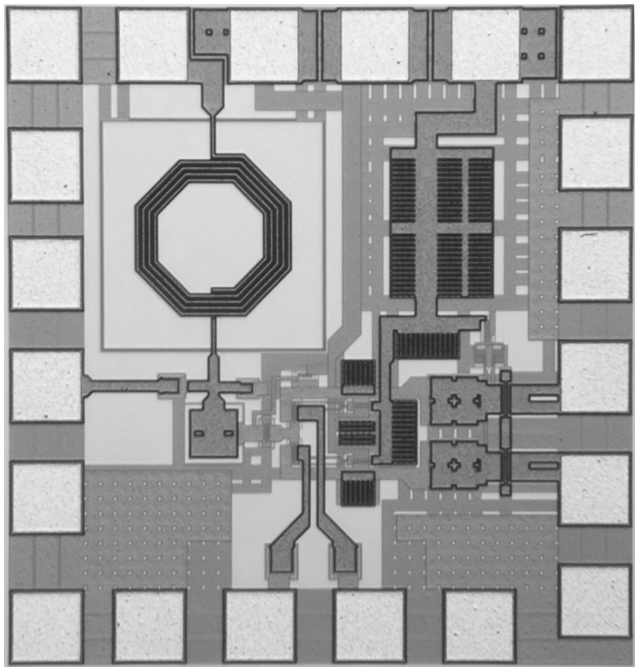


Fig. 17. Microphotograph of a conventional merged LNA and SB mixer (occupies an area of 0.85×0.9 mm^2).

In the proposed scheme, we can achieve high conversion gain by employing LNA and the current-reused transconductance stage in the inverter-type mixer. This high gain can reduce the SNR degradation caused by flicker noise. If same matching circuits are used, overall voltage gain enhancement of the proposed front-end compared with the merged LNA and SB mixer is given by

$$(g_{m\_\mathrm{LNA}} \cdot \omega_0 Q_{\mathrm{load}} L_{\mathrm{load}}) \frac{g_{m\_\mathrm{MIX\_N}} + g_{m\_\mathrm{MIX\_P}}}{g_{m\_\mathrm{SB}}} \qquad (14)$$

where ω_0 is operating frequency, Q_{load} and L_{load} are the Q-factor and inductance of the load inductor, $g_{m_{\mathrm{LNA}}}$, $g_{m\_\mathrm{MIX\_N}}$, and $g_{m\_\mathrm{MIX\_P}}$ are the transconductances of MLNA, MMIX_N, and MMIX_P, respectively, and g_{m_SB} is the transconductance of the SB mixer. As shown in (14), if $g_{m\_\mathrm{MIX\_N}}$, $g_{m\_\mathrm{MIX\_P}}$, and g_{m_SB} have the same value, the proposed front-end can achieve by maximum $2 \cdot (g_{m\_\mathrm{LNA}} \cdot \omega_0 Q_{\mathrm{load}} L_{\mathrm{load}})$ times higher voltage gain than the conventional merged LNA and mixer. Therefore, if only considering flicker noise effect, the total SNR improvement of the proposed front-end over the merged LNA and SB mixer can be given by

$$2 \cdot (g_{m\_\mathrm{LNA}} \cdot \omega_0 Q_{\mathrm{load}} L_{\mathrm{load}}) \frac{I_{\mathrm{tail\_SW\_SB}}}{I_{\mathrm{tail\_SW\_Folded}}}. \qquad (15)$$

Equation (15) ensures that the proposed front-end will be much more immune to flicker noise as well as to white noise.

V. Measurement Results

Fig. 16 shows the fabricated current-reused folded-cascode front-end including the LO frequency source, which occupies an area of 1.6×1.45 mm^2 including the pads area. In order to verify the proposed concepts, we also fabricated a conventional merged LNA and SB mixer for the purpose of performance comparisons, as shown in Fig. 17. This chip occupies an area of 0.85×0.9 mm^2. The two chips were fabricated using 0.18-μm one-poly six-metal CMOS technology, which provides a 2-μm-thick Al metal layer. An Agilent N8973A Noise Figure Analyzer was used to measure the single-side band (SSB) noise figure. The output spectrum and phase noise are obtained from the HP 8564E Spectrum Analyzer and its Phase Noise Measurement Kit.

The frequency source consists of a 1.2-GHz differential LC-VCO and a 2.4-GHz current-reused differential frequency multiplier. In order to increase the Q-factor for low phase noise and low-power frequency source, differential octagonal-shape inductors are used in both *LC* tanks. Note that the two *LC* tanks used in the VCO and frequency multiplier are tuned by the same control voltage and have narrow pass-bands centered at the different frequencies of 1.2 GHz and 2.4 GHz, respectively. Therefore, to make the multiplier output as large as possible, the *LC* tank in the multiplier should be carefully optimized to resonate at exactly twice the frequency of the VCO regardless of the changing varactor control bias.

The fabricated frequency source consumes 840-μA bias current (490 μA for a VCO and 350 μA for a frequency multiplier) from a 0.7 V power supply. The frequency source tunes from 2.22 GHz to 2.45 GHz by changing the control bias from 0 V to 0.7 V. Measured phase noise at 1 MHz offset from the 2.2-GHz carrier frequency is -115.83 dBc/Hz, as shown in Fig. 18. The figure of merit (FOM) of the fabricated frequency source is 187.4 dBc/Hz excluding the power consumption of the frequency multiplier. Fig. 19 shows the harmonic spectrum of the fabricated frequency source. The output power of the second harmonic amplified by the frequency multiplier is about -10.8 dBm at 2.2 GHz, which is about 23 dB larger than that of the first harmonic at 1.1 GHz. This result shows that the first harmonics of the VCO cancel each other out by applying differential signals to a pair of transistors, as shown in Fig. 6. But

TABLE II
FRONT-END PERFORMANCE COMPARISON

	[19]	[21]	This work	This work	*Improvement
Type	Merged LNA & SB mixer	Cascaded LNA & SB mixer	Merged LNA & SB mixer	Current-reused front-end	-
Process	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	-
Frequency (GHz)	2.35	2.44	2.4	2.4	-
V_{DD}/I_{DD} (V / mA)	1.2 / 1.4	1.8 / 3.6	1.0 / 0.5	1.0 / 0.5	-
Power (mW)	1.68	6.48	0.5	0.5	
Voltage gain (dB)	14.5	21.4	20.4	30.5	10.1
P1dB (dBm)	-	-	–23	–31	
NF (dB)	**24.5	13.9 @ 2 MHz IF	19 @10 MHz IF	10.1 @10 MHz IF	8.9
			13.1 @ 50 MHz IF	9.2 @ 50 MHz IF	3.9

* Performance improvement of the proposed front-end compared with the merged LNA and SB mixer in this work.
** Measured from analog test output, not front-end.

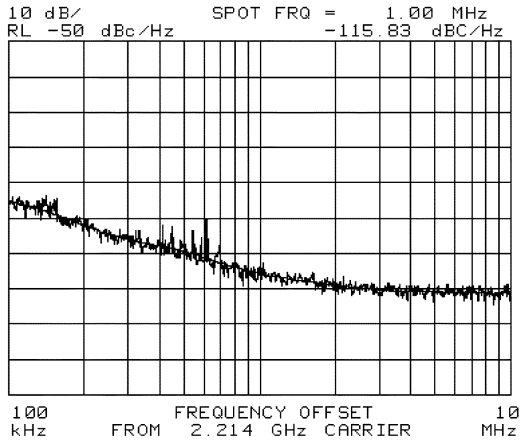


Fig. 18. Measured phase noise of the fabricated frequency source.

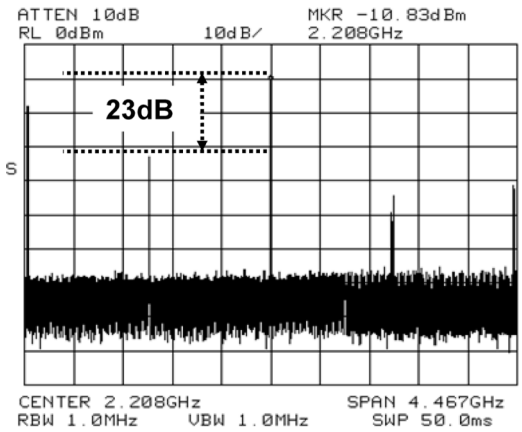


Fig. 19. Measured output spectrum of the frequency source at the center frequency of 2.21 GHz.

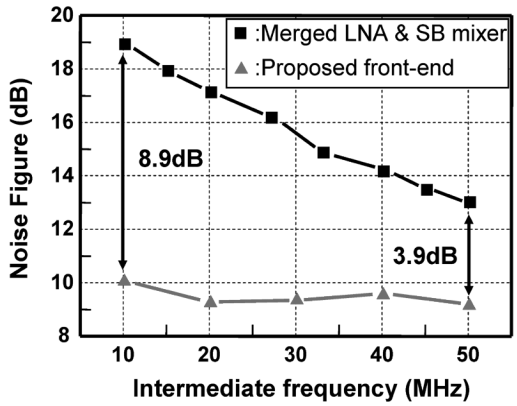


Fig. 20. Measured SSB NF of fabricated front-ends.

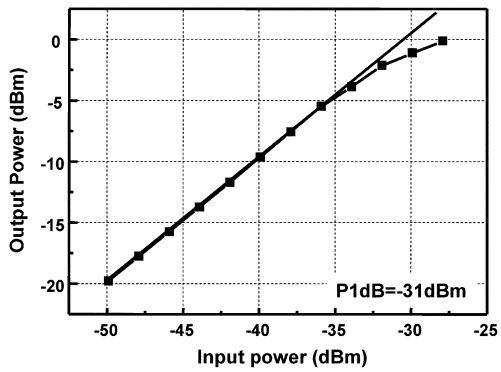


Fig. 21. Output power versus input power of the proposed front-end.

the difference is much smaller than in the simulation results presented in Fig. 8. As mentioned in Section III-B, this nonperfect cancellation of the first harmonic is caused by the asymmetry of the VCO output signals and layout mismatches.

The measured conversion gain of the conventional merged LNA and SB mixer is 20.4 dB, while taking only 500 μA from a 1.0-V power supply. In the same bias condition, the proposed front-end achieves a maximum gain of 30.5 dB, which is 10 dB greater than the conventional front-end. Fig. 20 shows the measured single-side band (SSB) noise figure over the output frequency range of 10 MHz to 50 MHz. As expected, the noise figure of the proposed front-end was significantly lower compared to that of the merged LNA and SB mixer. This is true over the entire measured frequency range. It is especially noteworthy that the noise figure shows a greater improvement at lower output frequencies in our graph (8.9 dB at 10 MHz and 3.9 dB at 50 MHz). These data confirm that the proposed current-reused folded-cascode front-end is much more immune to flicker noise as well as white noise due to the lower flicker noise contribution of the folded-cascode mixer and the noise screening effect of the LNA. The measured 1-dB compression

point (P1 dB) of the proposed front-end is −31 dBm, as shown in Fig. 21. Table II shows the summary of the measured performance of the proposed current-reused front-end compared with the conventional merged LNA and mixer and previously reported work.

VI. Conclusion

We have proposed and demonstrated a 2.4-GHz fully integrated CMOS receiver front-end and a frequency source using a current-reused technique. The proposed frequency source consists of a 1.2-GHz VCO and a 2.4-GHz differential frequency multiplier to reduce power consumption. The proposed receiver front-end improves noise figure and conversion gain by employing a vertically stacked LNA and folded-cascode mixer. The fully integrated frequency source achieves a phase noise of −115.83 dBc/Hz at 1 MHz offset from the 2.2-GHz carrier frequency with 590 μW power consumption (343 μW for a VCO and 245 μW for the frequency multiplier). And the fabricated receiver front-end achieves a voltage gain of 30.5 dB with a noise figure of 10.1 dB, achieved with only 500 μW power consumption.

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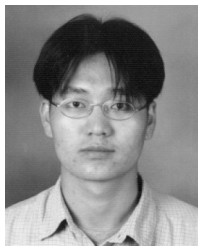

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