Spintronic Logic and Memory Devices: Prospects and Challenges

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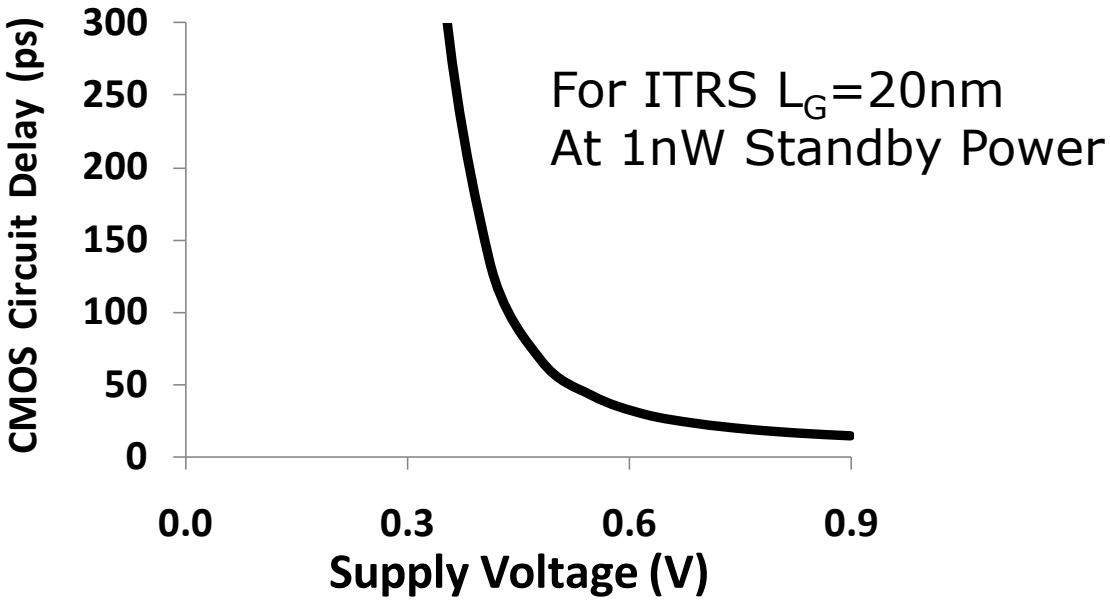
Why are we looking beyond CMOS?

Computation Efficiency needs max. performance at lowest supply (V_{dd})

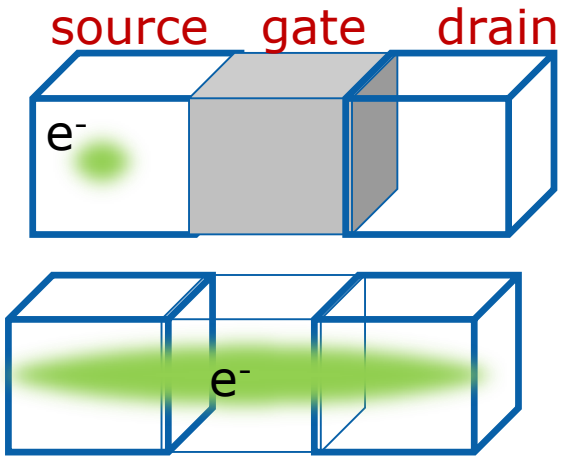
- Switching Energy α CV_{dd}^2
- At $V_{dd} \leq V_{th}$, performance suffers significantly
- Lowest V_{th} is limited by leakage
- Computation efficiency of CMOS limited by 60 mV/dec I_d/V_{gs} sub-threshold Slope

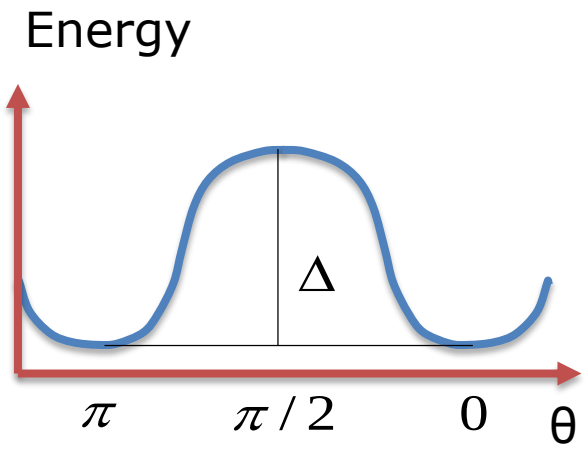


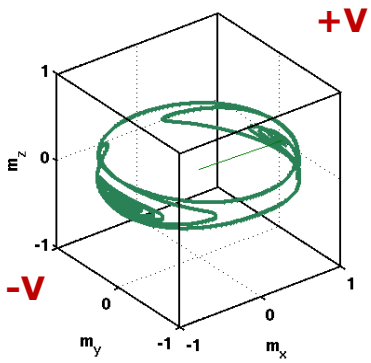
Agenda

1) Introduction
   - ❑ the need for a Beyond-CMOS Logic Device
2) Spintronics and All-Spin Logic
   - ❑ Operation
   - ❑ Modeling
   - ❑ Spin Logic Circuit Simulation
3) Materials and Interfaces to enable scaling

Barriers, Collectives, Thermodynamics







Generic Electronic Switch

$$E = NeV \sim 4000kT \quad I_{on}/I_{off} < e^{\frac{eV}{kT}}$$

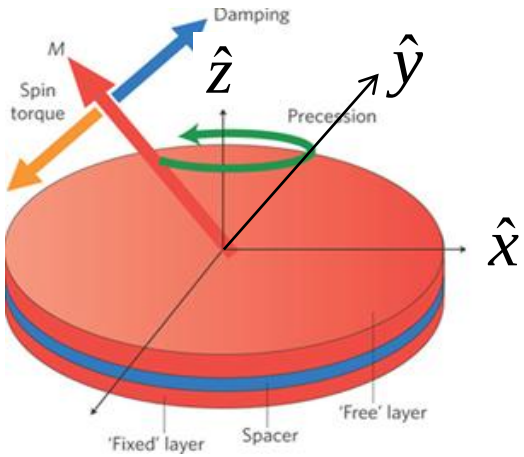
Generic Spintronic Switch

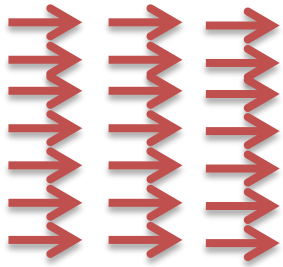
$$E = \frac{1}{2}\mu_0 V M_s H_k \sim 60kT$$

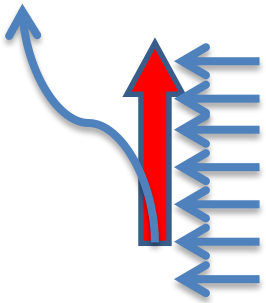
	Generic Electronic Switch	Generic Spintronic Switch
Barrier	20 kT at V_{dd} = 0.5 V	60 kT (Non-volatile)
Voltage	0.5 – 1 V	10-100 mV
Switching Energy	N*20kT, N=200 electrons	60-80 kT
Phenomenon	Non collective	Collective

2. Spin Logic and Circuit Exploration

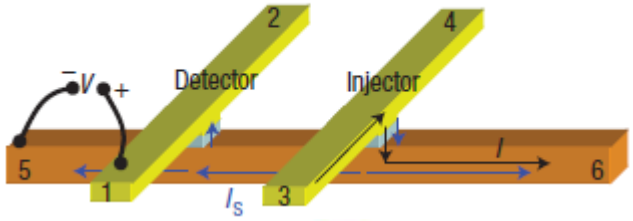
Spin logic device based on spin torque

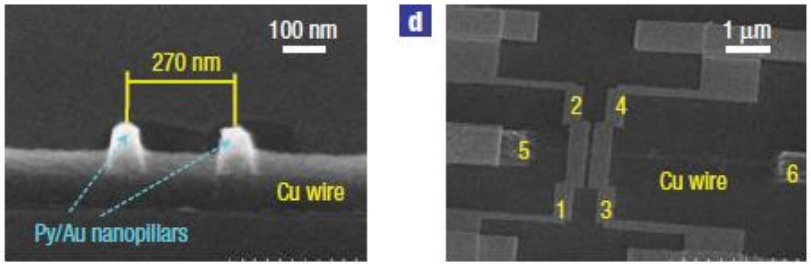




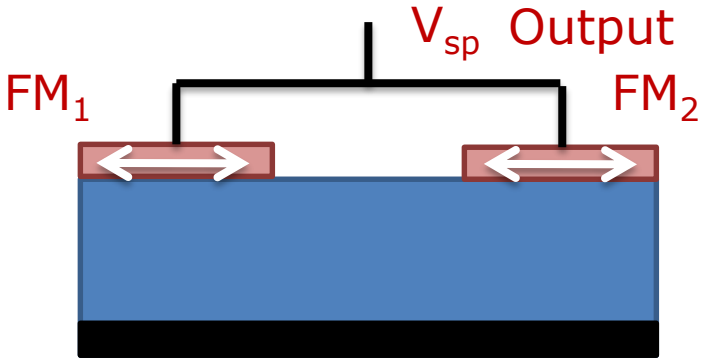


Injected current





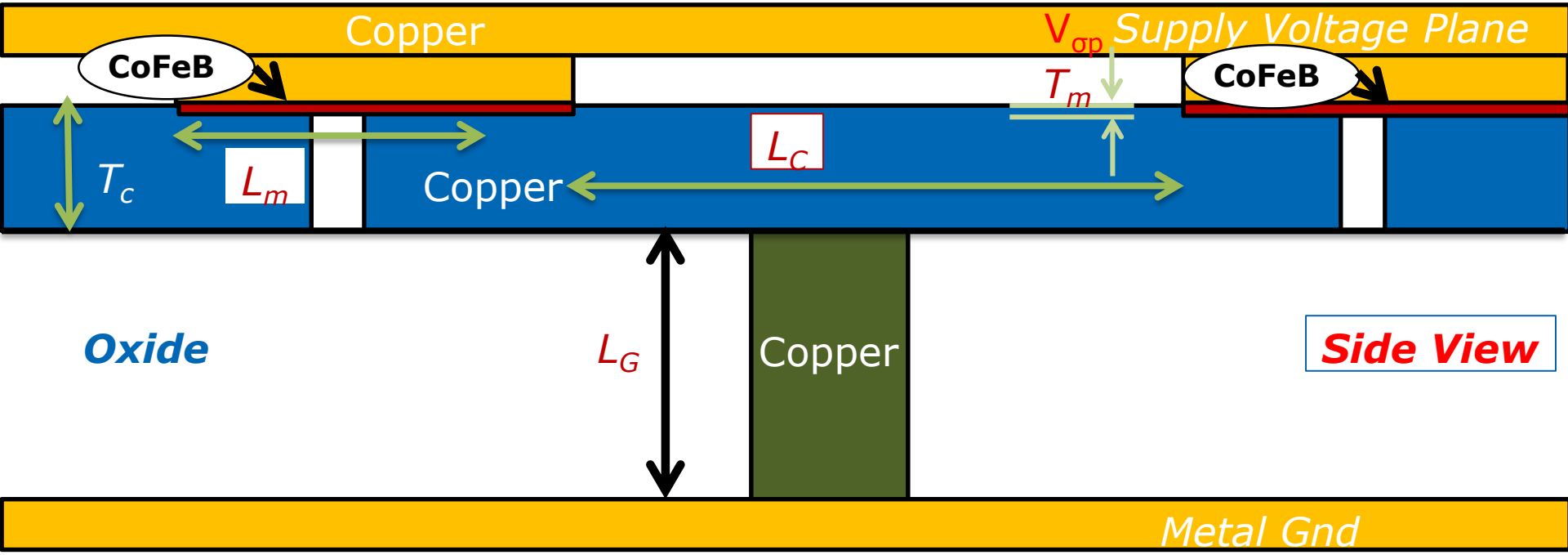
Nature Physics **4**, 851 - 854 (2008)



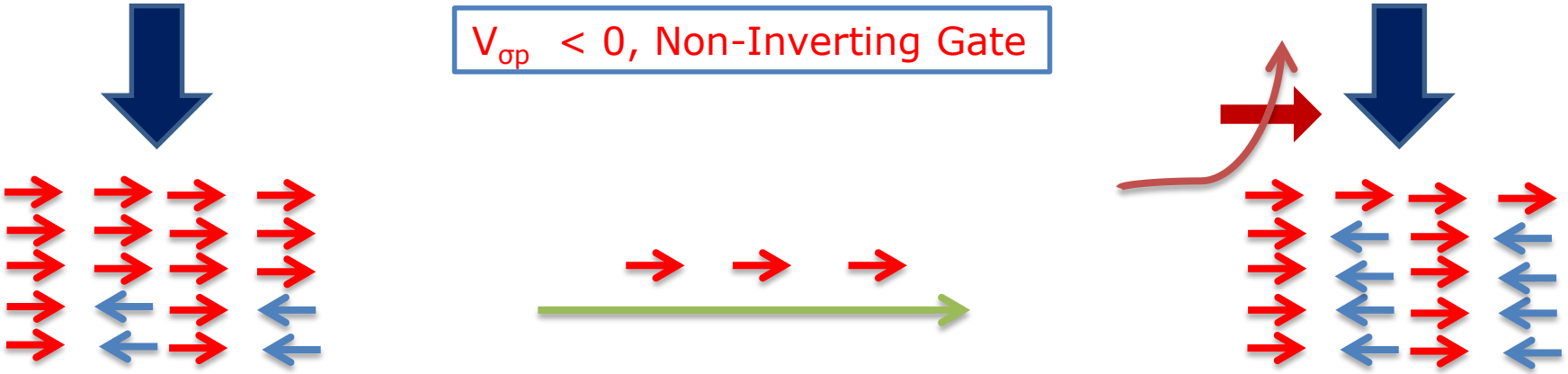
Proposed all spin logic device

ASL-Purdue, STMG-Intel

An example Spin logic device schematic



$V_{\sigma p}$ < 0, Non-Inverting Gate



The dominant magnet injects net spin into the output forcing output to align

Exploring Spin Logic Devices

1. Modeling the spin devices and circuits

2. Extracting the scaling methods for spin logic (using 1)

3. Realizing the materials and interfaces (guided by 2)

Describing Spin currents, Voltages, Conductances

Vector spin current is the net flow of vector magnetic moment between the nodes

$$\vec{I}_s = I_{sx}\hat{x} + I_{sy}\hat{y} + I_{sz}\hat{z}$$

Spin voltage is proportional to the net spin population

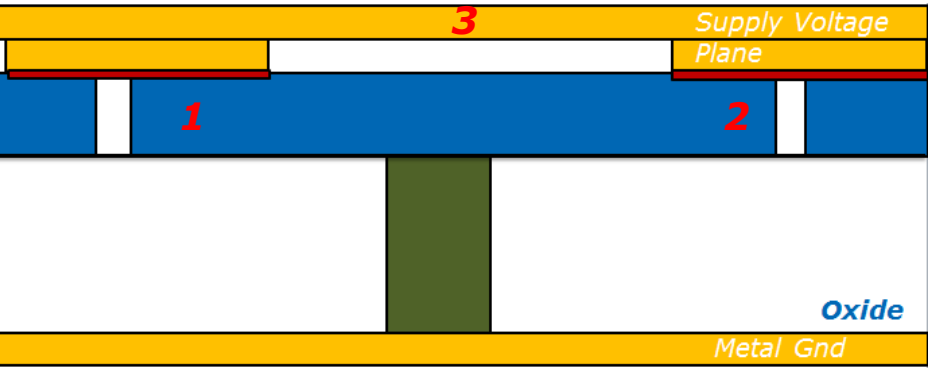
$$-e\vec{V}_s = \frac{4}{3}\frac{\Delta\vec{n}}{n}\mu$$

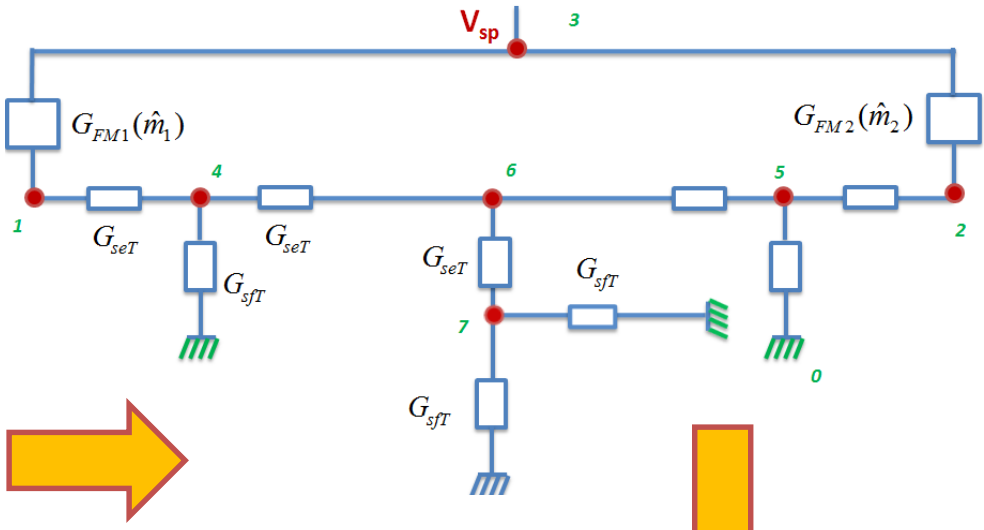
A spin conductance relates vector spin voltages to vector spin currents

$$\begin{bmatrix} I_c \\ I_{sx} \\ I_{sy} \\ I_{sz} \end{bmatrix} = \begin{bmatrix} \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \end{bmatrix} \begin{bmatrix} V_1 - V_2 \\ V_{sx1} - V_{sx2} \\ V_{sy1} - V_{sy2} \\ V_{sz1} - V_{sz2} \end{bmatrix}$$

Spin circuit theory is simply the book keeping of spin currents imposed by spin transport

Inverting/Non-inverting Gate : "*spin-SPICE" Example*





Current Sources

Voltage Sources

$$\begin{bmatrix} O \\ O \\ O \\ O \\ O \\ O \\ O \\ V_{sp} \end{bmatrix} = \begin{bmatrix} G & B \\ C & D \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \\ I_{sp} \end{bmatrix}$$

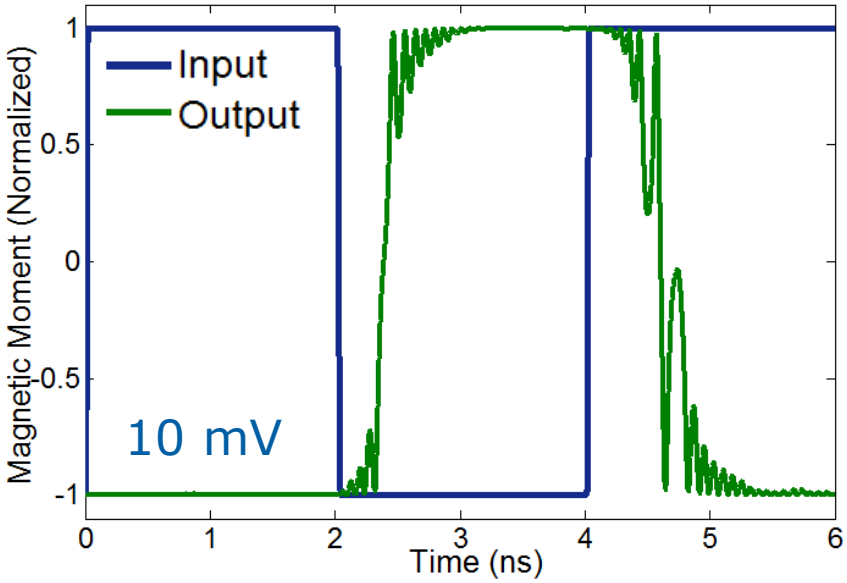
Node Voltages

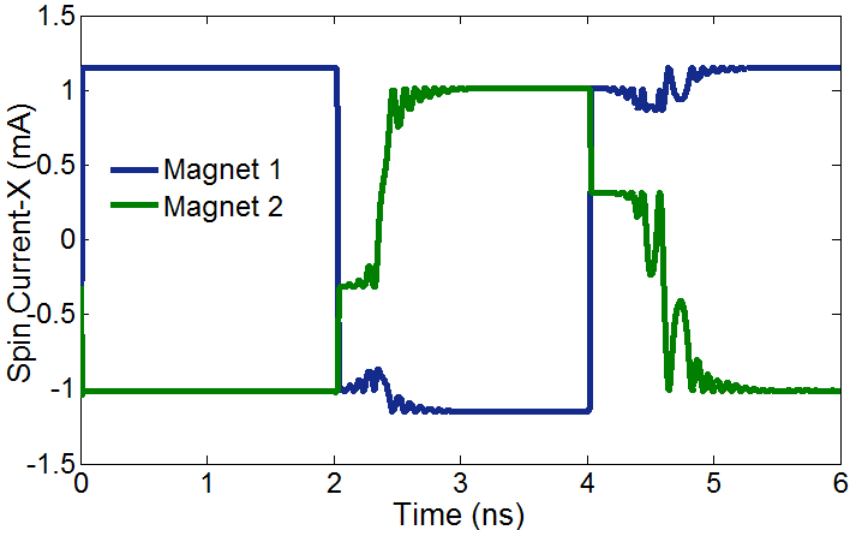
Spin net list

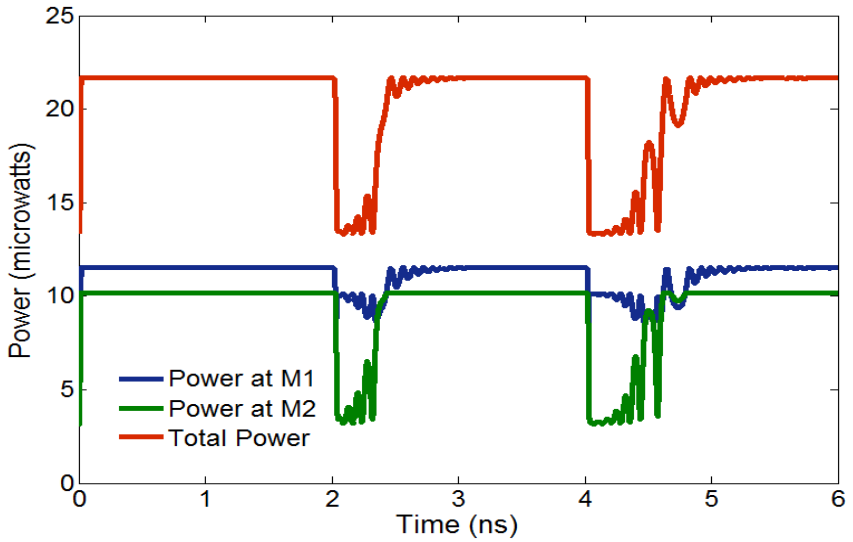
```
V3 3 0 1
RF1 1 3 GF1
RF2 2 3 GF2
Rst1 1 4 Gset
Rst1 4 6 Gset
Rsft 4 0 Gsft
Rst1 2 5 Gset
Rst1 5 6 Gset
Rsft 5 0 Gsft
Rst1 6 7 GsetG
Rstsft1 7 0 GfttG0
```

Manipatruni, S., Nikonov, D. E., & Young, I. A. (2012). Modeling and Design of Spintronic Integrated Circuits. Circuits and Systems I: Regular Papers, IEEE Transactions on, 59(12), 2801-2814.

Inverting Gate : "*spin-SPICE" Results*

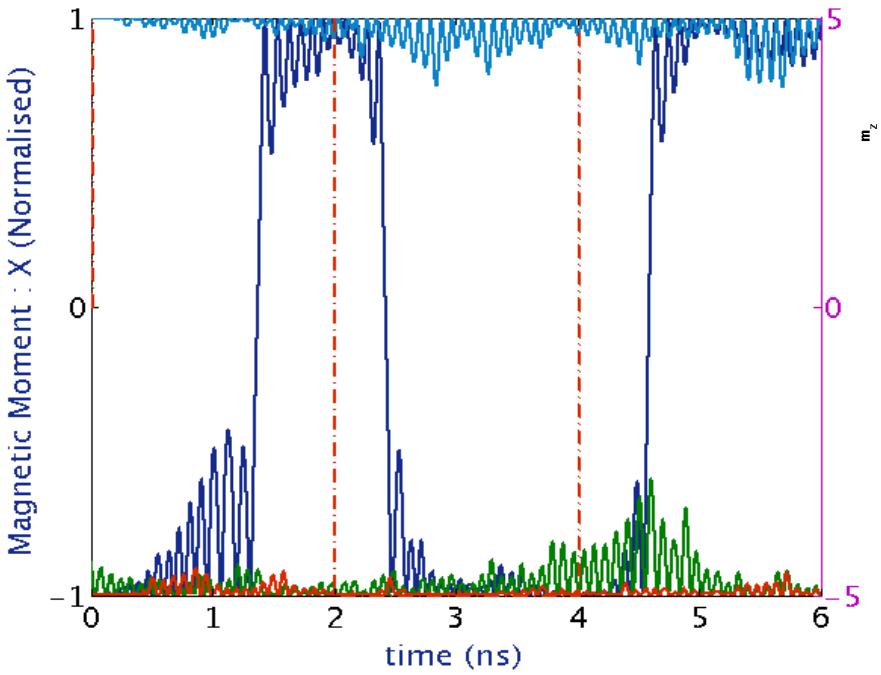


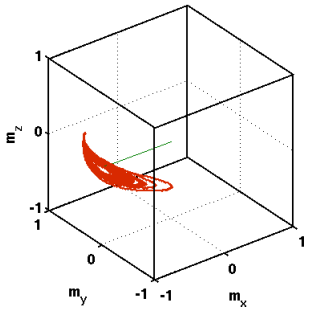


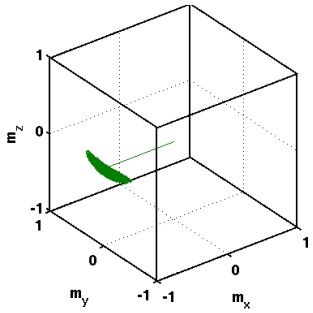


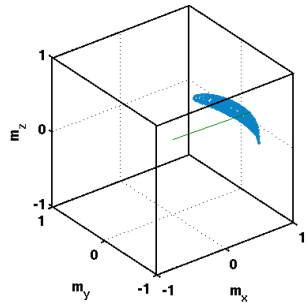
Delay = 0.5 ns
Energy = 7.2 fJ
E x D = 3.6 fJ.ns, ~0 leakage
7 year retention time

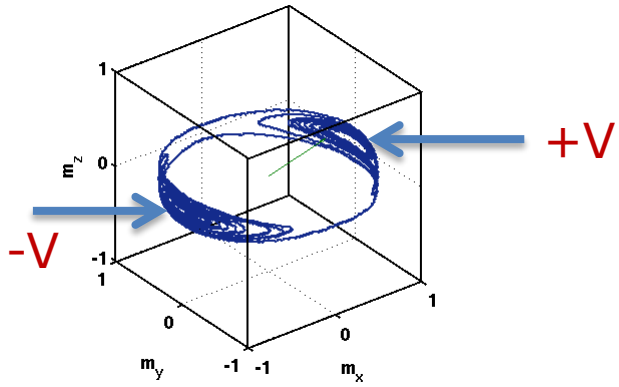
Majority Logic input [1 1 0] Output [1]









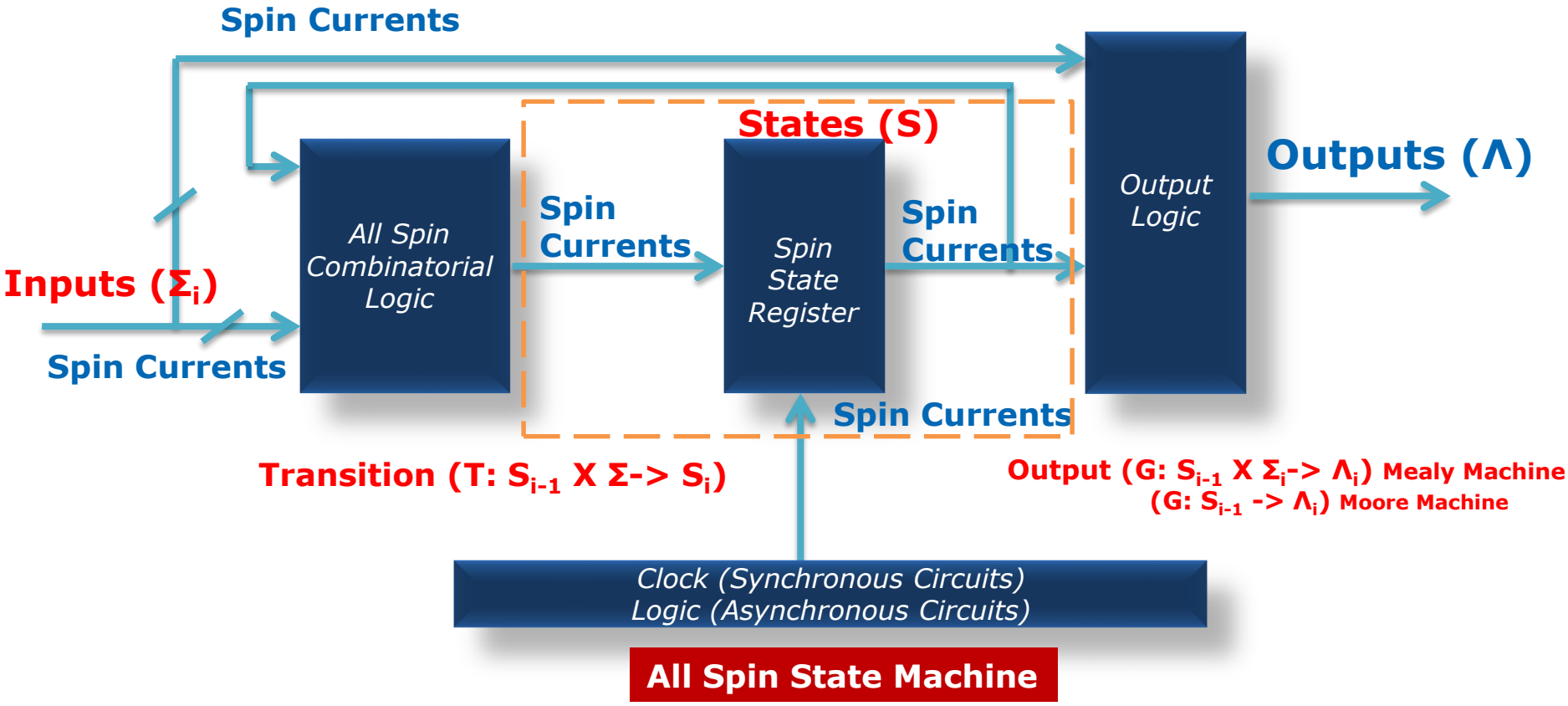


In1	In2	In3	Major	Minor
1	1	1	1	0
1	1	0	1	0
1	0	1	1	0
1	0	0	0	1
0	1	1	1	0
0	1	0	0	1
0	0	1	0	1
0	0	0	0	1

Spin Logic is compatible with high fan in logic

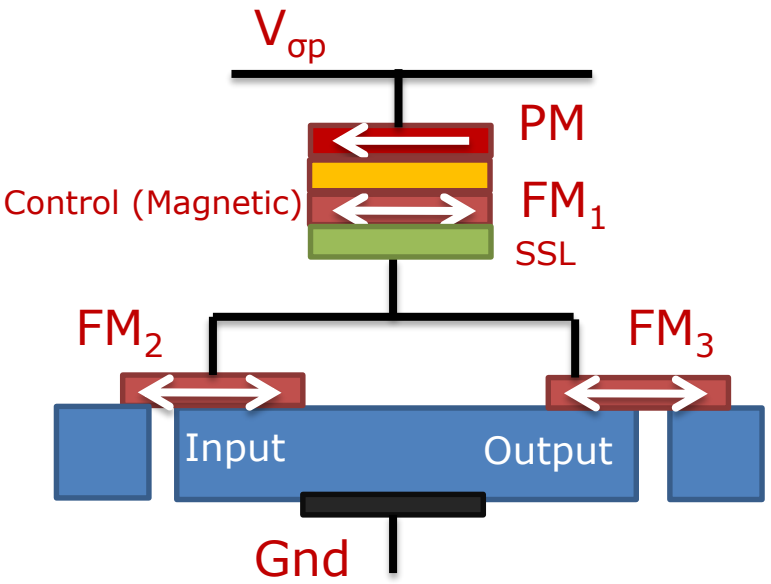
Calayir, V., Nikonov, D., Manipatruni, S., & Young, I. A.
TCAS 2013

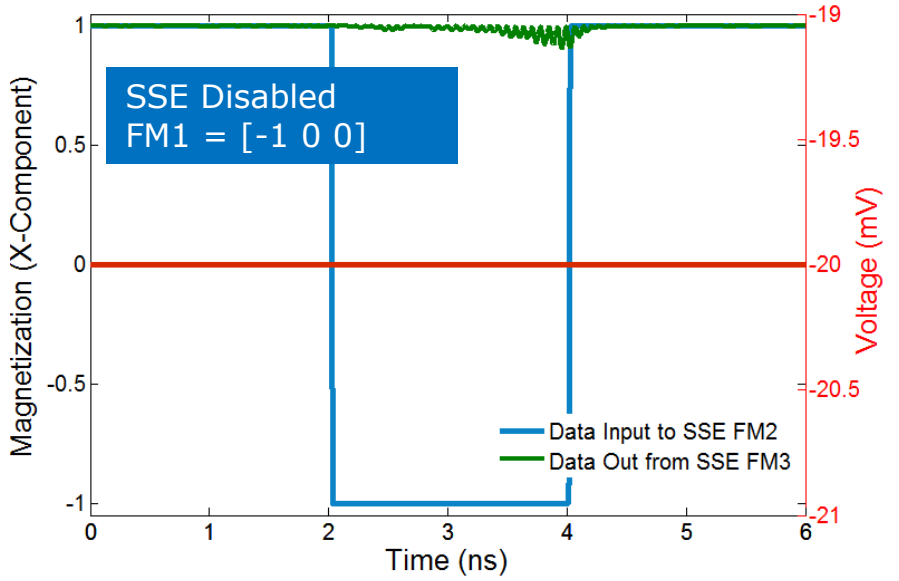
Spin State Elements and Machines

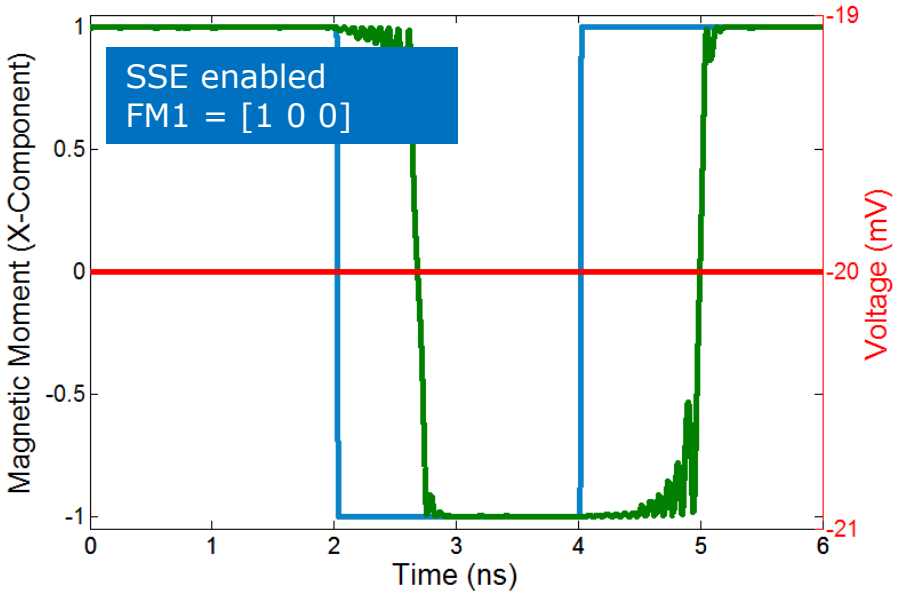


State element is an essential but often overlooked component.

Spin State Elements







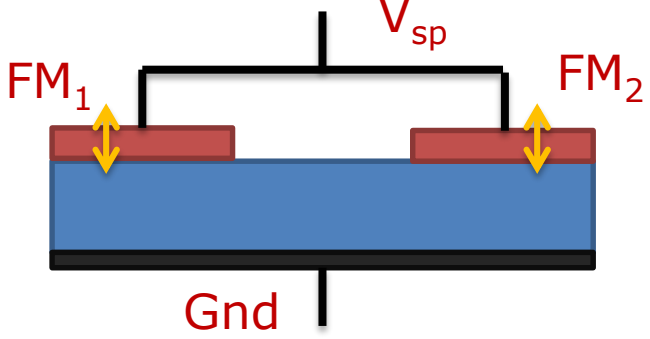
State elements combined with combinatorial logic and interconnects form a full synchronous compute family.

Exploring Spin Logic Devices

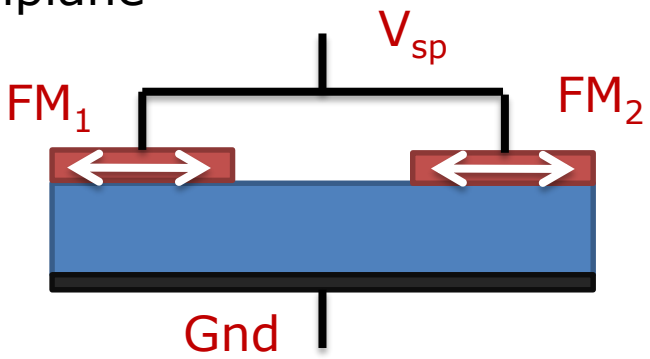
1. Modeling the spin devices and circuits
2. Extracting the scaling methods for spin logic (using 1)
3. Realizing the materials and interfaces (guided by 2)

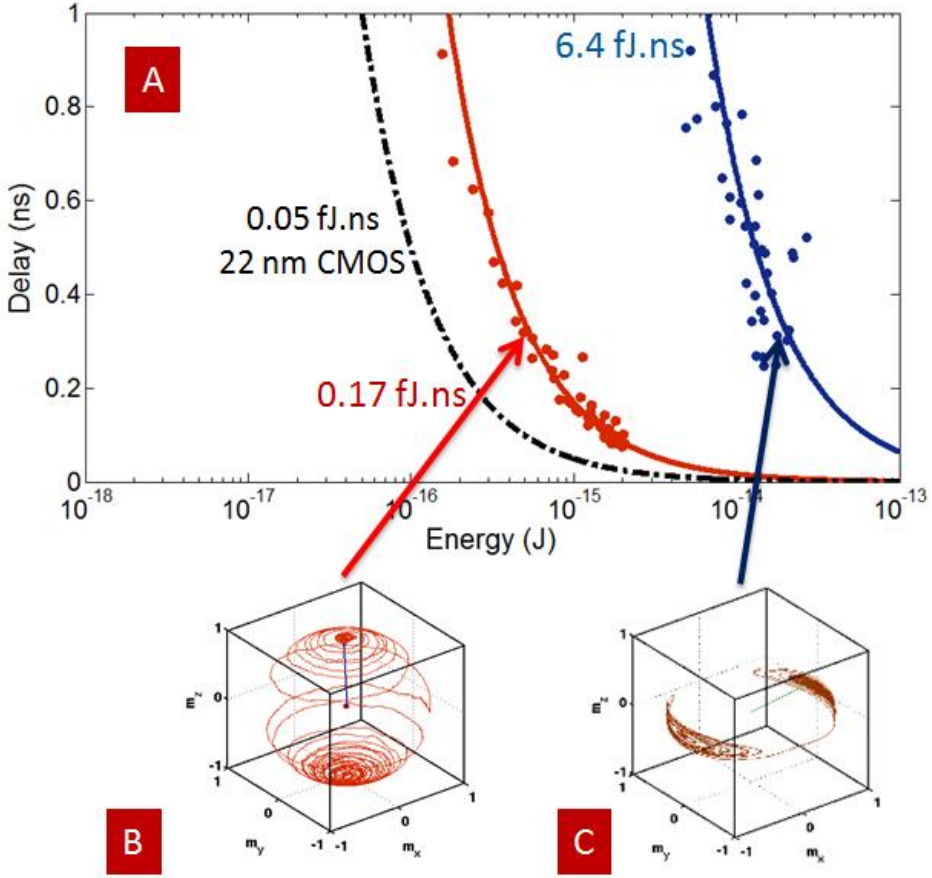
Method 1: Scaling with PMA for Spin Logic Devices

PMA



Inplane





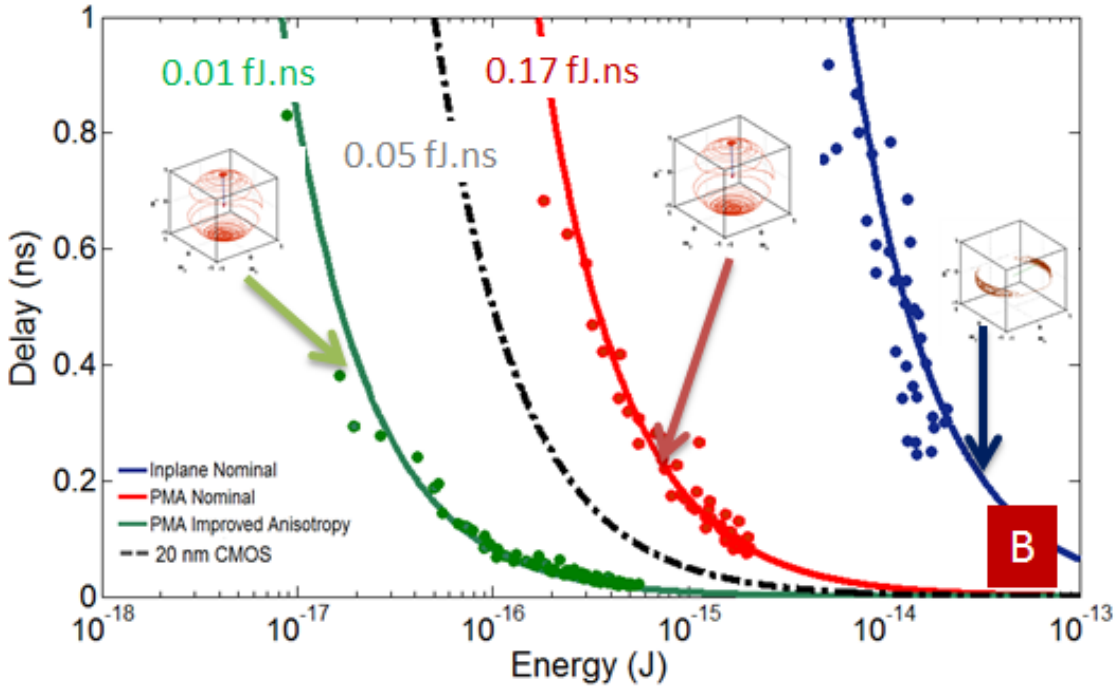
Perpendicular magnetic materials are a wide class of materials with promising performance improvement for area and Energy-Delay

Manipatruni, Sasikanth, Dmitri E. Nikonov, and Ian A. Young. "Material Targets for Scaling All Spin Logic." arXiv preprint arXiv:1212.3362 (2012).

Method 2: Scaling by M_s vs H_k Tradeoff

$$E_b = \frac{1}{2}\mu_0 M_s H_k V$$

Decoupled from M_s in PMA

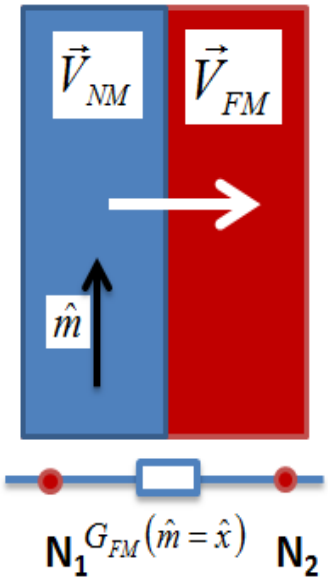


Perpendicular magnetic materials may also enable individual control on M_s and H_k allowing for improved performance.

Manipatruni, Sasikanth, Dmitri E. Nikonov, and Ian A. Young. "Material Targets for Scaling All Spin Logic." arXiv preprint arXiv:1212.3362 (2012).

Method 3: Scaling by Interface Engineering

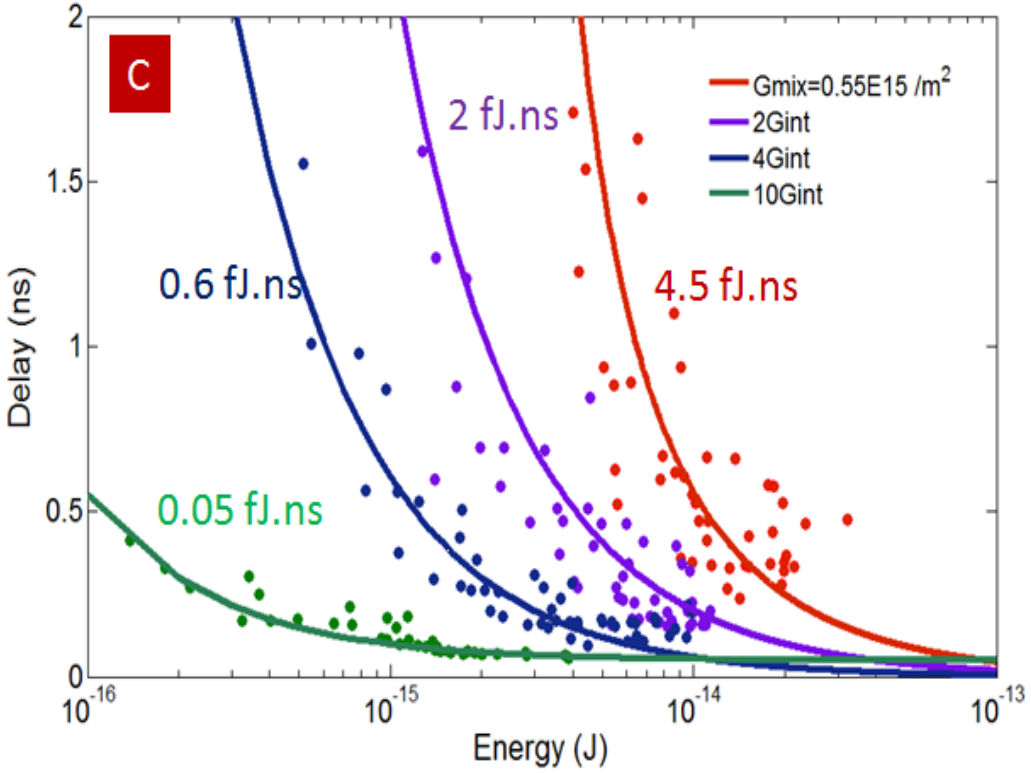
A



B

$$\begin{bmatrix} I_c \\ I_{sx} \\ I_{sy} \\ I_{sz} \end{bmatrix} = \begin{bmatrix} G_{11} & \alpha G_{11} & 0 & 0 \\ \alpha G_{11} & G_{11} & 0 & 0 \\ 0 & 0 & G_{SL} & \sim 0 \\ 0 & 0 & \sim 0 & G_{SL} \end{bmatrix} \begin{bmatrix} V_N - V_F \\ V_{sx} \\ V_{sy} \\ V_{sz} \end{bmatrix}$$

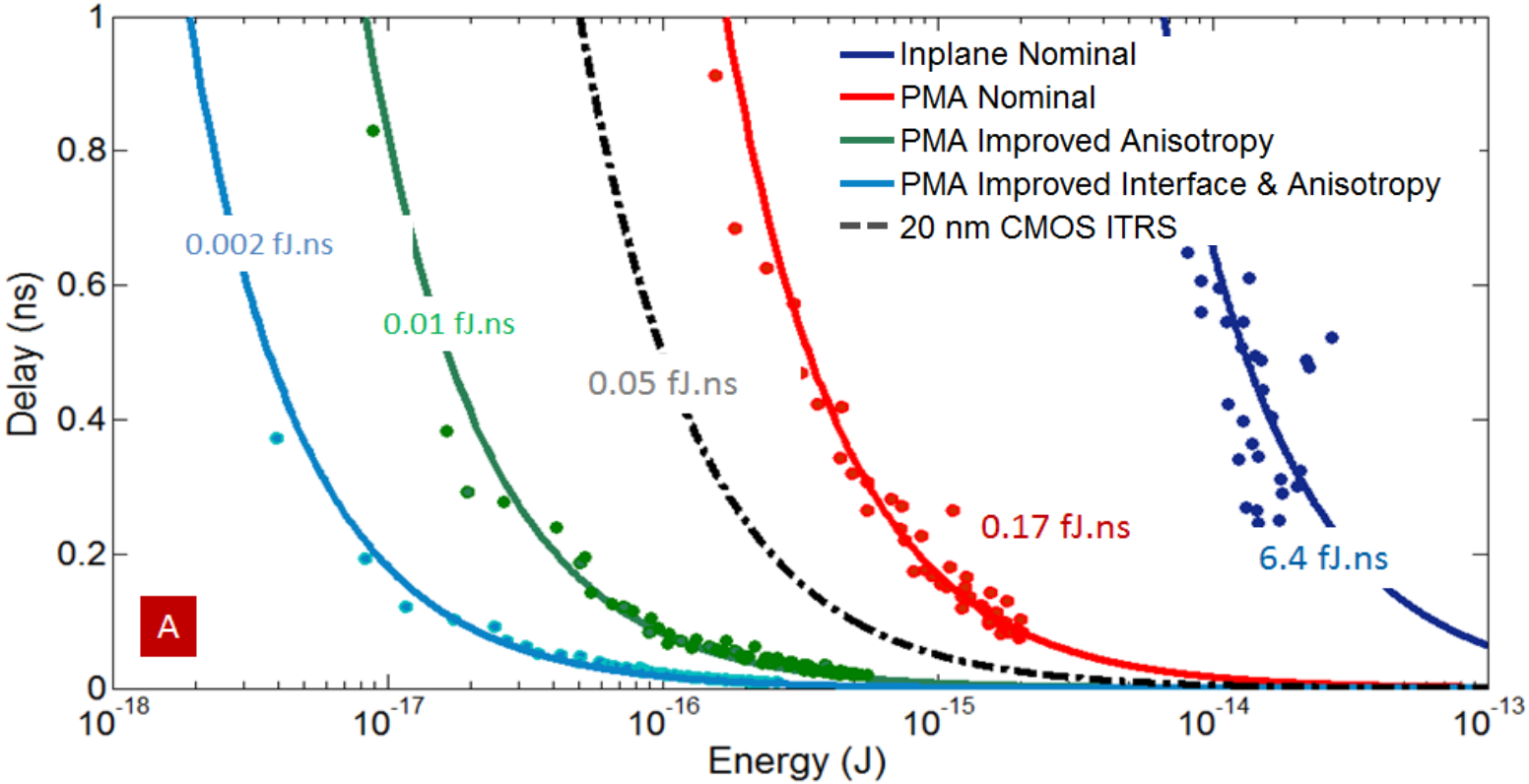
C



Interface properties play a very critical role in the net performance of the device.

Manipatruni, Sasikanth, Dmitri E. Nikonov, and Ian A. Young. "Material Targets for Scaling All Spin Logic." arXiv preprint arXiv:1212.3362 (2012).

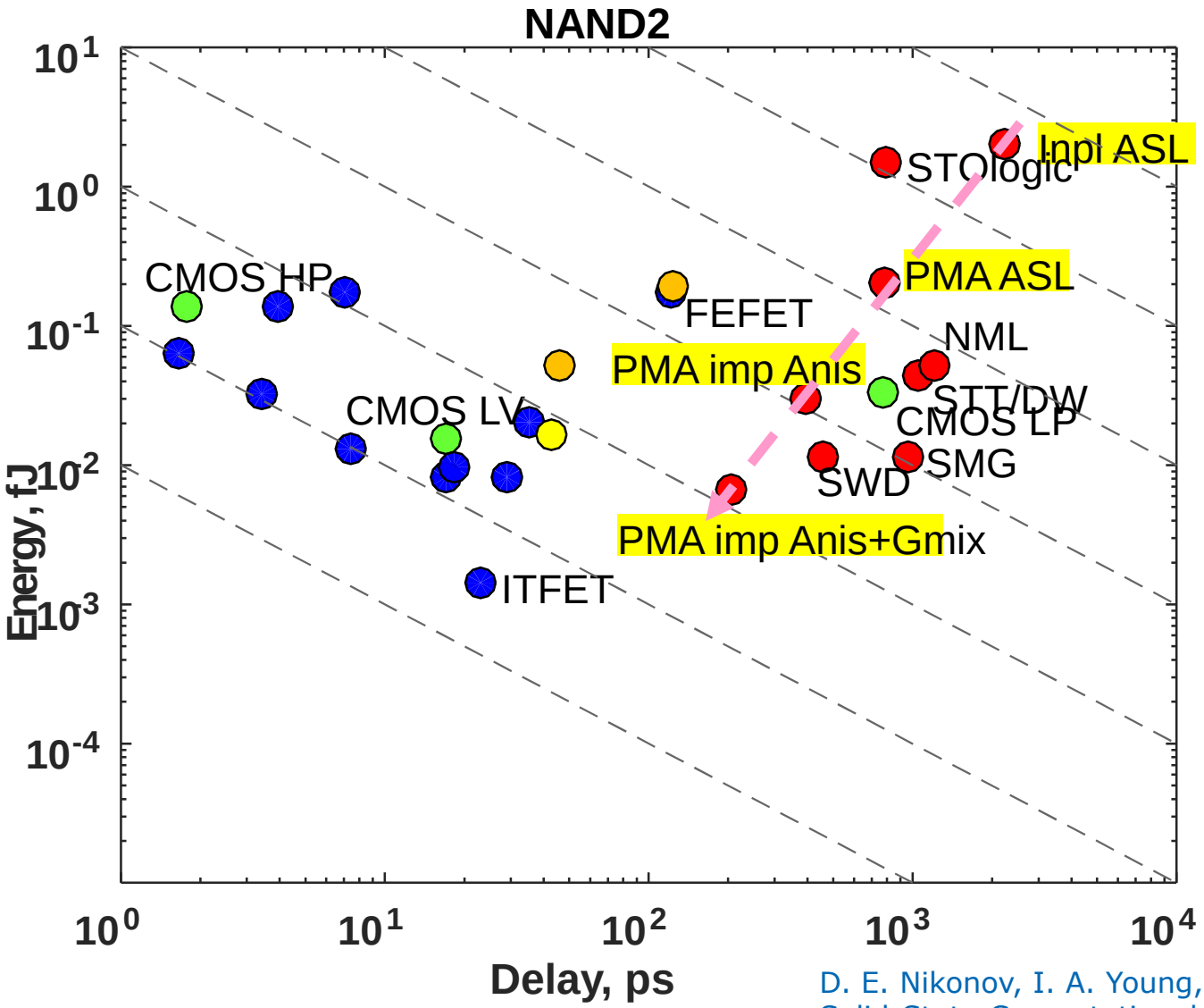
Opportunity for material exploration : ASL Material Scaling Methods



B		In-plane	PMA	Improved PMA	Improved PMA + Interface
Energy-delay	aJ.ns	6400	170	10	2
M_s	(A/m)	10^6	10^6	$250X10^3$	$250X10^3$
H_k	(A/m)	$3X10^4$	$4X10^4$	$16X10^4$	$16X10^4$
$G_{spin-mix}$	($\mu m^{-2}\Omega^{-1}$)	550	550	550	2200

Reference: Manipatruni, Sasikanth, Dmitri E. Nikonov, and Ian A. Young. "Material Targets for Scaling All Spin Logic." arXiv preprint arXiv:1212.3362 (2012).

ASL Imporvement



CMOS ref

Electronic

Spintronic

Ferroelectric

Orbitronic

Straintronic

D. E. Nikonov, I. A. Young, IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2015

Exploring Spin Logic Devices

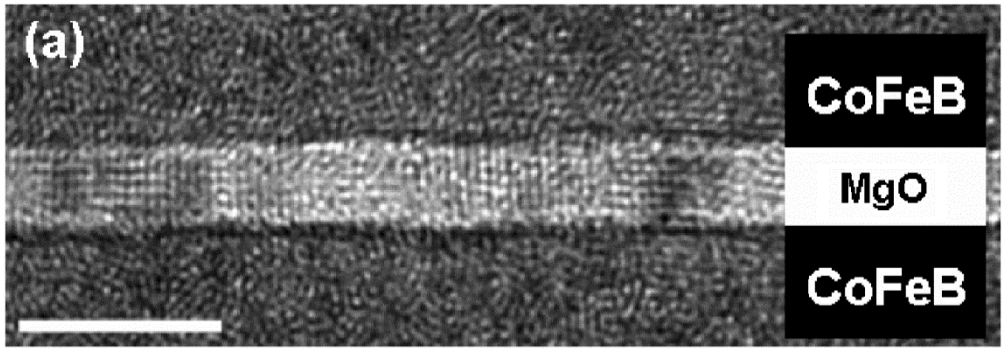
1. Modeling the spin devices and circuits

2. Extracting the scaling methods for spin logic (using 1)

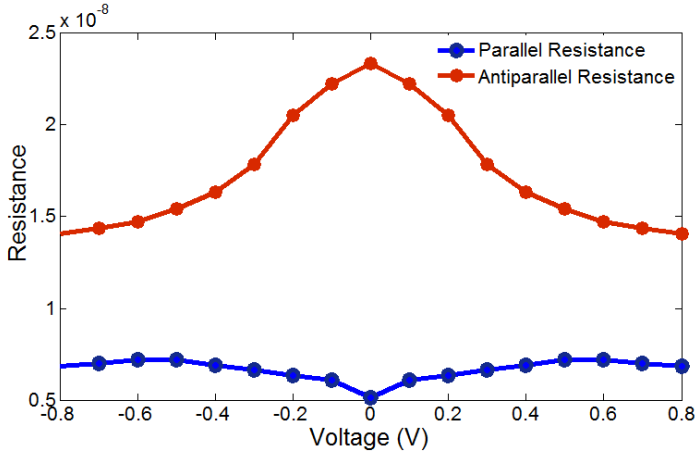
3. Realizing the materials and interfaces (guided by 2)

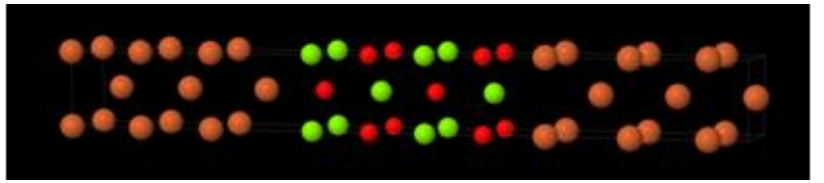
Materials and Interfaces Play A Critical Role in Spin Devices

Example 1 : Δ_1 spin filtering in MgO



Appl. Phys. Lett. **91**, 062516 (2007)



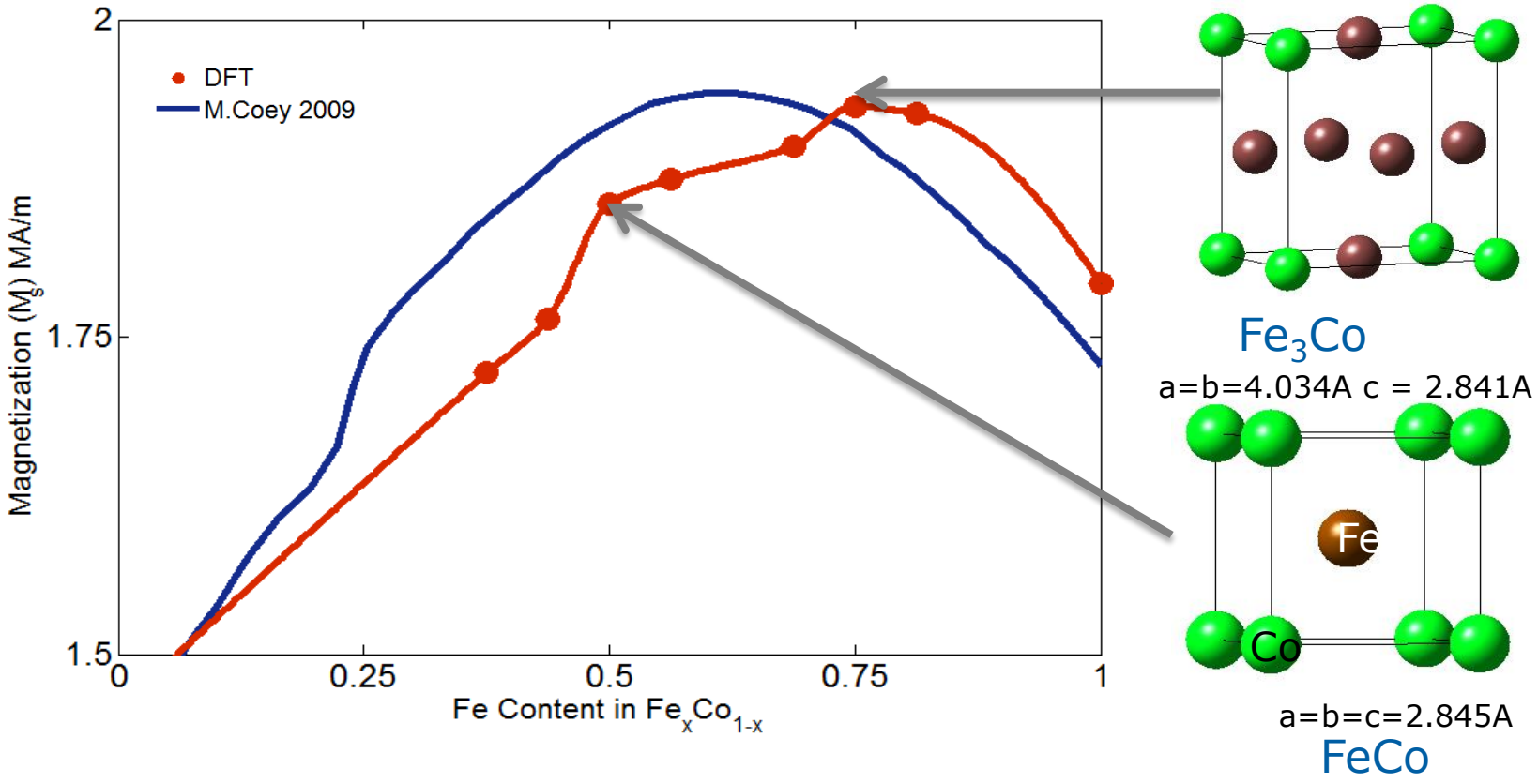


Ab-initio models with strong experimental co-ordination is essential to discover and engineer spintronic materials for devices.

Nature Materials 3, 868 - 871 (2004) *A. Roy, D. Nikonov, I.A. Young, JAP 2011*

Materials And Interfaces Play A Critical Role in Spin Devices

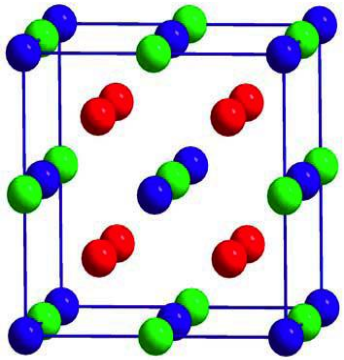
Example 2 : Sensitivity in Fe-Co Phase diagram



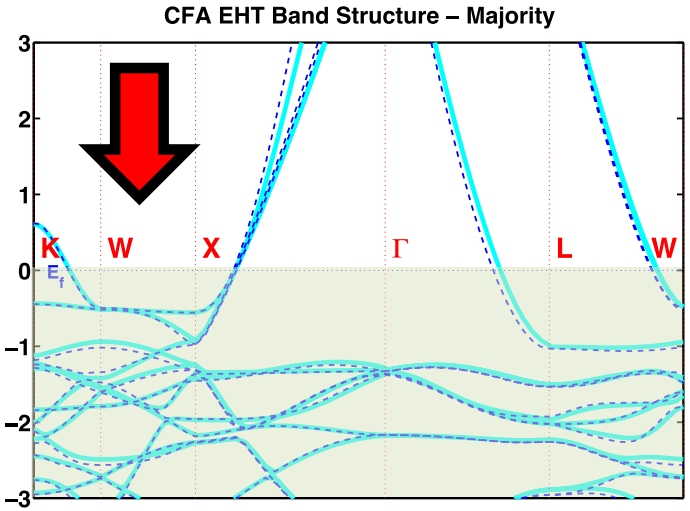
Ab-initio models with strong experimental co-ordination is essential to discover and engineer spintronic materials for devices.

3. Improving All Spin Logic with New Materials

Heusler Alloys : Magnetic Material For Scaled Spin Valves

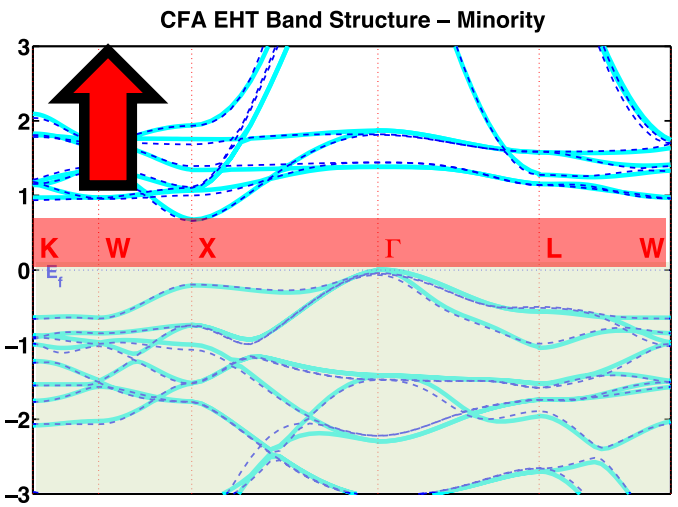


X_2YZ



Majority band structure

From DFT+U (solid) and EHT (dashed)



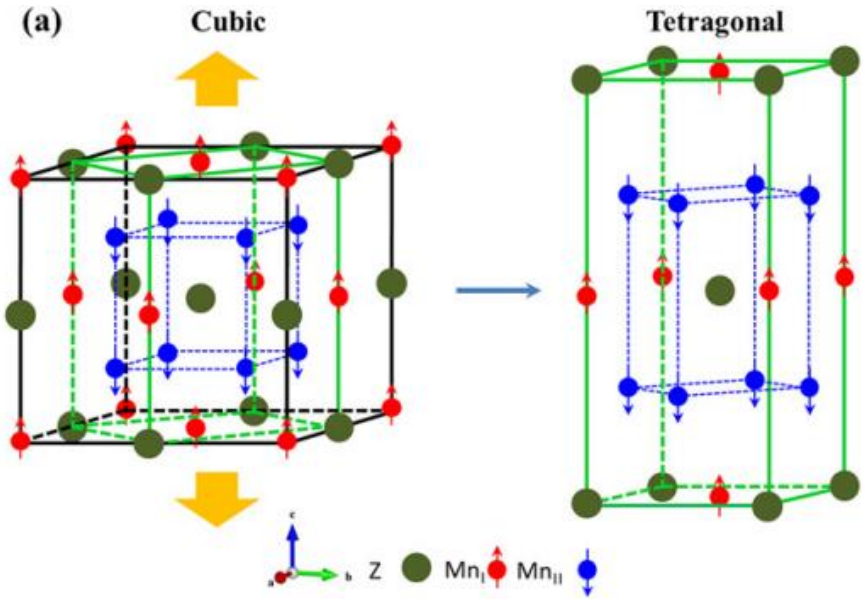
Minority band structure

From DFT+U (solid) and EHT (dashed)

Heusler alloys enable high intrinsic spin polarization 70 % - ~100%
<u>Without</u> the need for tunneling electrodes.
Path for highly scaled (10 nm dots) with RA < 0.1 Ohm.um²

EHT Modeling of Transport in Heusler spin devices, G. Shine et al SISPAD 2014

Heusler Alloys: Magnetic Material Mn_3Ga For Scaled Spin Valves



partial magnetic moments (Bohr magnetons):

Atom	s	p	d	total
Mn#1	-0.037	-0.030	-2.692	-2.759
Mn#2	0.018	-0.014	2.224	2.255 x2
Ga	-0.020	-0.032	0.004	-0.048

Magnetic moment :
VASP* calc. = 1.745 μ_B

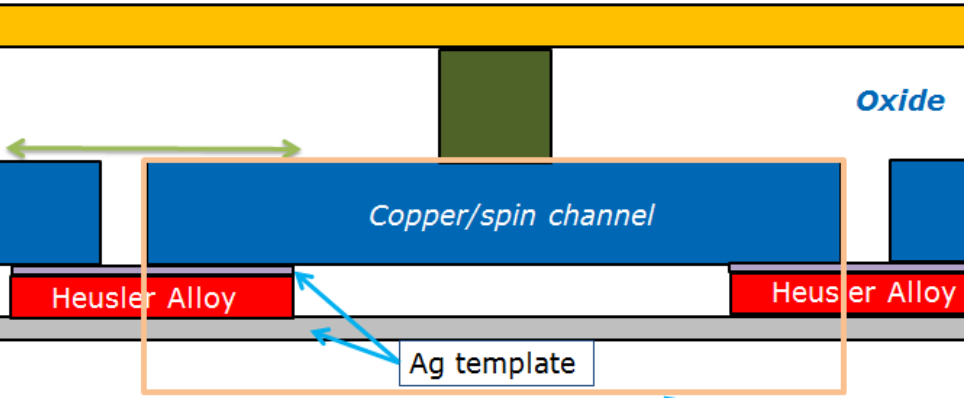
* DFT tool

- High PMA due to tetragonal structure
- Low Ms Due to compensation.

Heusler alloys enable
1. High intrinsic spin polarization -> 70 % - ~100%
2. High perpendicular magnetic anisotropy (H_k> 10000 Oe)
3. High injection efficiency with no tunnel barrier

EHT Modeling of Transport in Heusler spin devices, G. Shine SISPAD 2014

Heusler Alloy Magnetic Devices for Spin Logic

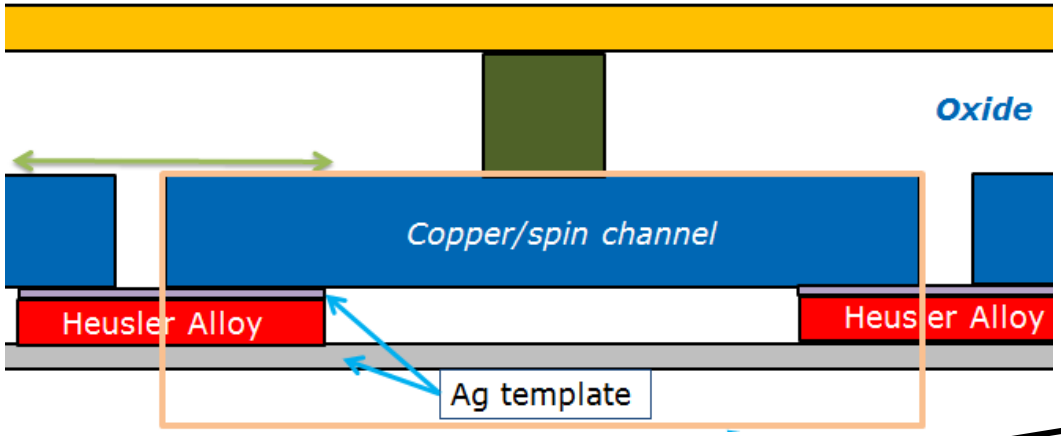


Material	GMR/TMR	H_k
CoFeB	*-/100-200%*	3000 Oe
Co_2FeAl	*-/650%*	1000 Oe
$CoFe_2Si$	-	1000 Oe
$Co_2FeAl_{0.5}Si_{0.5}$	20 %/*800%*	1000 Oe
$Co_2Mn_{1.29}Al$	*-/1100 %*	1000 Oe
$Mn_{3-x}Ga$	-	10000 Oe
$Co_2FeGe_{0.5}Ga_{0.5}$	40 %	1000 Oe
$Co_2Mn(Ga_{0.25}\ Ge_{0.75})$	12.2 %	1000 Oe
$Co_2Fe_{0.4}Mn_{0.6}Si$	70 % GMR	1000 Oe

Need to integrate Heuslers in MRAM and Spintronics for
1. Low Ms and high Hk -> Improved retention / Write Error rate
2. Improve spin Polarization -> higher GMR
3. Lower RA to enable voltage scaling
➢ *VALUE PROPOSITION FOR HEUSLERS*

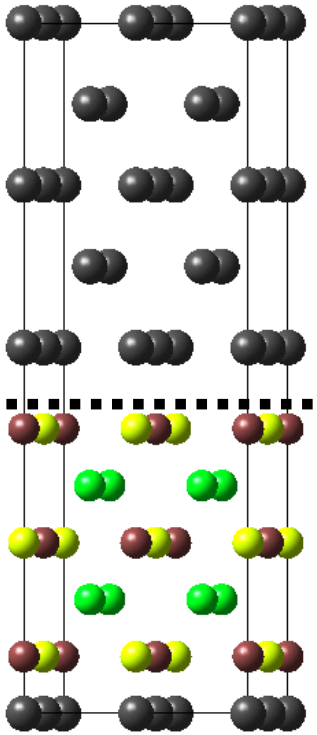
Appl. Phys. Lett. 100, 052405 (2012)

Heusler Alloy Magnetic Devices for Spin Logic

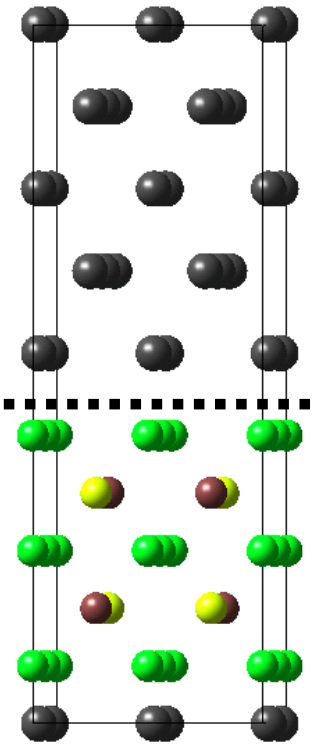


Ag FCC a=4.05 A
225 space group

CFGG a=5.737 A
a/sqrt(2)=4.067 A
225 space group



Co-Fe/GeGa (CFGG) interface



Co-Ag interface

Atomistic modeling shows the potential
1. CFGG/Ag good interface alignment like CoFeB/MgO.
2. Need GMR research with Heusler alloys on metals

An Outlook for scaling MRAM/Spin Logic

For PMA, Dot size sets H_k

$$E_b = \frac{1}{2}\mu_0 M_s H_k t(volume)$$

Nominal
$M_s = 10^6$ A/m

$$\longrightarrow \quad H_k$$

RA scaling - Dot Scaling

$$R_p = \frac{4RA}{\eta_{round}\pi d^2}$$

$$\longrightarrow \quad RA$$

Voltage scaling

$$V_{Ap-MTJ} = \frac{4(RA)}{\eta_{round} d^2}\left(1 + TMR(V)\right) I_{drive} \leq 0.9V$$

Polarization loss around 0.9V

Resistance of MTJ scales with d^2 at fixed RA.
Write voltage (AP-P) scales as square of dot diameter at fixed RA.

A Heusler based Outlook for scaling MRAM/Spin Logic

For PMA, Dot size sets H_k

$$E_b = \frac{1}{2}\mu_0 M_s H_k t(volume) \longrightarrow \frac{M_s}{n} \quad nH_k$$

RA scaling - Dot Scaling

$$R_p = \frac{4RA}{\eta_{round}\pi d^2} \longrightarrow RA_{GMR} < \frac{RA_{TMR}}{10}$$

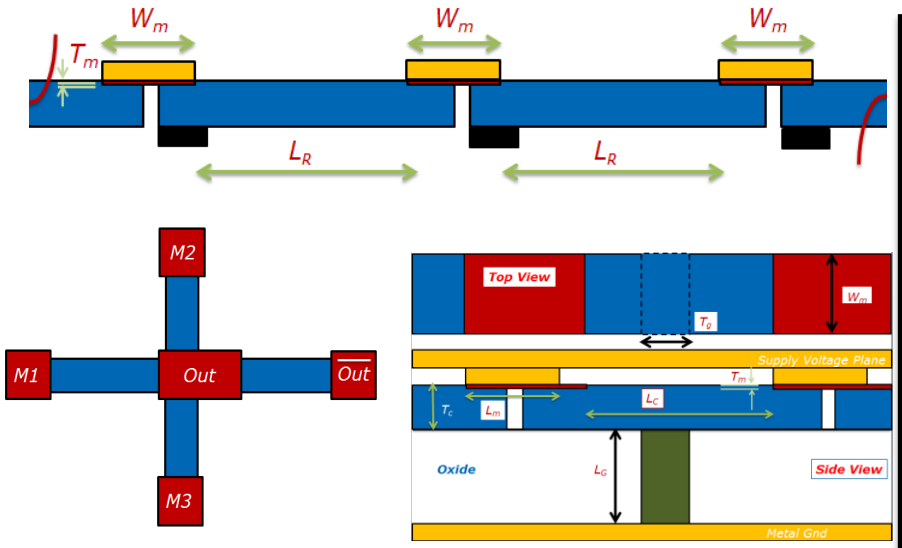
Voltage scaling

$$V_{Ap-MTJ} = \frac{4(RA)}{\eta_{round} d^2}\left(1 + GMR(V)\right)I_{drive} \leq 0.1V$$

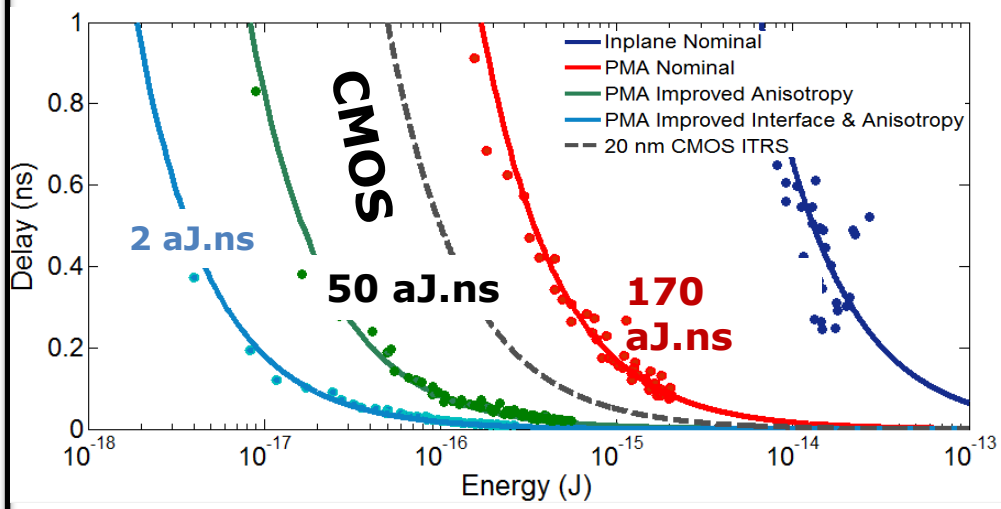
Polarization loss around 0.1V

The above described Heusler alloy scaling path may provide a way to continued scaling.

Conclusion



Components for all spin logic

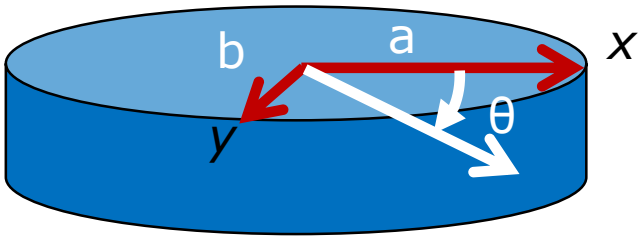


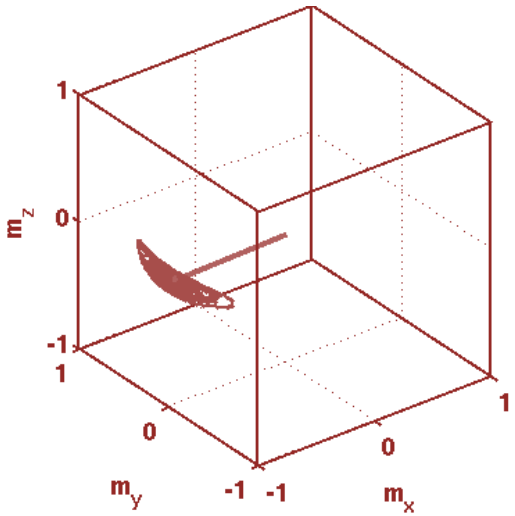
- Functional blocks for an all spin logic exist & are verified by simulations.
- Material optimization may enable ASL energy-delay comparable with CMOS with added non-volatility & logic efficiency.
- Material and interface understanding with ab-initio models and experiments are the key to enabling spin logic.

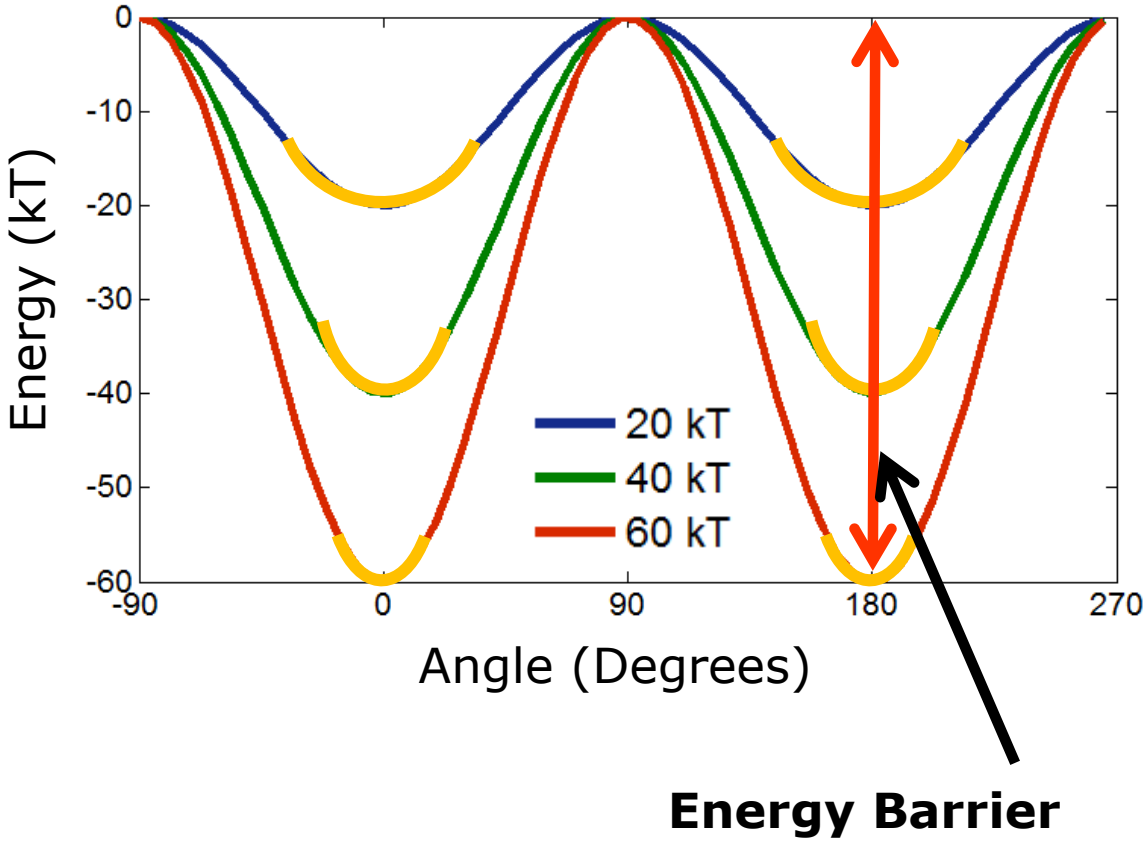
…..and one more thing!

Non-volatility for Embedded Memory and Logic:

Magnetic Energy Landscape and Noise

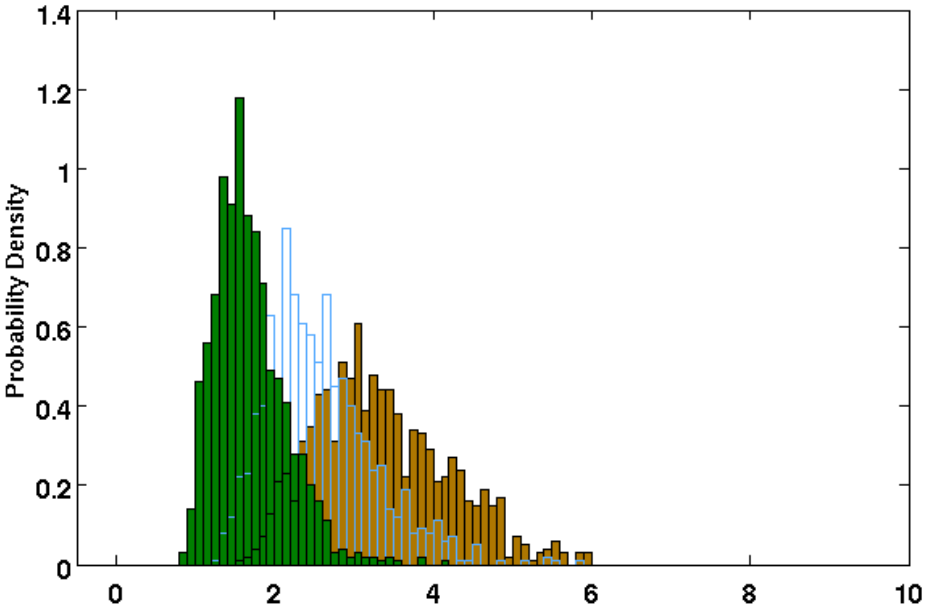




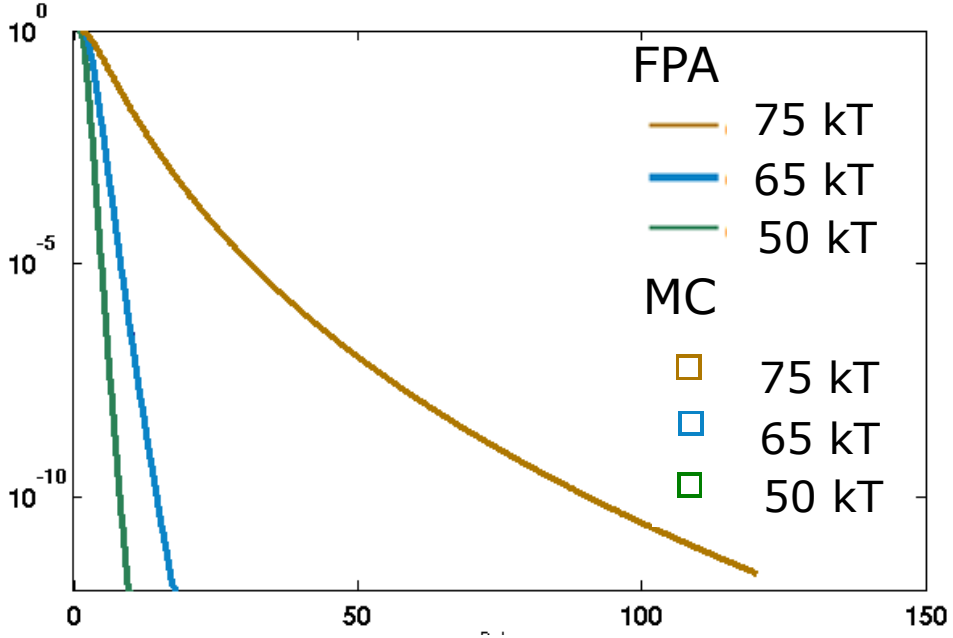


Origin of the magnetic retention/write/read failure is thermal noise which continuously perturbs the magnet's internal field.

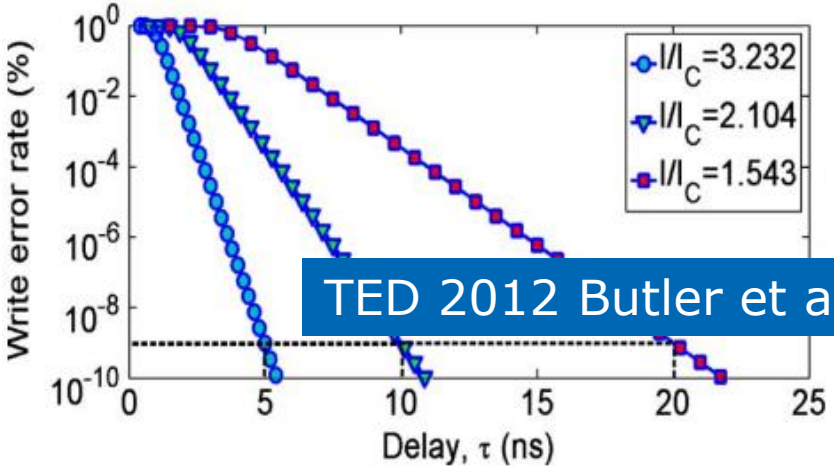
Switching Speed of MRAM/STT Comprehending Dynamic Variations



Write Time Distribution



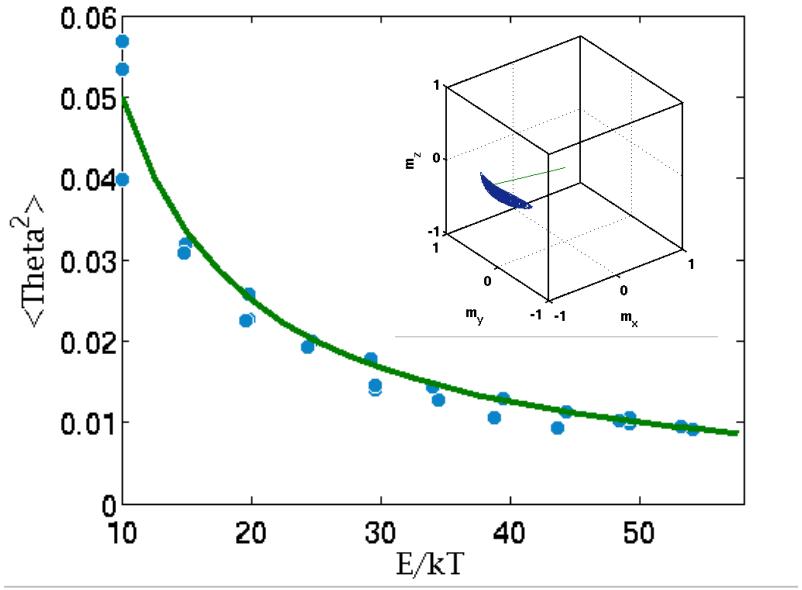
Write Error Rate
Monte-Carlo & Fokker-Planck

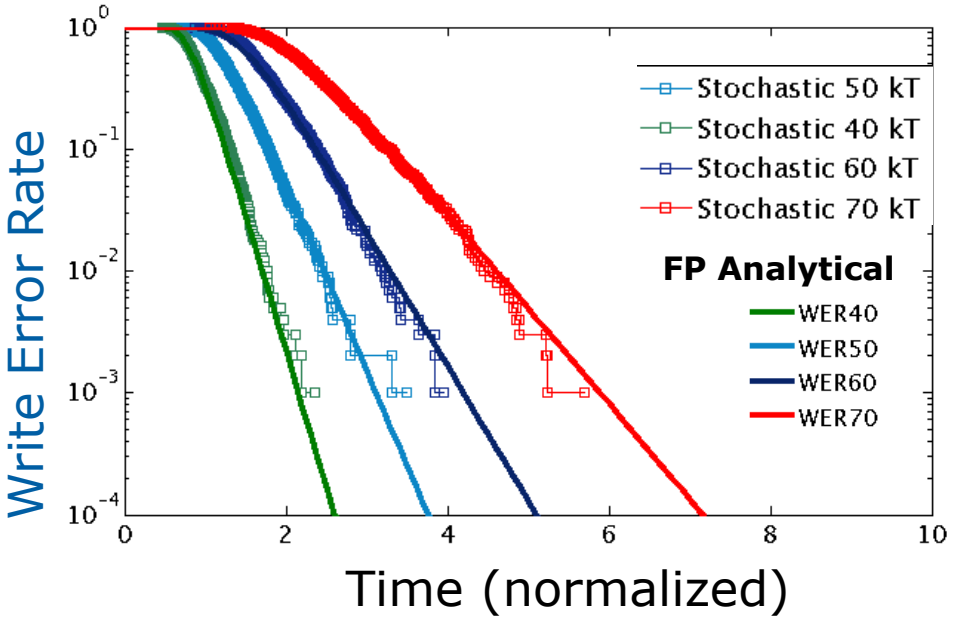


TED 2012 Butler et al

Dynamic variations set the switching Speed for MRAM.

Modeling Langevin Noise: Write Error Rates





$$\frac{\partial m_1}{\partial t} = -\gamma\mu_0[m_1 \times \bar{H}_{eff}] + \alpha\left[m_1 \times \frac{\partial m_1}{\partial t}\right] - \frac{1}{eN_s}(m_1 \times m_1 \times \bar{I}_{s1})$$

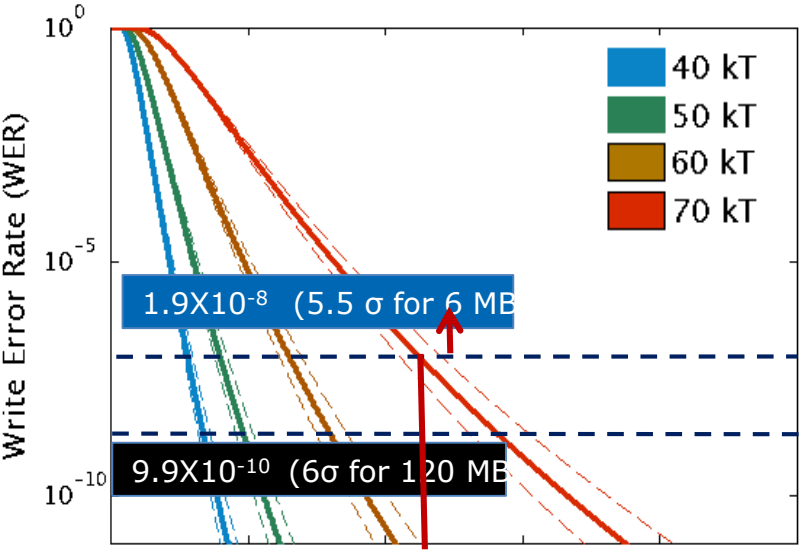
$$\bar{H}_{eff}(T) = \bar{H}_{eff} + Noise$$

$$\tau = \frac{\tau_0 \ln(\pi/2\theta_0)}{(I/I_c - 1)}$$

Butler, Fischer et al TMAG Dec 2012

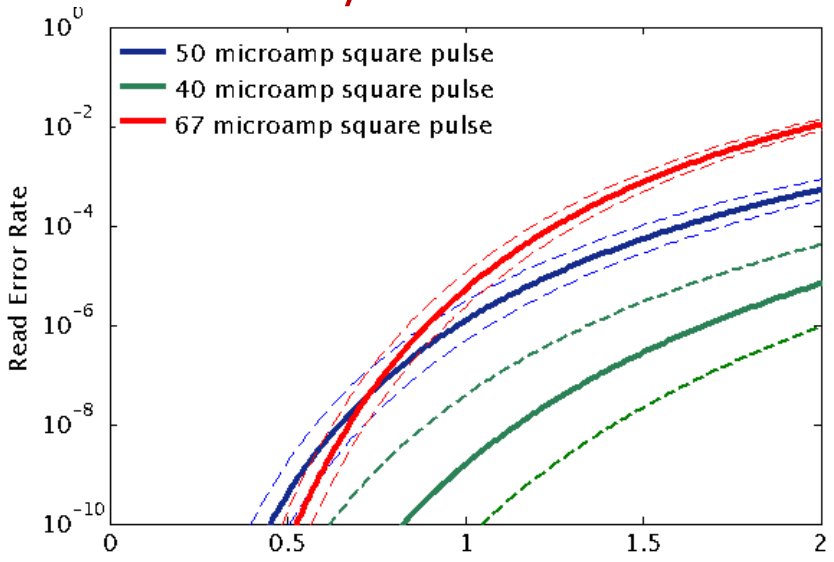
Langevin Noise model provides a strong variability limitation to MTJ operating speed.

Write and Read Error Rates in STT/MRAM



Write Pulse Width (normalized)

Write Error Rate



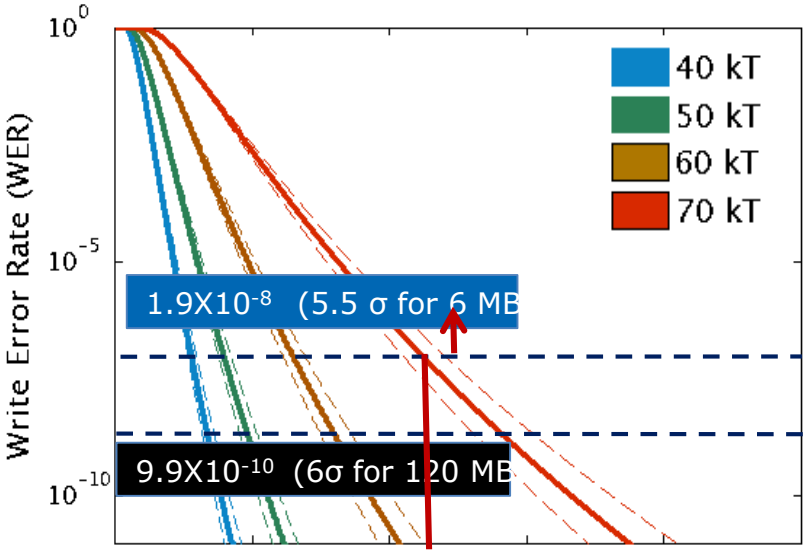
Read Pulse Width (normalized)

Read Error Rate

Dynamic variations can be a significant factor in the performance of spin logic/memory. Accurate modeling is required to quantify and mitigate.

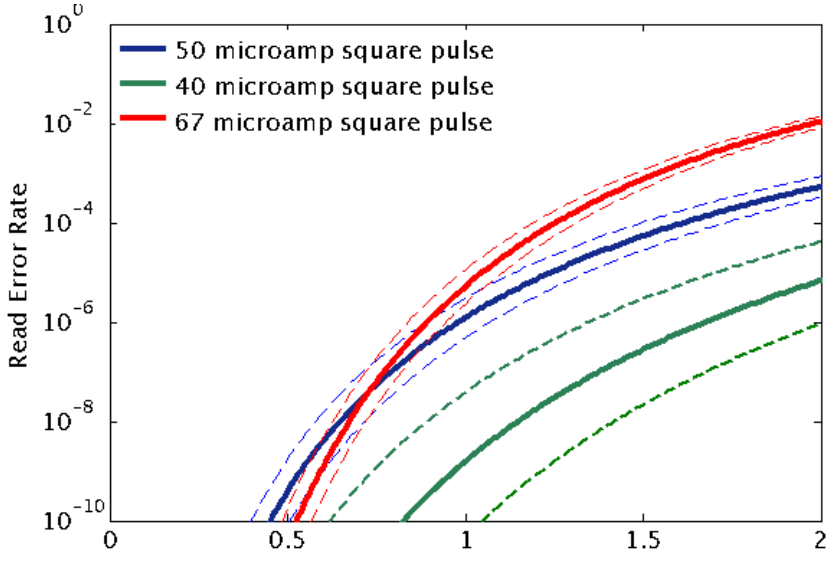
e.g. Butler, Fischer et al TMAG Dec 2012

Write and Read Error Rates in MRAM



Write Pulse Width (normalized)

Write Error Rate



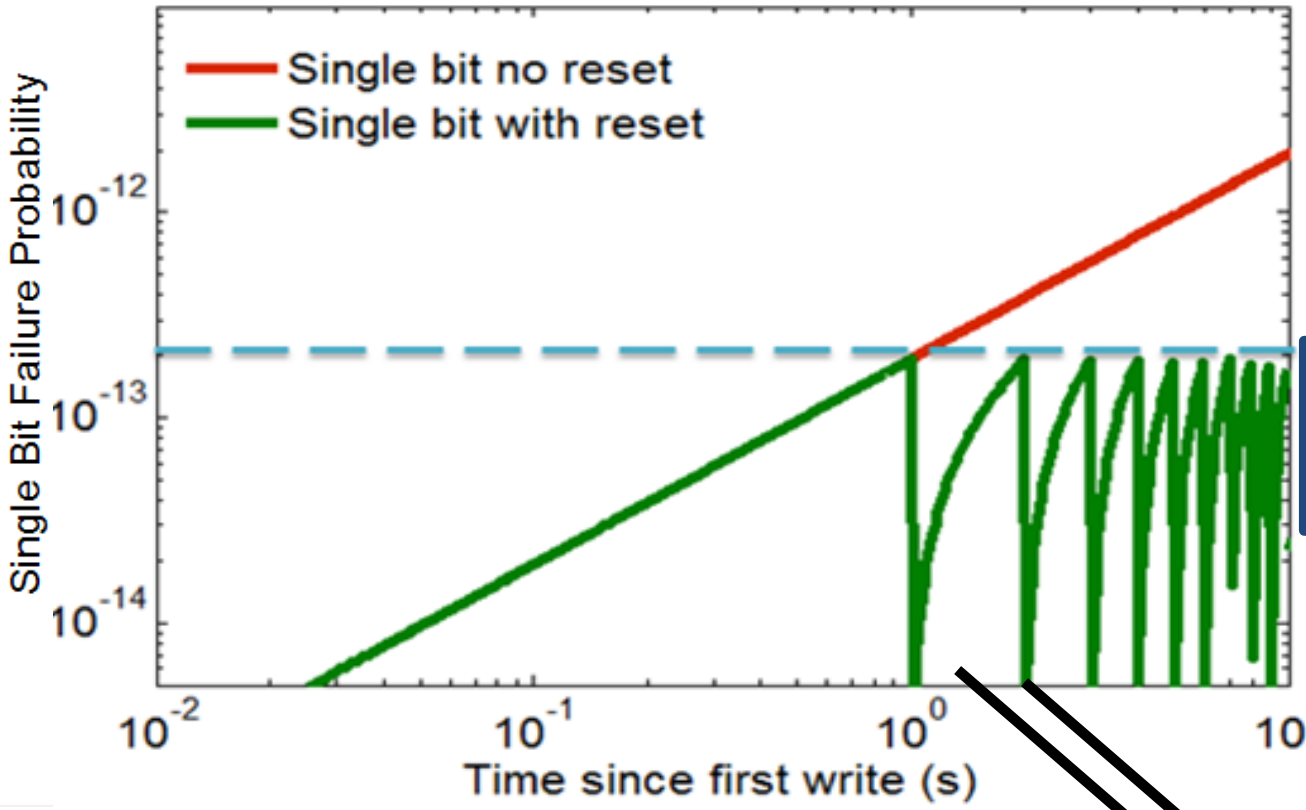
Read Pulse Width (normalized)

Read Error Rate

Write and read of an MRAM bit is not ideal. A simple reset would not be sufficient. Hence a quantitative scheme for retention error management is necessary.

e.g. Butler, Fischer et al TMAG Dec 2012

Resetting MRAM can enable low retention failure rate



Example failure target

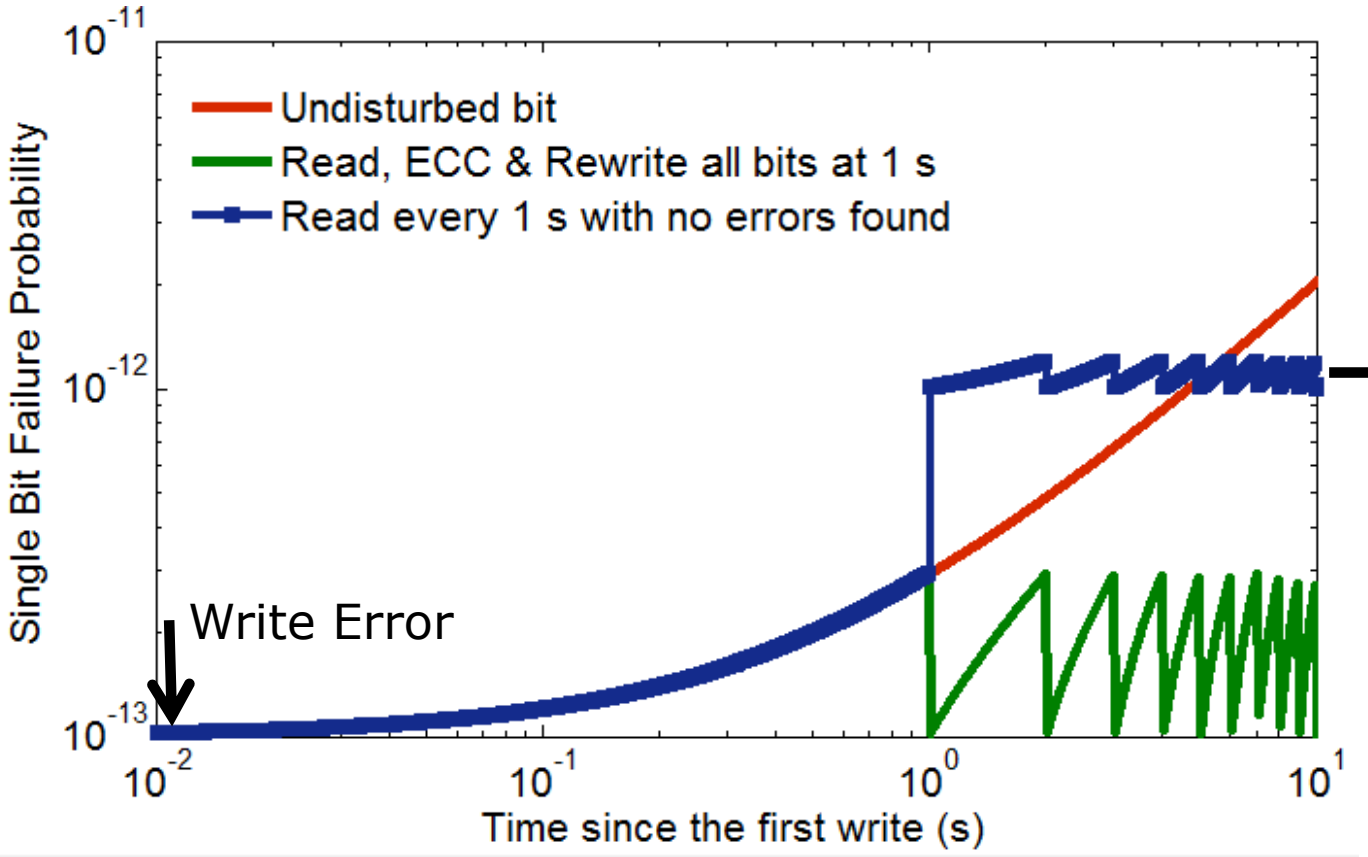
Ideal Scenario with Ideal reset
Assuming WER=0, RER=0

Resetting the probability every 1 s

Finite read error rate and finite write error rate complicate the scenarios.

Manipatruni, Nikonov, Young MMM 2015

(Scenario 1) *Resetting* MRAM: RDR>WER



RER of 10^{-12}
WER of 10^{-13}

Case 1 (RDR > WER): read, ECC and Rewrite of all bits is preferred.

Manipatruni, Nikonov, Young MMM 2015

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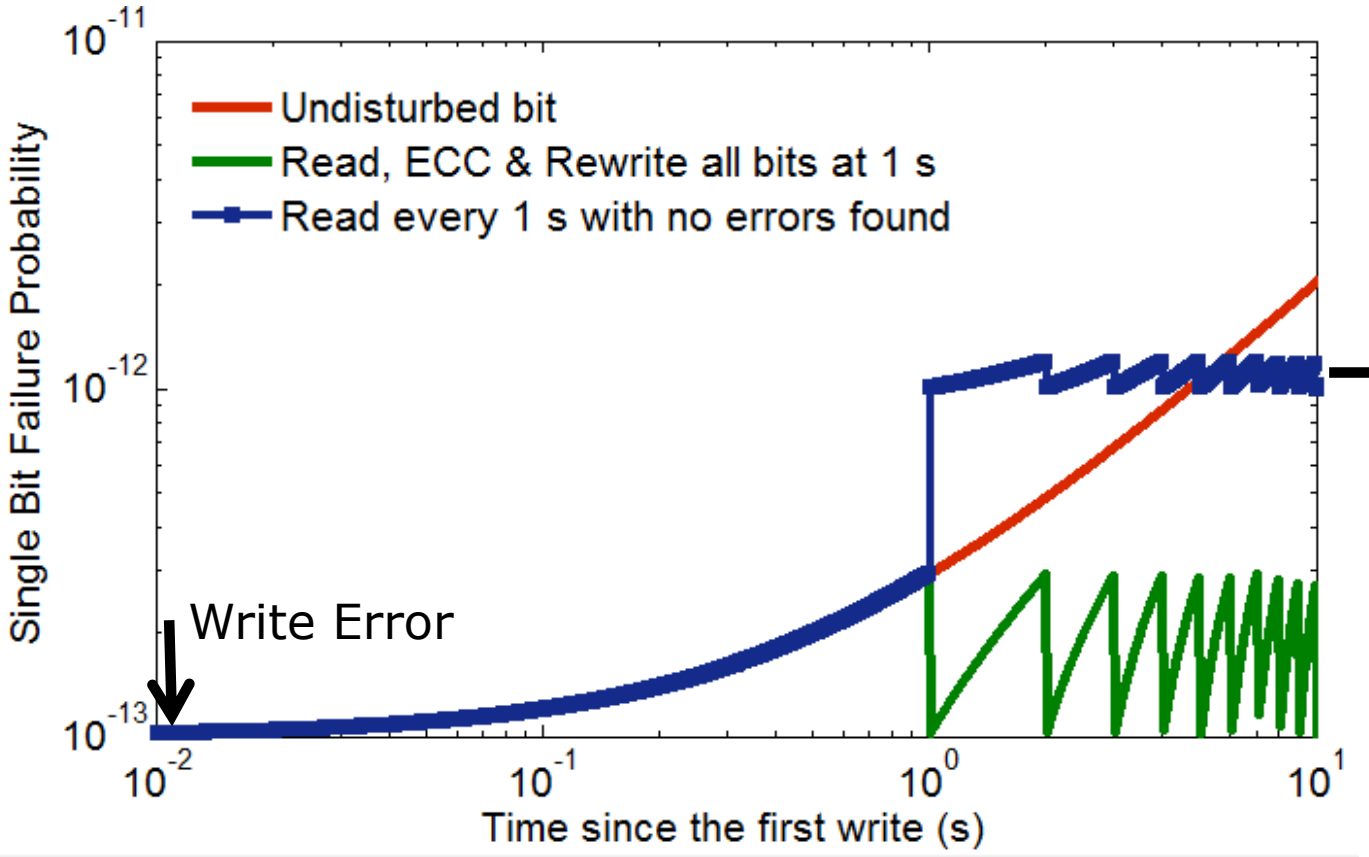
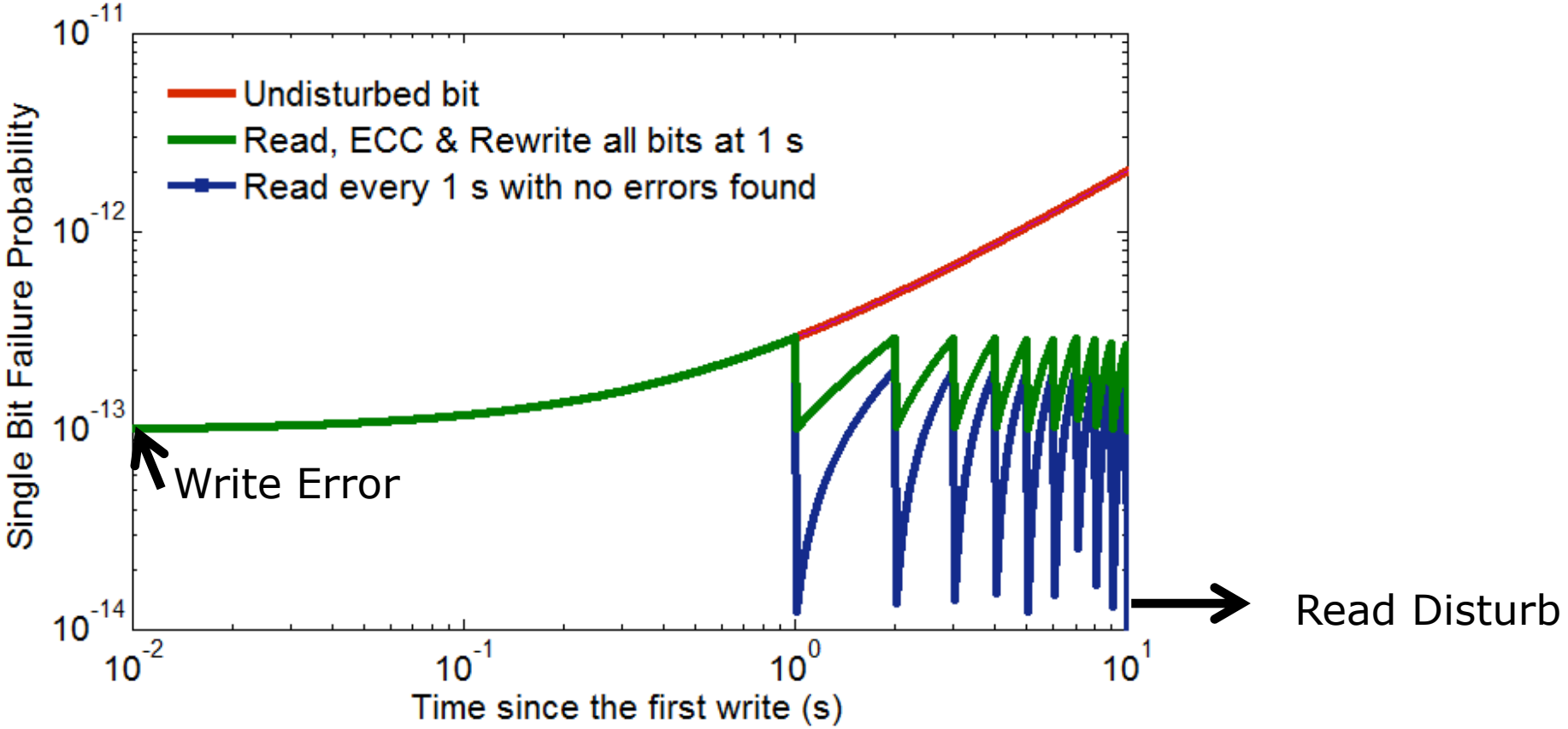


RER of 10^{-12}
WER of 10^{-13}

If (RDR > WER): read, ECC and Rewrite of all bits is preferred.
This is highly energy inefficient.

Manipatruni, Nikonov, Young MMM 2015

(Scenario 2) *Resetting* MRAM: RDR<WER

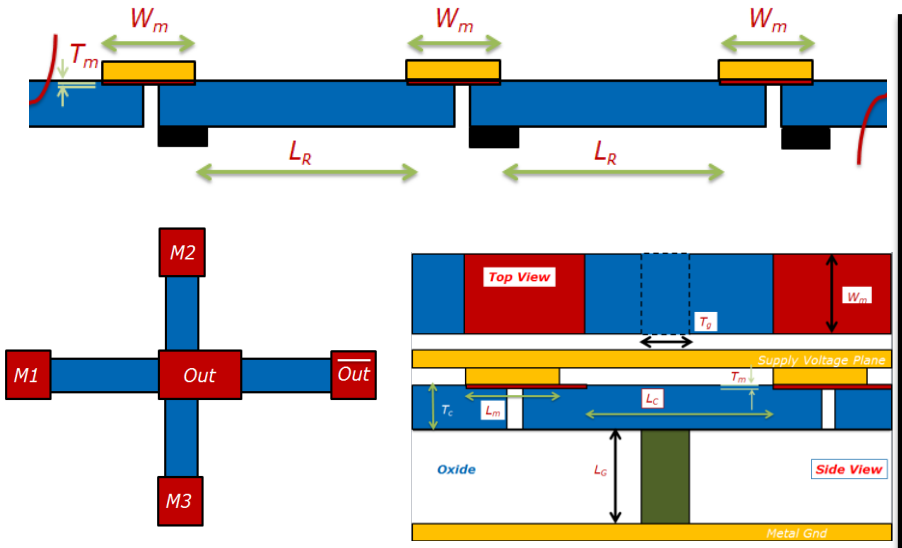


RER of 10^{-14}
WER of 10^{-13}

Case 2 (RDR<WER) : Read, ECC and Rewrite of the failing bit only is preferred.
If RDR < WER, an energy efficient method for MRAM reset can be implemented.

Manipatruni, Nikonov, Young MMM 2015

Conclusion



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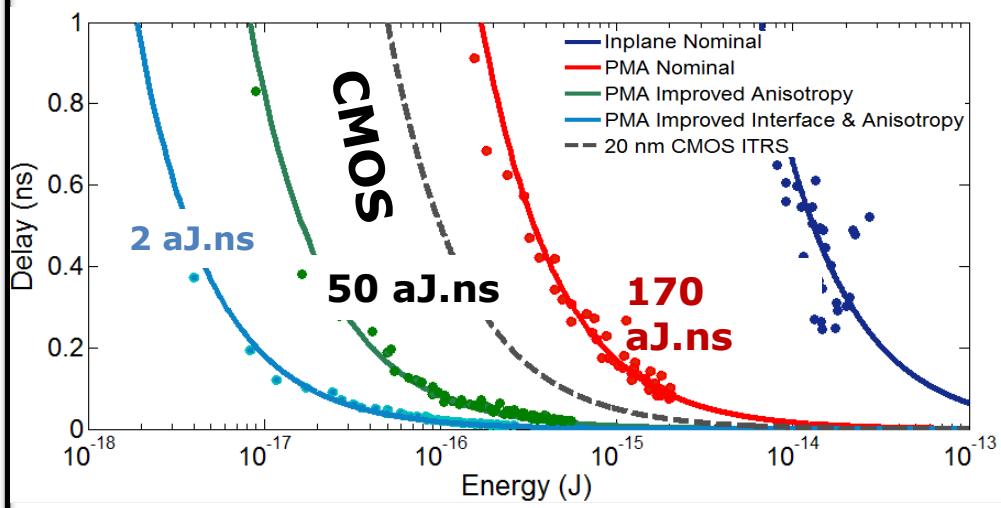

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