Hybrid CMOS + Spintronics for the Next Big Leap in Energy Efficient Computing

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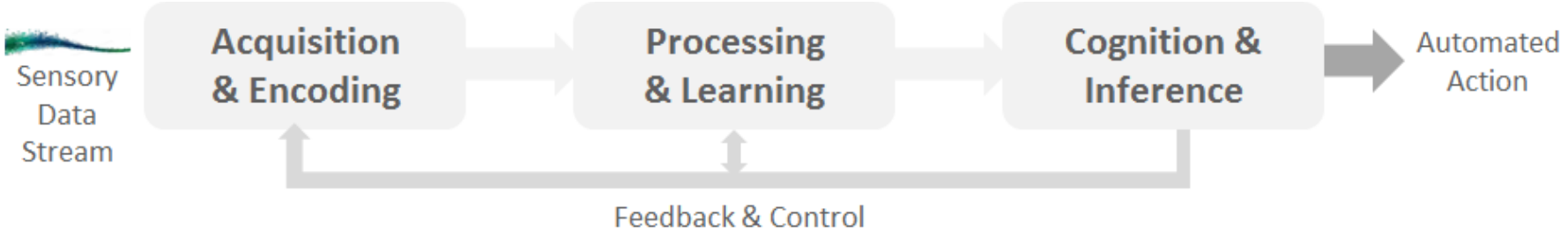
Intel Labs

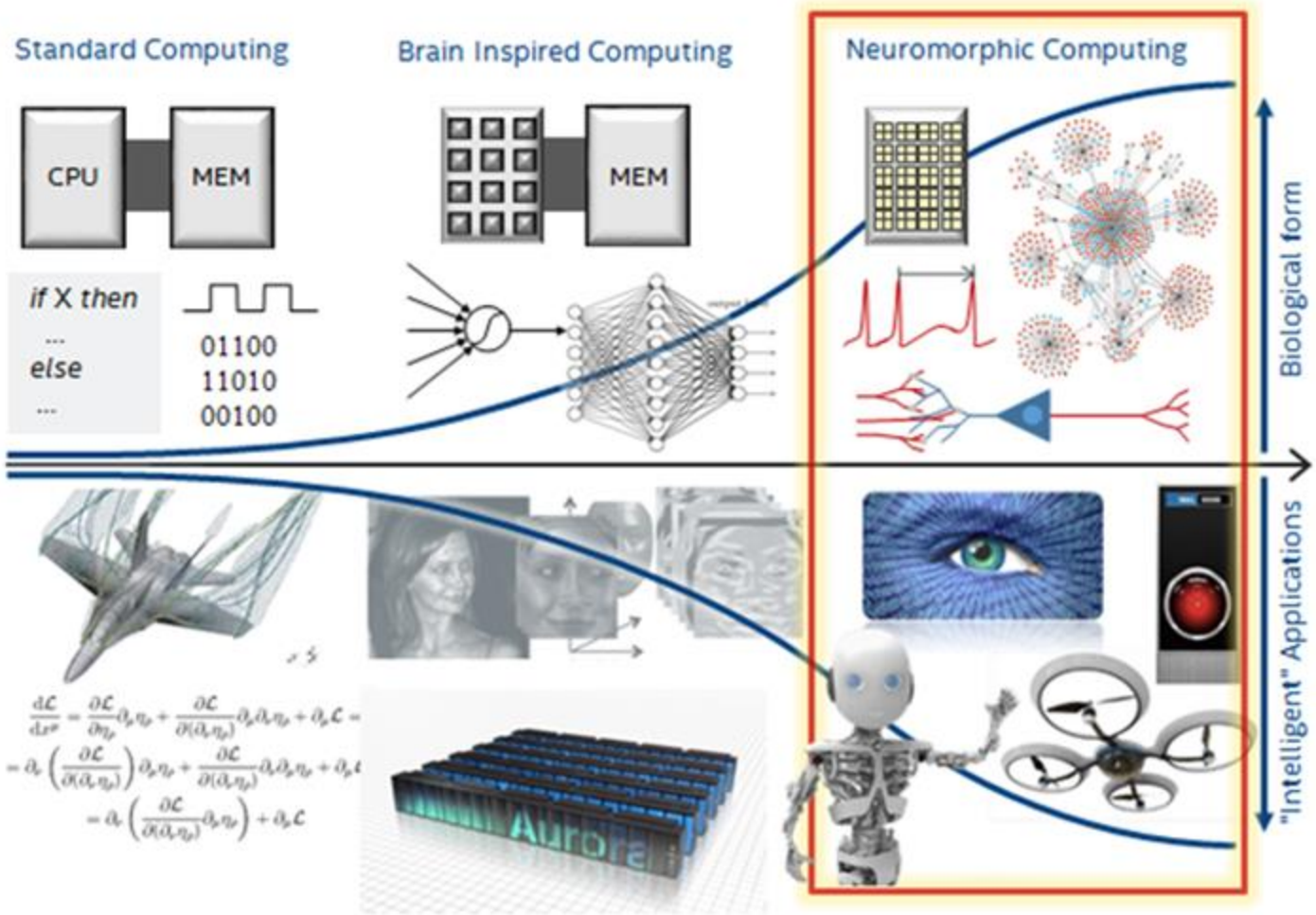
Workshop on the Future of Spintronics
June 5, 2016

The Internet of Everything (IoE)



Paradigm shifts across architecture, circuits, design & technology

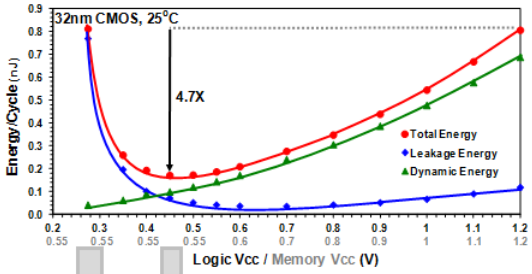
Universal-Scalable-Efficient Cognitive Computing



Exploit Moore's Law integration, spike timing, sparsity & resiliency

Voltage Scaling & Variation Tolerance

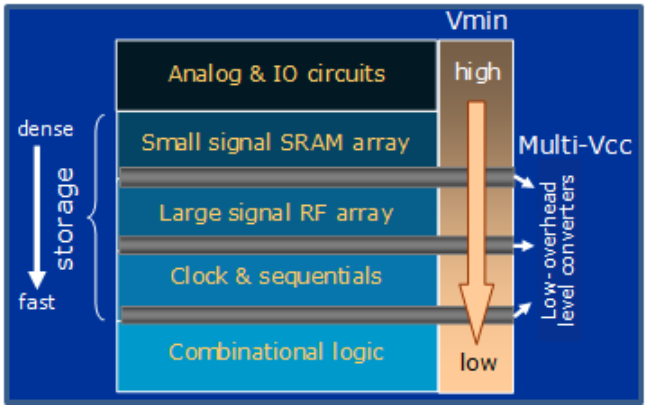
Near Threshold Voltage (NTV)



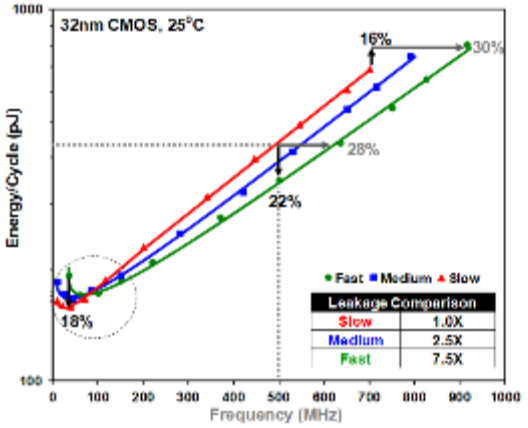
NTV operation for peak energy efficiency

Minimum core voltage limited by circuit functional and timing failures from process variations and noises

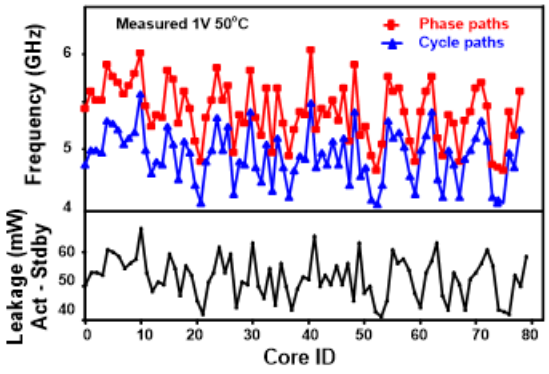
Multi-Voltage Design

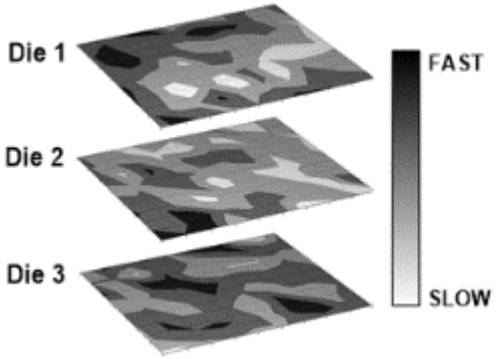


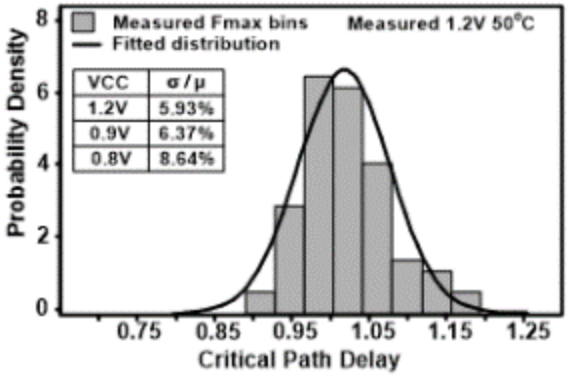
NTV & Variability



Within-Die & Die-to-Die Variations



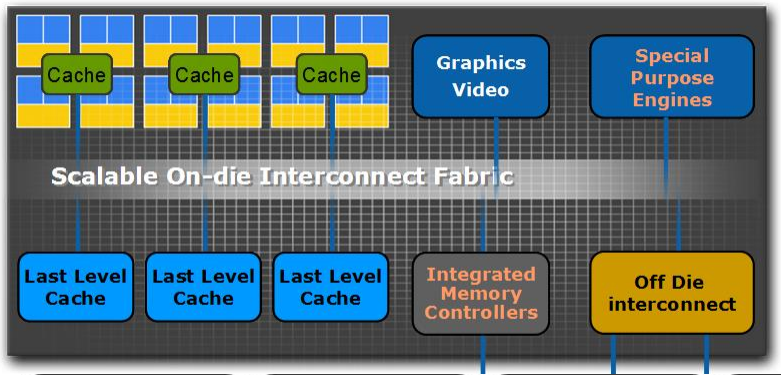


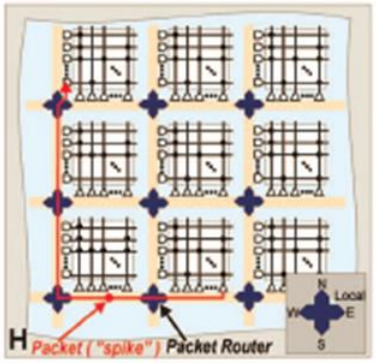


Variation-tolerant NTV design essential for energy efficiency

Fine-Grain Power Management

Autonomous Power Control





Independent V/F control regions

Scenario-based power allocation

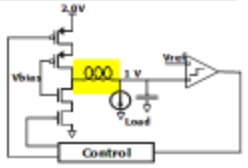
Dynamic V/F control

Fine-grain sleep & wake-up

Spike rate control via homeostasis

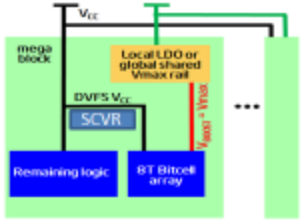
Fine-Grain & Scalable Integrated Voltage Regulators

LCVR
- High efficiency
- Off-die inductor
- Continuous Vout
- Large domains
- Fast response



Off-die inductors
All circuits on die

SCVR
- High efficiency
- Die integration
- Discrete Vout
- Finer domains
- Faster response

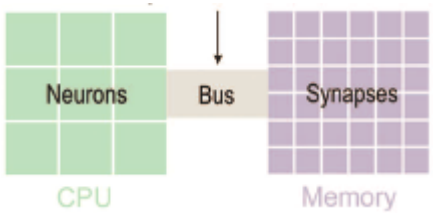


LDO
- Low efficiency
- Die integration
- Narrow Vout range
- Finest domains
- Fastest response

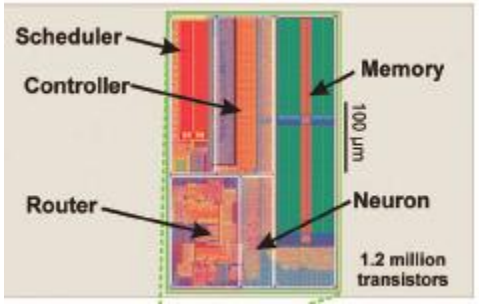
Autonomous & distributed fine-grain power management is essential

Distributed Memory + Compute

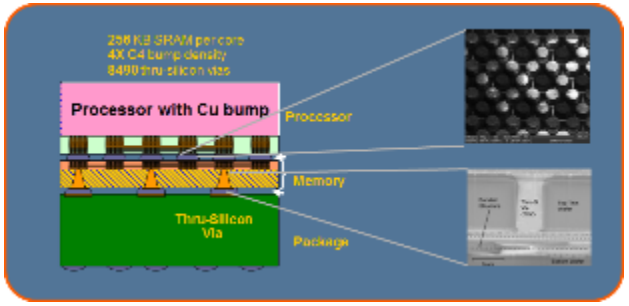
Conventional



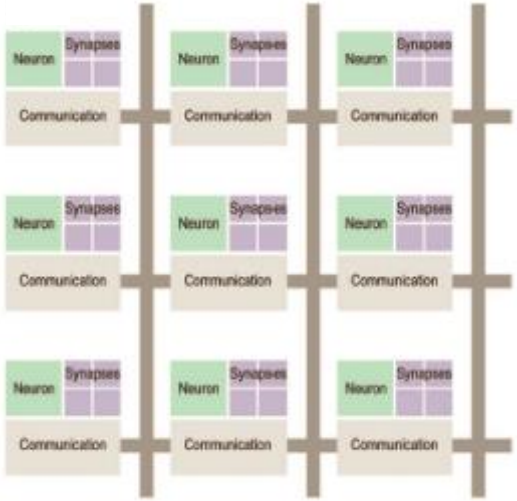
Embedded SRAM Array



3D Integration: SRAM

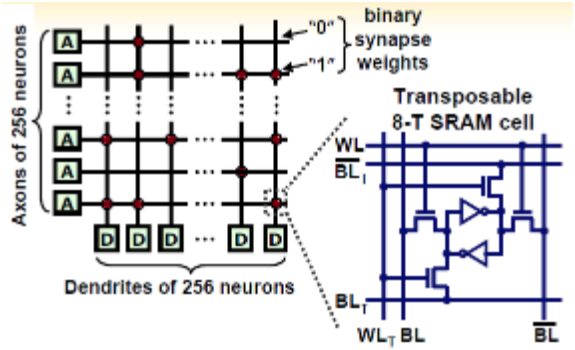


Distributed



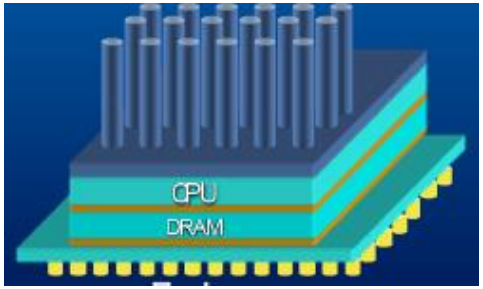
Merolla et al., 2014 Science

Transposable SRAM Cell



Seo et al., 2011 CICC

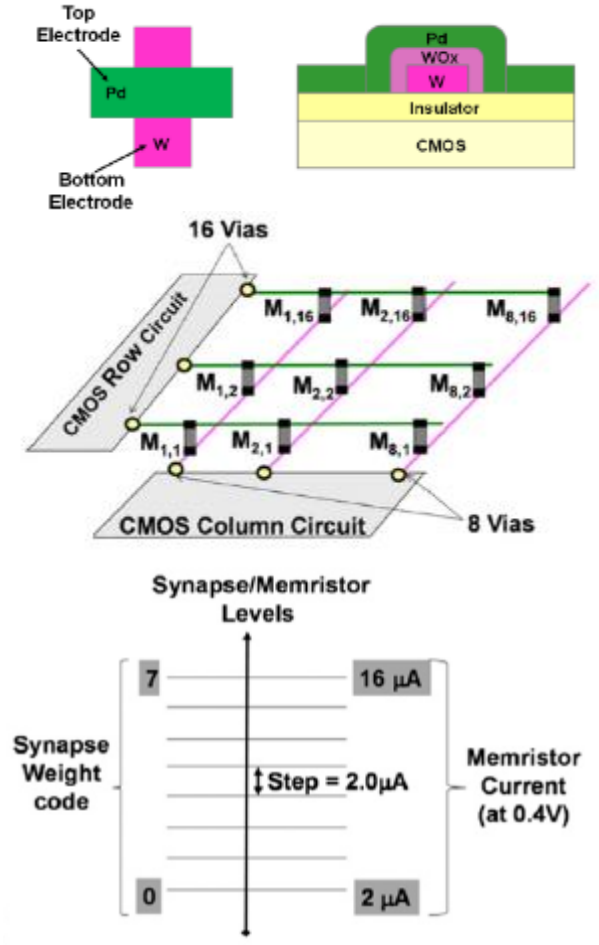
3D Integration: DRAM



Integrated high-density & energy-efficient memory is critical

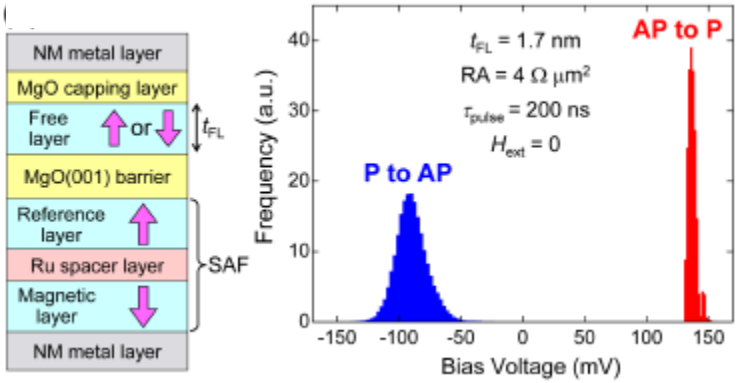
Emerging Technologies: Memory

Integrated ReRAM



Cruz-Albrecht et al., 2013 Nanotechnology

Embedded STT-RAM



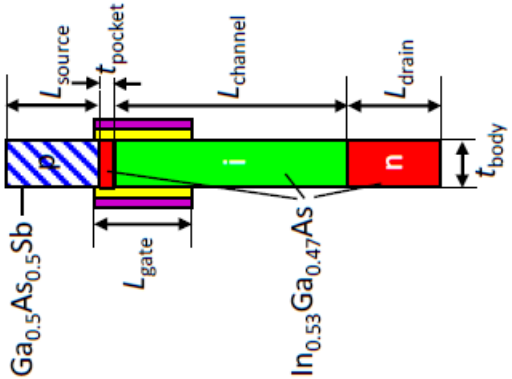
Yuasa et al., 2013 IEDM

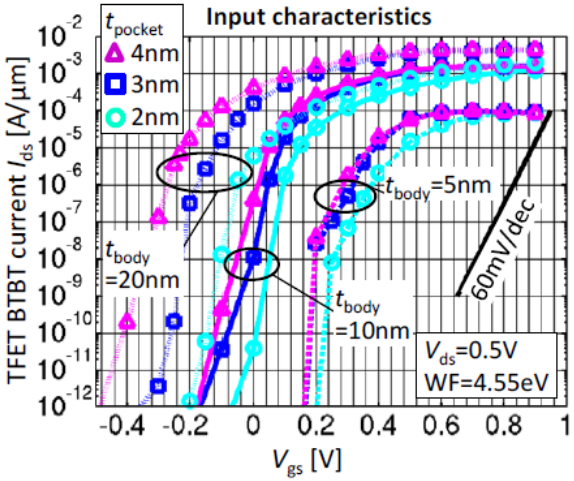
STTRAM vs. SRAM	
Leakage Power	17X lower
Cell Area	2.8X lower
Read Energy	5.6X lower
Write Energy	2X lower

Integrated dense & non-volatile memory for synaptic weight storage

Emerging Technologies: Neurosynapse

Tunnel FET (TFET)

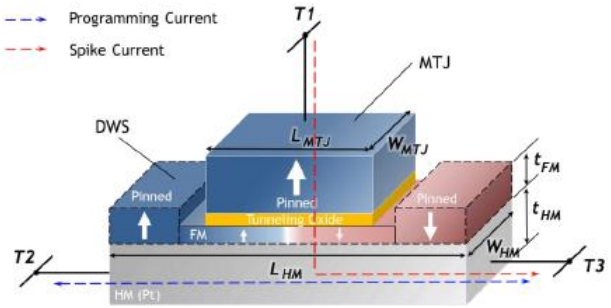




Verhulst et al., 2014 IEDM

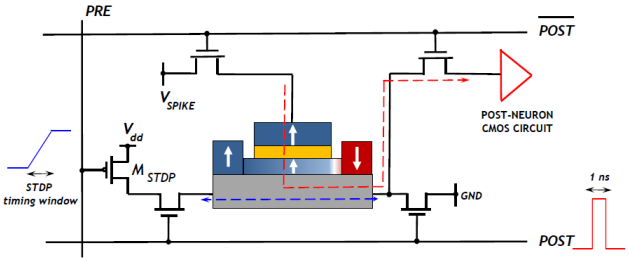
Spintronics

Neel wall based synapse



Spin-orbit torque domain wall motion

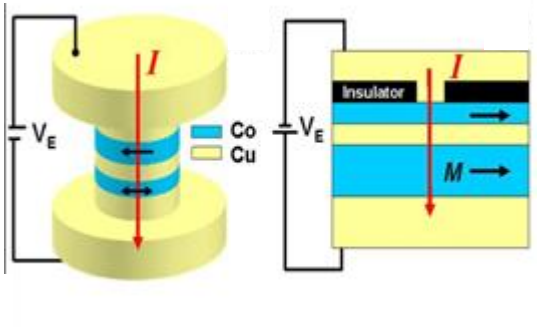
STDP



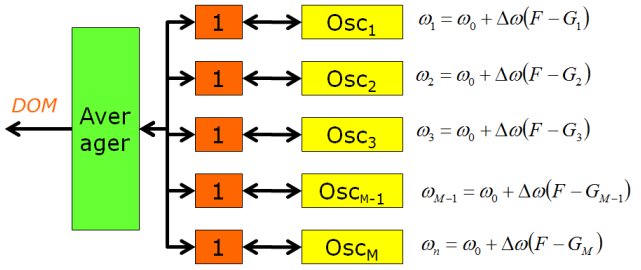
Kaushik Roy, Purdue, 2015

Nano-oscillators

Spin Torque Oscillator (STO)



Pattern matching

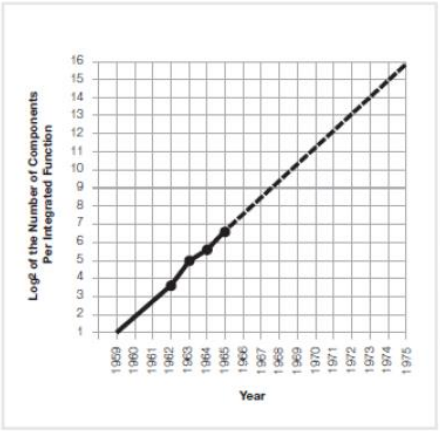


D. Nikonov et al., 2015 JXCDC

TFET, spintronics & nano-oscillators for beyond-CMOS neurosynapse

Beyond CMOS Technology Outlook

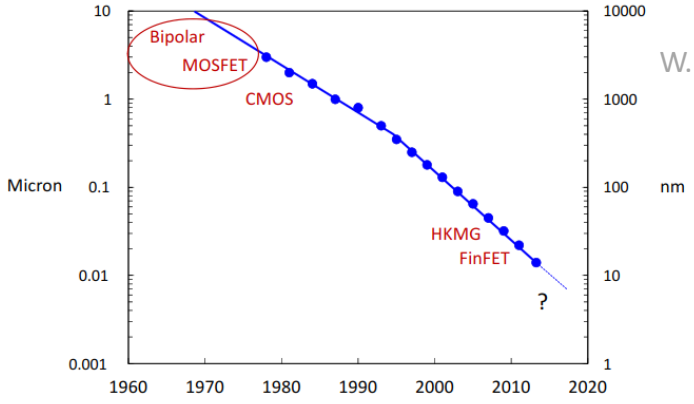
Moore's Law: Economics AND Power



Heat problem

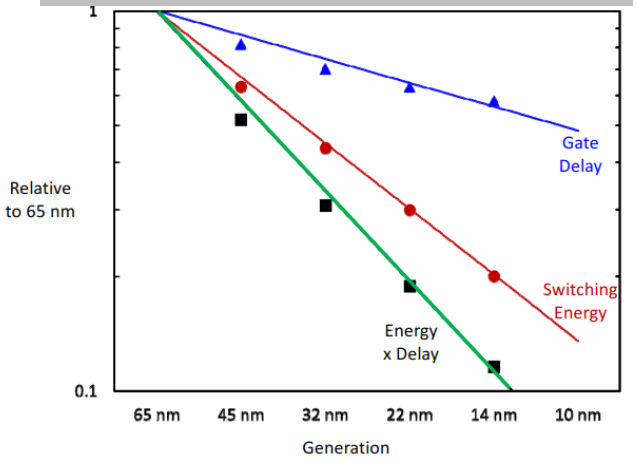
"Will it be possible to remove the heat generated by tens of thousands of components in a single silicon chip?"

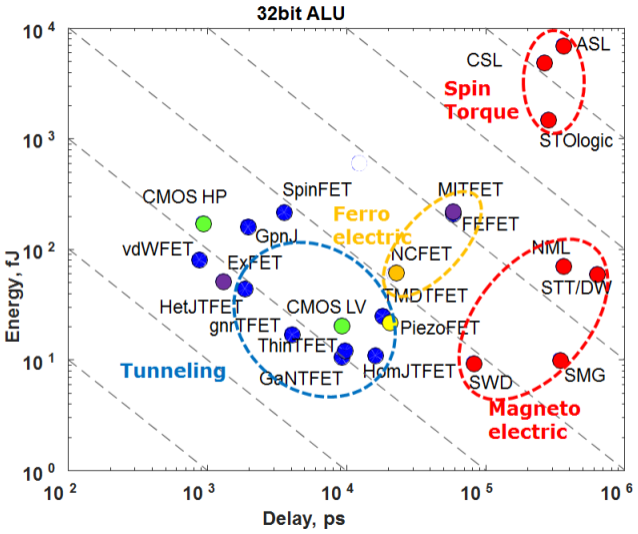
"Cramming more components onto integrated circuits", Electronics, Volume 38, Number 8, April 19, 1965



W. Holt, 2016 ISSCC

Technology Outlook

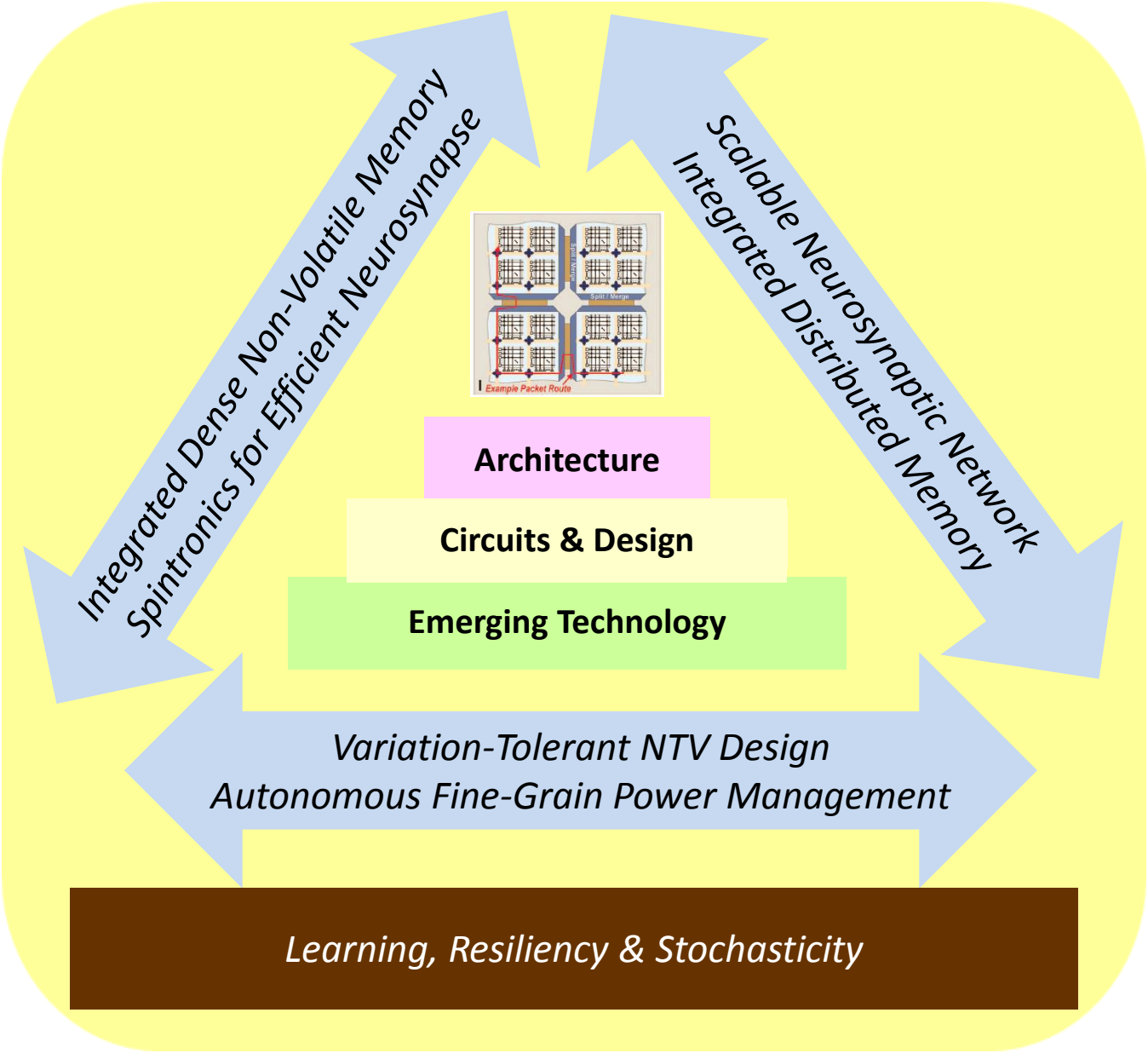




D. Nikonov & I. Young, 2015 JXCDC

Big leaps in energy efficiency trigger technology transitions!

Summary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Spintronics for Efficient Neurosynapse
Scalable Neurosynaptic Network
Integrated Distributed Memory
Example Packet Route
Architecture
Circuits & Design
Emerging Technology
Variation-Tolerant NTV Design
Autonomous Fine-Grain Power Management
Learning, Resiliency & Stochasticity