

Center for Spintronic Materials, Interfaces, and Novel Architectures

Emerging spintronics-based logic technologies

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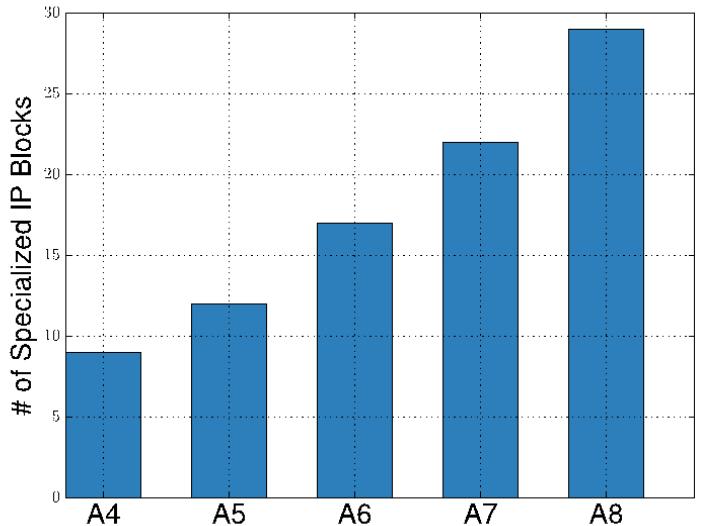


Workshop on the Future of Spintronics (June 5, 2016)

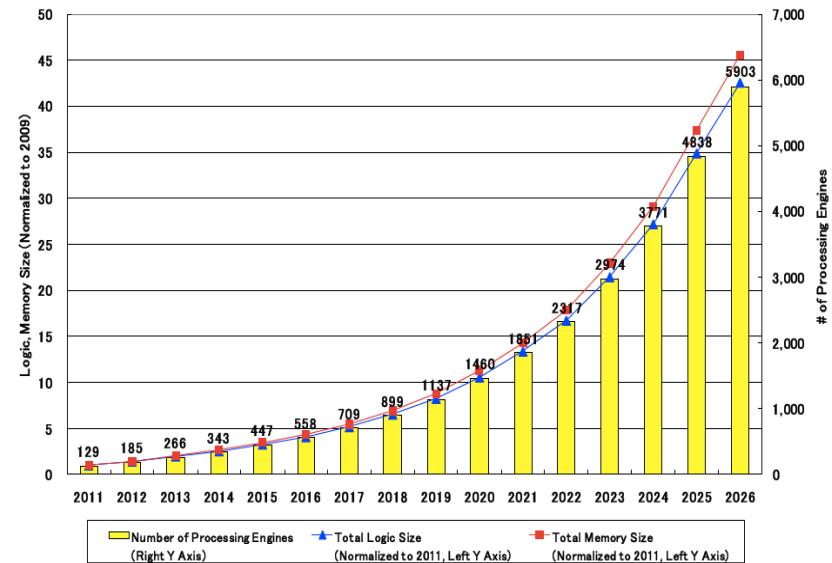


On-chip heterogeneity

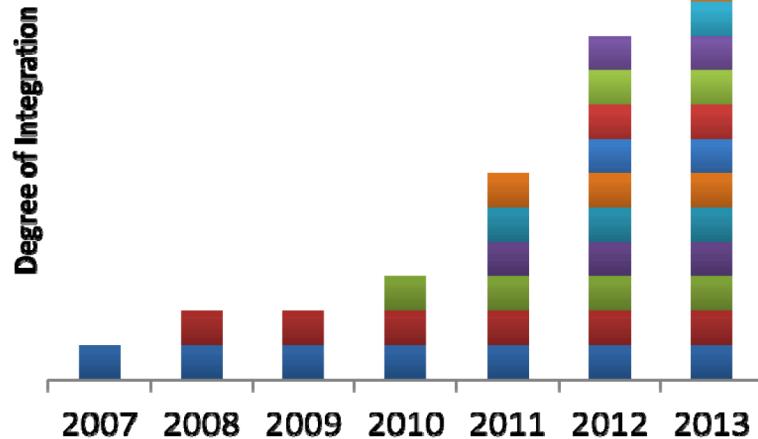
Apple



[<http://vlsiarch.eecs.harvard.edu/accelerators/die-photo-analysis>]



Snapdragon



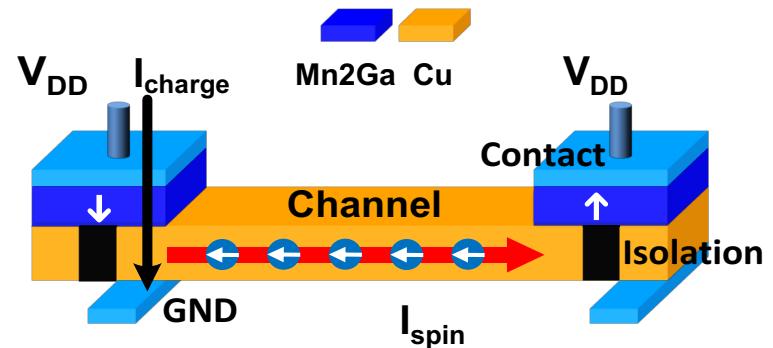
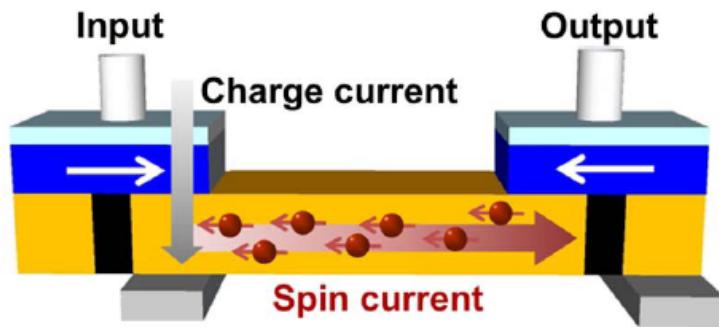
- LPDDR3
- ARMv8 ISA
- LTE
- Integrated wireless
- Integrated BT
- 1080p Video
- W-CDMA
- ARMv7 ISA
- GHz Application processor
- LPDDR2
- GPU
- ARMv6 ISA

[ITRS 2014 whitepaper]

Outline

- Contenders: spintronic logic
- Requirements for spin-based logic
- A new device concept

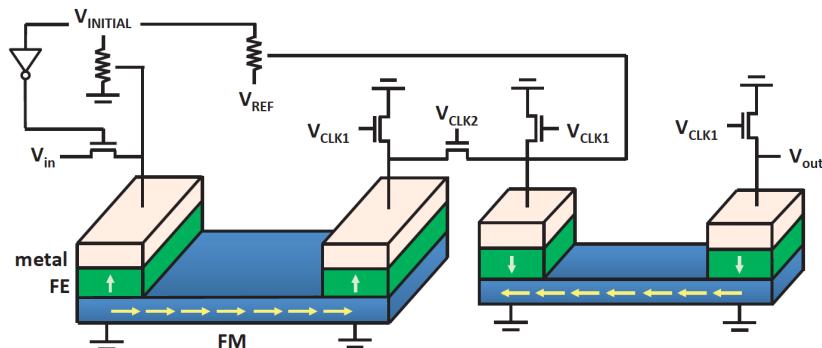
Background: ASL and HEAL



- Input magnet injects spin into channel
- Channel transfers spin to output end
- Output magnet receives spin and stores state
- Heusler-based ASL (HEAL)
 - Heusler alloys: high spin polarization (0.7~1.0), high perpendicular magnetic anisotropy ($H_k > 10000$ Oe), high spin injection efficiency, no tunnel barrier
- Other variations based on Spin-Hall effect

Background: Magnetoelectric (ME) devices

- ME-based device

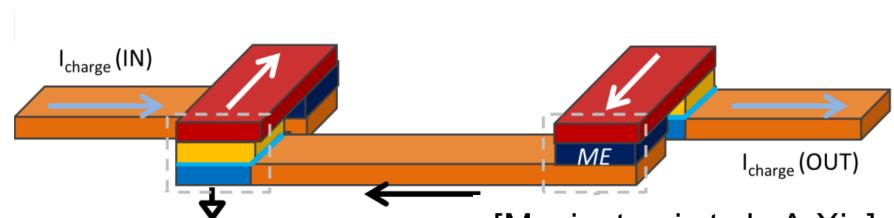


[Chang et al., JxCDC16]

- ME effect used to switch input
- Signal propagation and majority evaluation using domain wall automotion
- Inverse ME effect used to switch output

- MESO

- Charge-mediated device



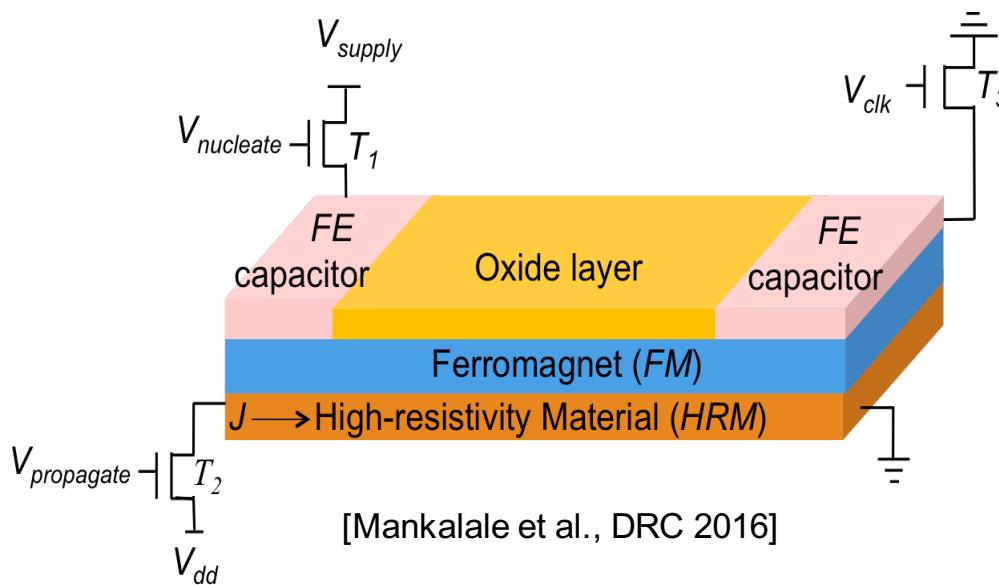
[Manipatruni et al., ArXiv]

- Charge used to switch input magnet using the ME effect
- Spin-orbit coupling (Spin-Hall effect, inverse Rashba-Edelstein effect) creates output charge current

Goals for spin-based logic devices

- High speed
~100ps switching time
- Low energy
~100aJ energy

ME + current-driven domain walls

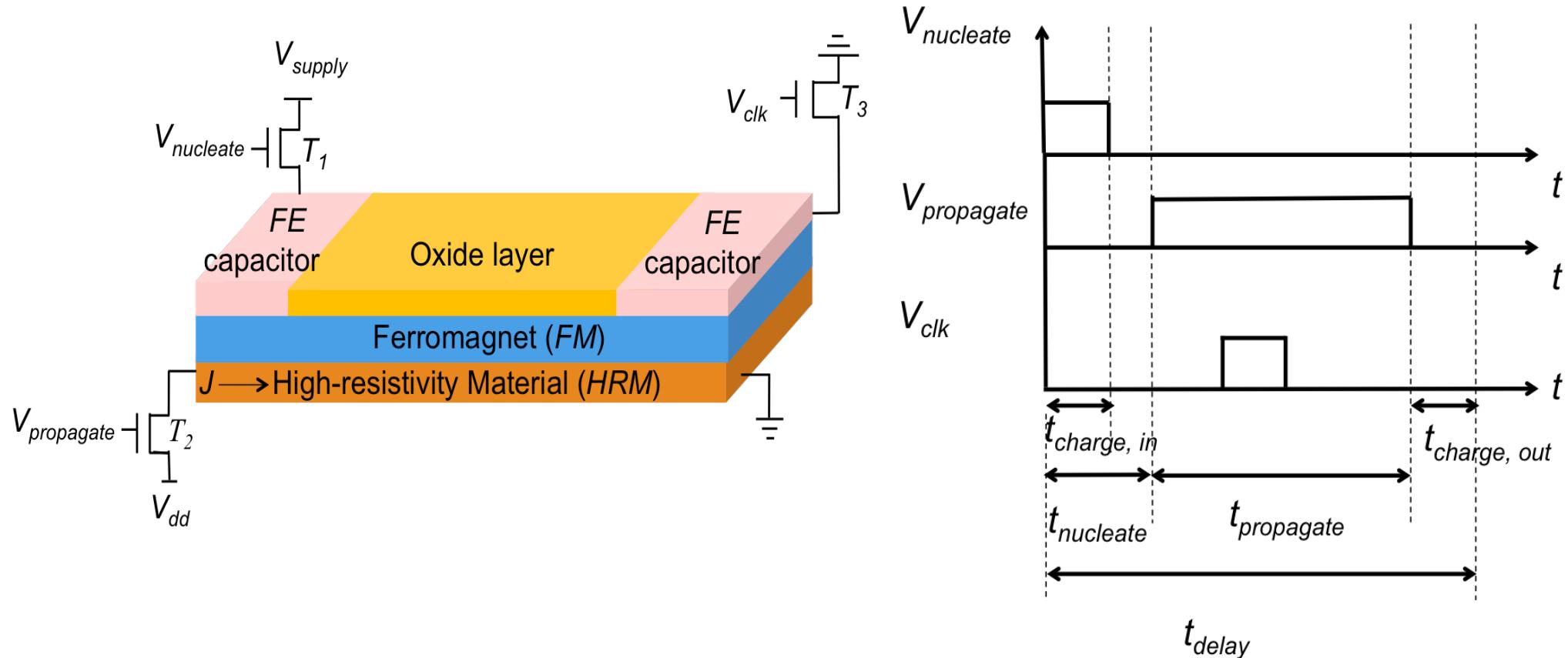


Goal: ~100ps delay, < 100aJ energy

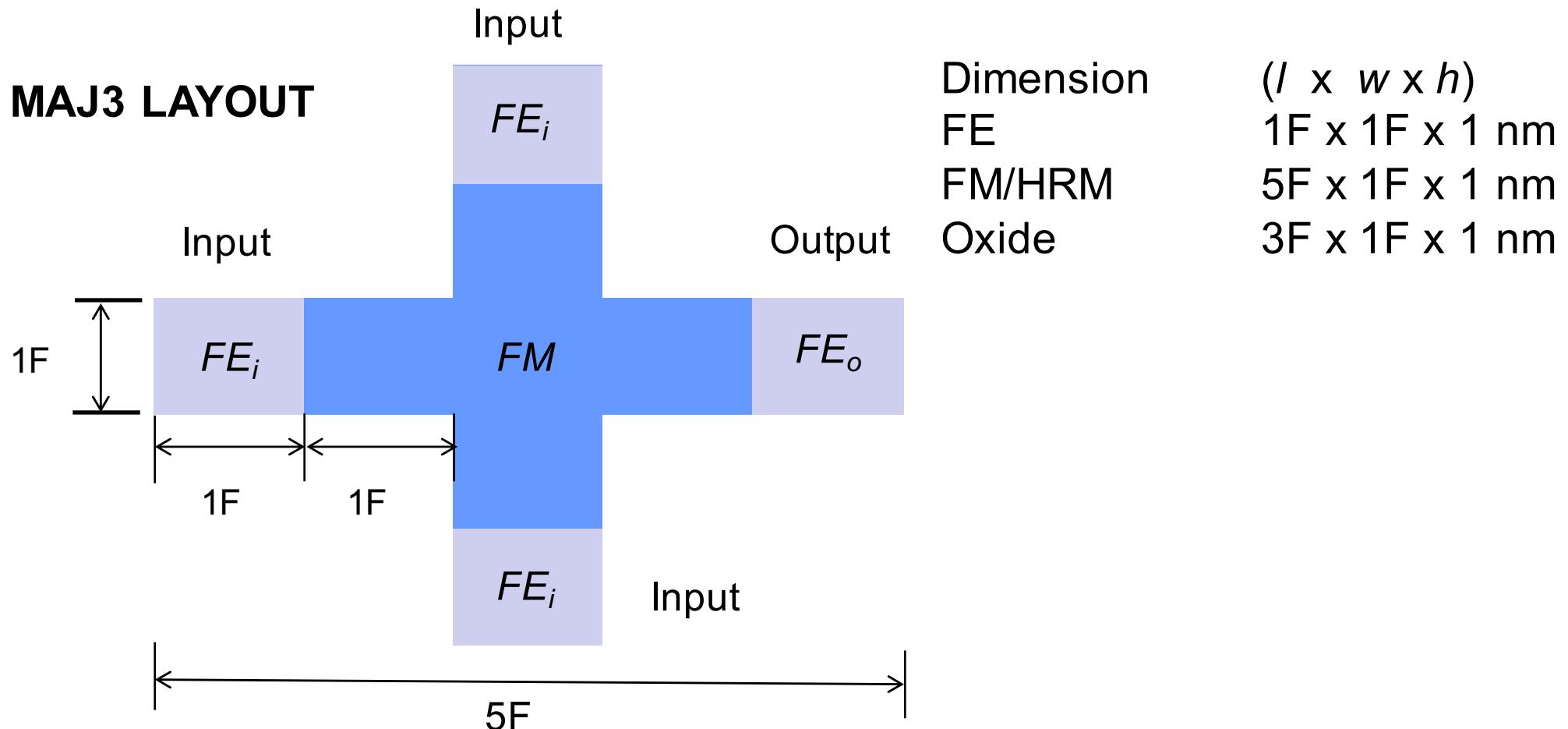
- Domain wall speed bottleneck
 - ME-based device using automotion proposed in [1]
 - Experimentally, automotion $\sim 70\text{m/s}$ [2]
 - **Expend energy, fast propagation**
- Design-space exploration of material parameters
 - **Existing/exploratory material**
 - We propose **CoMET**: **C**omposite-input **M**agneto-**E**lectric **T**echnology with domain wall propagation using spin orbit torque

[1] S.- C. Chang et al., IEEE JxCDC, 2016 [2] J. Chauleau et al., PRB, 2010.

ME Logic with Current–driven DW Motion

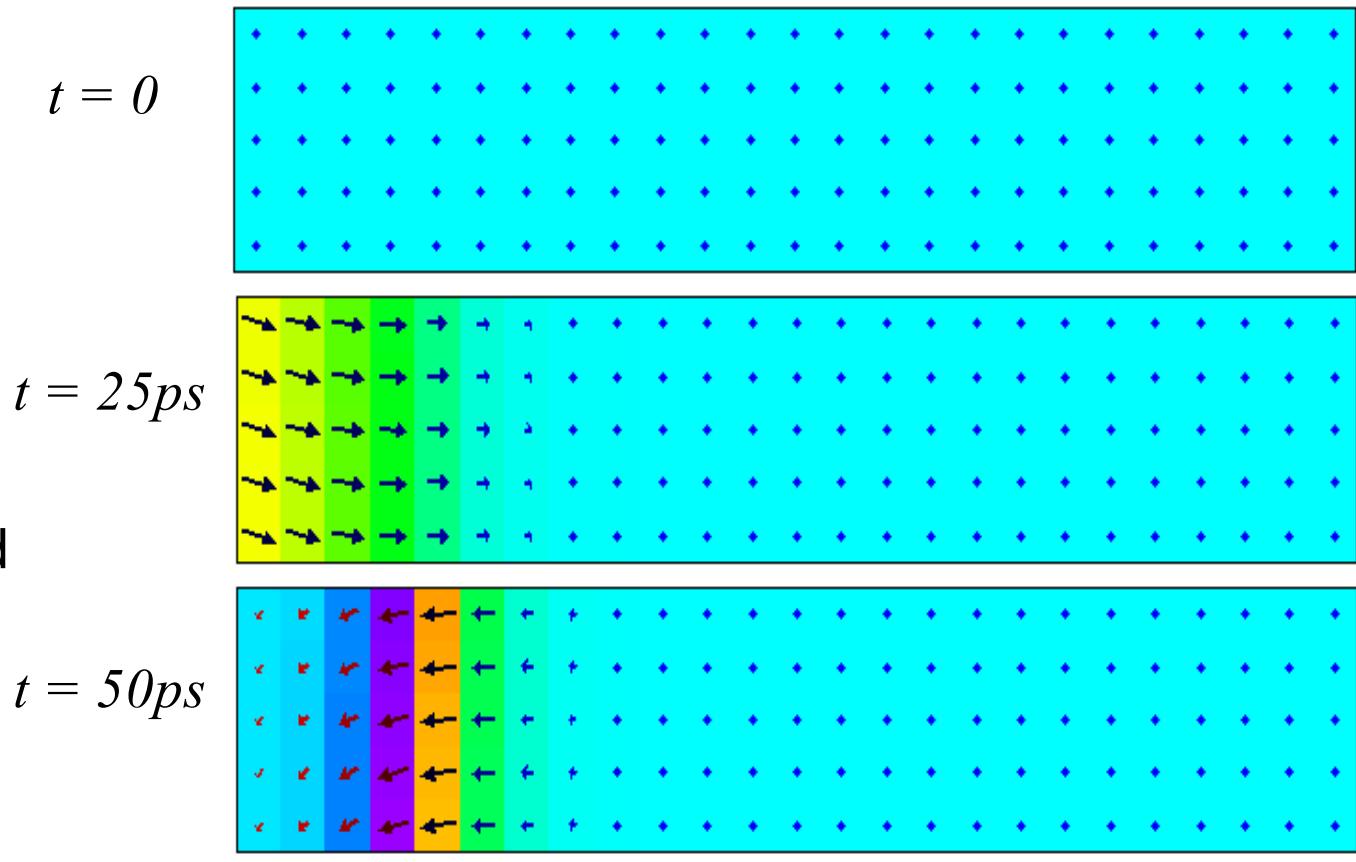
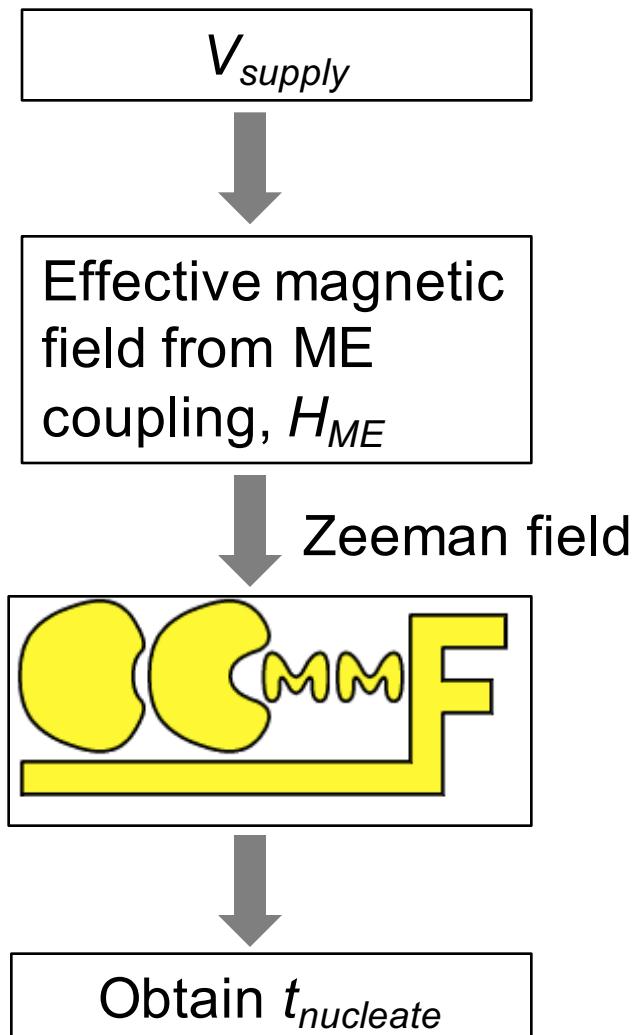


Device Dimensions



Technology nodes considered: 1F = 5nm, 7nm, 10nm

Domain Wall Nucleation



DW nucleation in FM

Current-driven Domain Wall Propagation

$$1 + \alpha^2 \frac{dV}{dt} = -\gamma\Delta \frac{H_K}{2} \sin(2\phi) + (1 + \alpha^2\beta) B_{STT} + \gamma\Delta \frac{\pi}{2} [\alpha H_{SHE} + H_{DMI} \sin(\phi)]$$

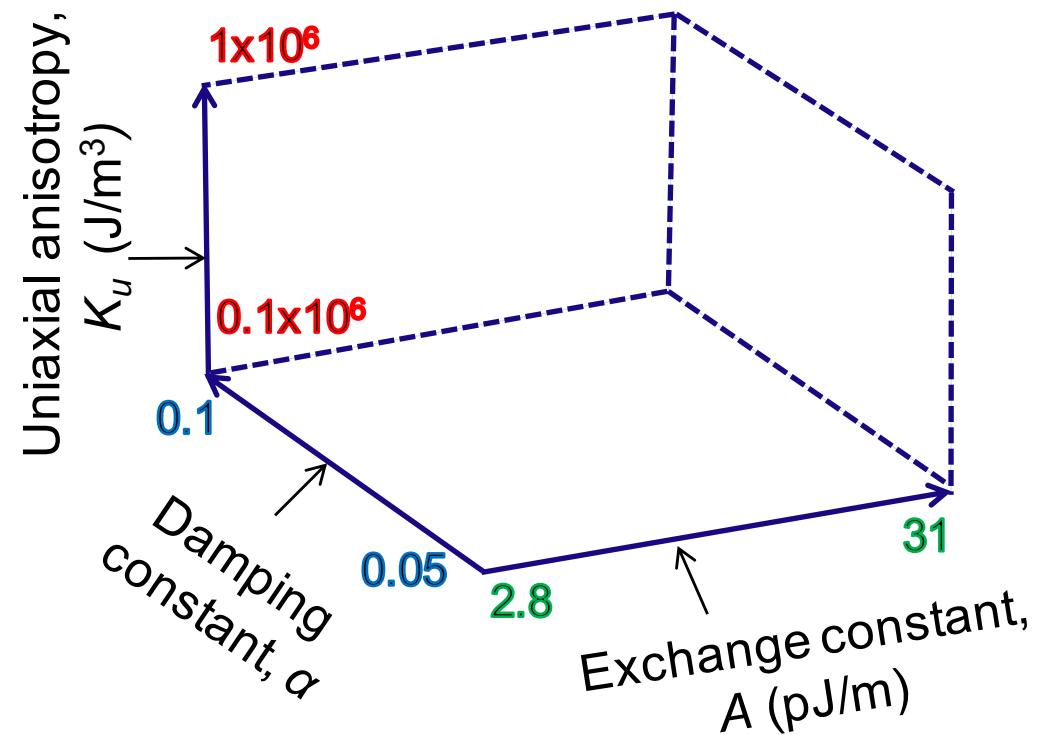
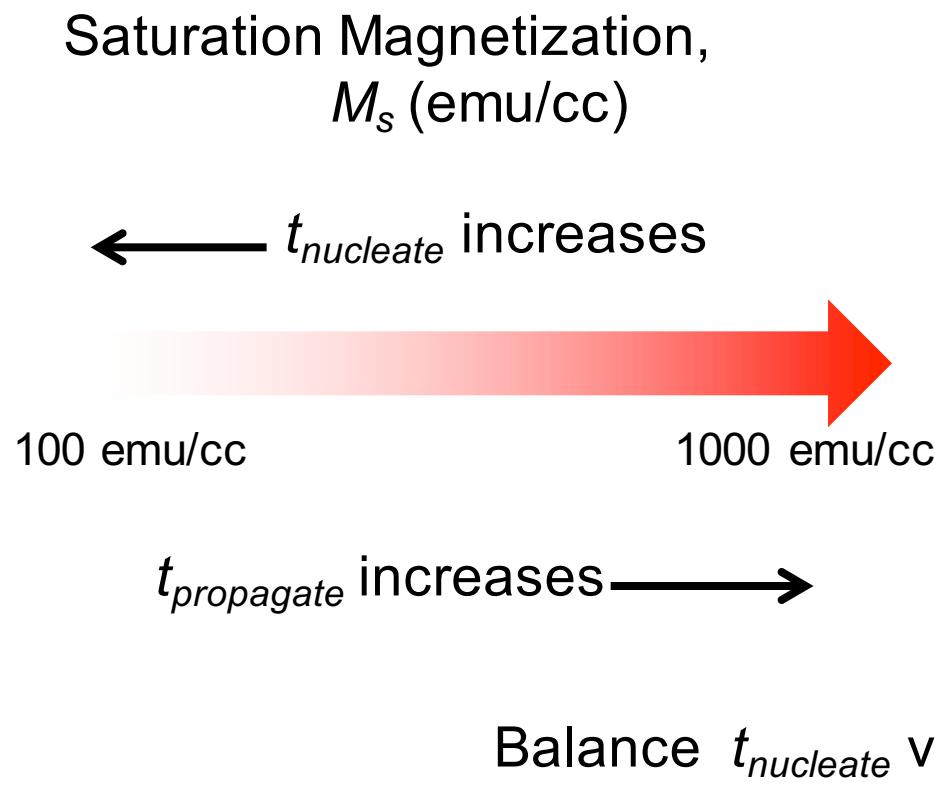
$$1 + \alpha^2 \frac{d\phi}{dt} = -\gamma\alpha \frac{H_K}{2} \sin(2\phi) + \frac{(\beta-\alpha)}{\Delta} B_{STT} + \gamma \frac{\pi}{2} [H_{SHE} \cos(\phi) + \alpha H_{DMI} \sin(\phi)]$$

where $H_{SHE} = \frac{\hbar \theta_{SHE} J}{2\mu_0 e M_s h_{FM}}$, $H_{DMI} = \frac{D}{\mu_0 M_s \Delta}$, $B_{STT} = \frac{\mu_B P_{FM} J}{e M_s}$, $\Delta = \sqrt{\frac{A/K_u}{1 + \frac{\mu_0 M_s^2}{K_u} \left[\frac{h_{FM}}{h_{FM} + \Delta} - \frac{h_{FM}}{h_{FM} + w_{FM}} \right] \sin^2(\phi)}}$

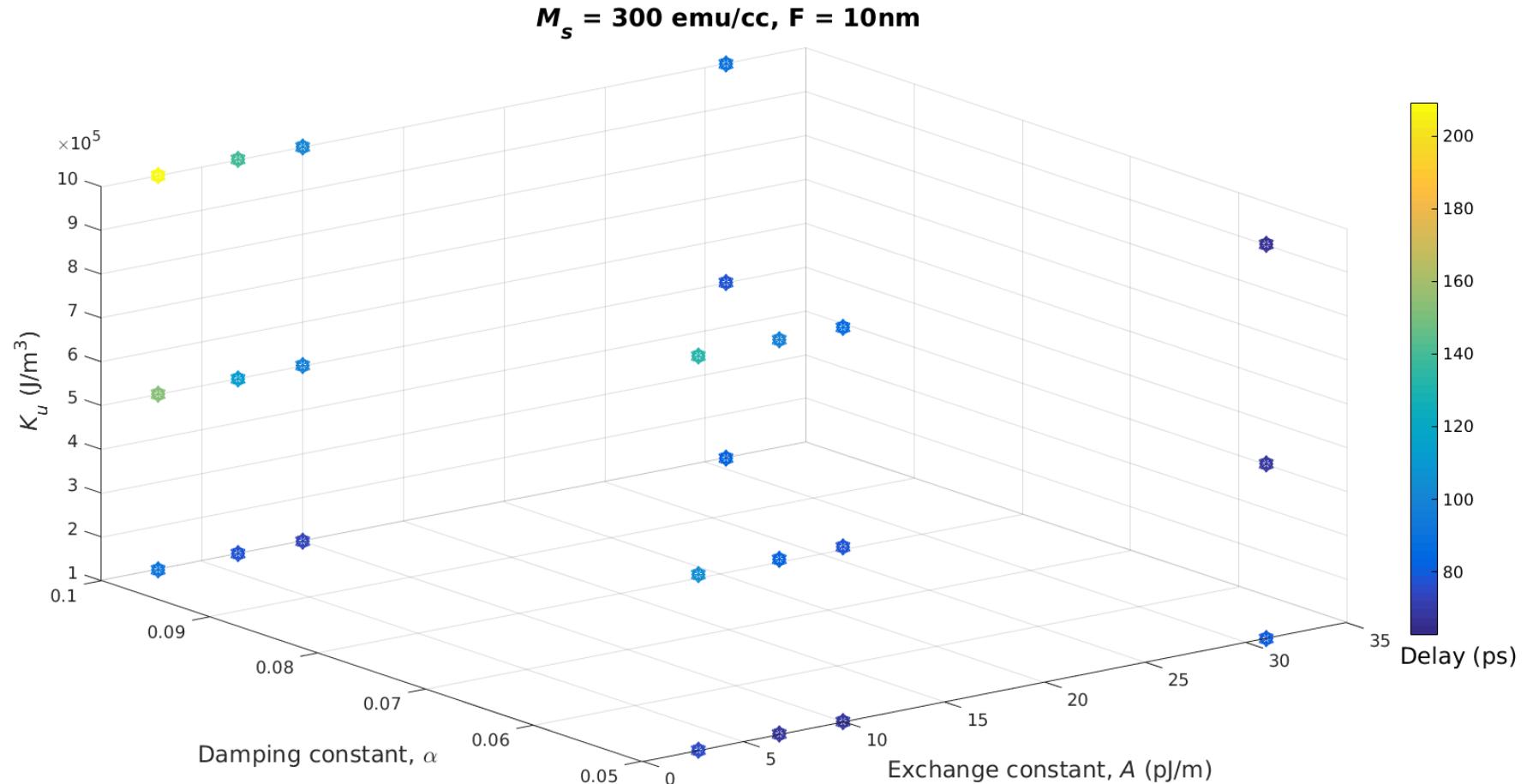
- Impact of scaled geometries considered for calculation of V , velocity of DW and ϕ , phase of the DW.
- Current density, $J = 9 \times 10^{10} \text{ A/m}^2$ (below electromigration limit).
- Walker breakdown field also accounted for.

Design Space Exploration

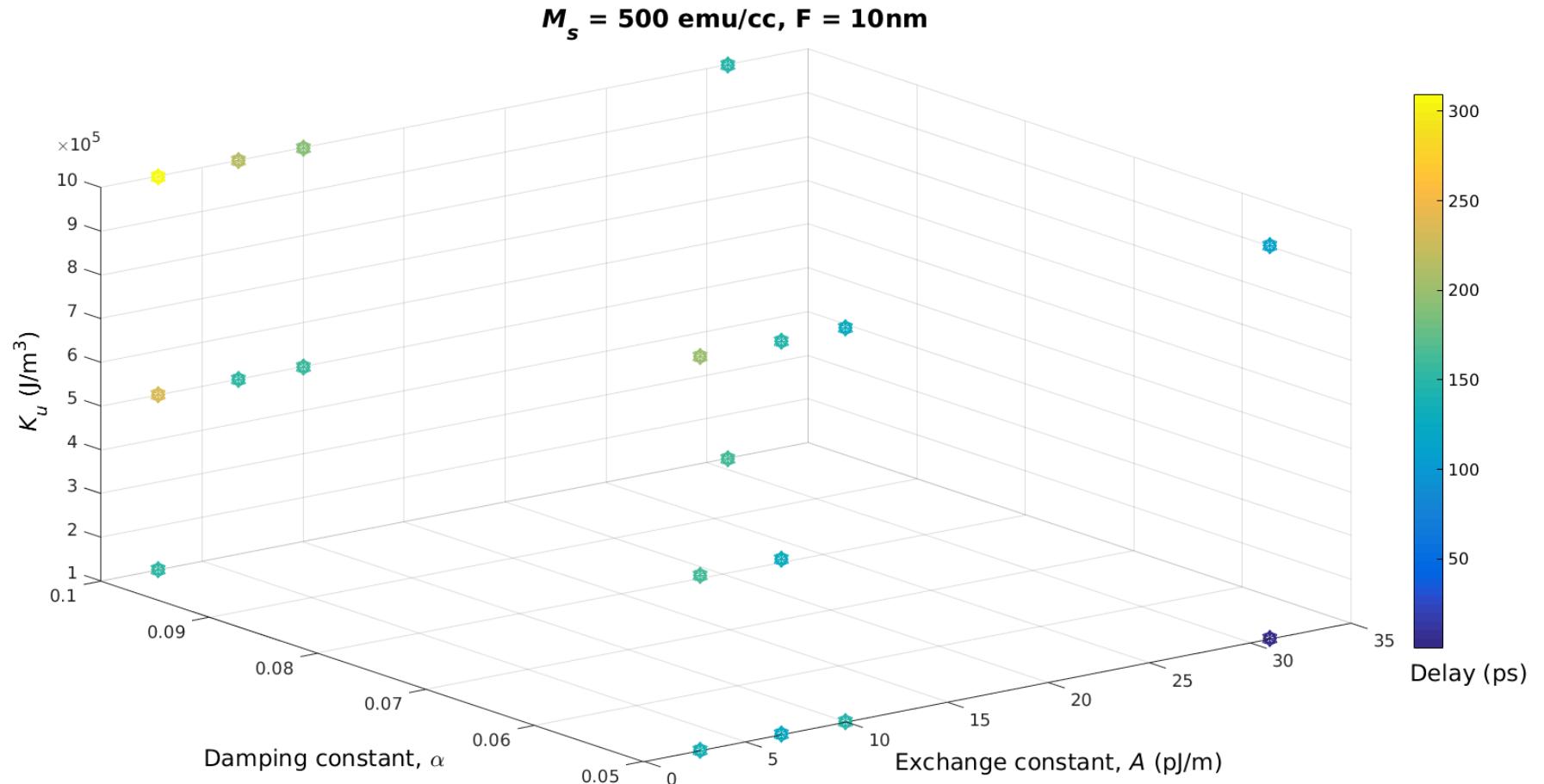
- Design space large – Focus only on *FM* material parameters
- Range of parameters chosen to cover both existing and exploratory materials



Design Space Exploration - DW Propagation



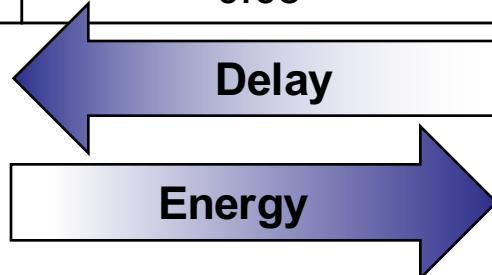
Design Space Exploration - DW Propagation



Results

Set Parameters	Set 1	Set 2	Set 3
Exchange constant , A (pJ/m)	10	2.8	6.8
Saturation Magnetization, M_s (emu/cc)	500	300	300
Supply voltage, V_{supply} (V)	0.93	1.50	2.12
Spin Polarization	0.5		
Spin Hall Angle	0.5		
Uniaxial anisotropy, K_u (J/m ³)	10⁶		
Damping constant, α	0.05		

Energy-delay tradeoff
between parameter sets.



t_{delay}

Technology node (1F)	Set 1 (ps)	Set 2 (ps)	Set 3 (ps)
5nm	128	125	117
7nm	156	149	124
10nm	198	184	155

DW Velocity (m/s)	362	420	540

Energy

Technology node (1F)	Set 1 (aJ)	Set 2 (aJ)	Set 3 (aJ)
5nm	67.4	130.6	212.0
7nm	108.6	209.0	417.6
10nm	173.4	375.6	701.0

Mapping to Materials

Set Parameters	Set 1	Set 2	Set 3
Exchange constant , A (pJ/m)	10	2.8	6.8
Saturation Magnetization, M_s (emu/cc)	500	300	300
Spin Polarization	0.5		
Uniaxial anisotropy, K_u (J/m ³)		10^6	
Damping constant, α	0.05		

FM

Mn-Ga based
Heusler alloy

FE Capacitor

BFO

HRM

β -Ta, Pt, β -W

Sneak Peek of CoMET

(currently being validated)

- Based on the use of a composite input structure
 - Similar speeds
 - Much lower Vdd
 - 0.93 – 2.12V → < 0.3V
 - Energy ~60aJ

Supply voltage (V)	Set 1	Set 2	Set 3
5nm	0.75	0.27	0.58
7nm	0.58	0.14	0.27
10nm	0.27	0.14	0.14

Technology node (1F)	Set 1 (ps)	Set 2 (ps)	Set 3 (ps)
5nm	137	123	105
7nm	175	156	131
10nm	233	206	170
DW Velocity (m/s)	362	420	540

Energy			
Technology node (1F)	Set 1 (aJ)	Set 2 (aJ)	Set 3 (aJ)
5nm	106.2	56.4	83.2
7nm	110.6	52.6	62.4
10nm	78.6	57.0	57.0

Summary

- New device for logic applications: ~100ps, ~100aJ per device
- Currently being extended to build larger circuits
- Possible applications
 - Logic circuits
 - In-/Near-memory processing structures
 - IoT elements
- Acknowledgments
 - Angeline Smith, Mahendra DC, Mahdi Jamali