Center for Spintronic Materials, Interfaces, and Novel Architectures

Exploiting Non-Volatility in Spin-Based Information Processing

X. Sharon Hu, University of Notre Dame

Students: Robert Perricone, Ibrahim Ahmed
Collaborators: Michael Niemier, Chris Kim,
Anand Ragunathan, Sachin Sapatnekar Jian-Ping Wang

Theme 5
Cross Theme 4

This work is sponsored in part by C-SPIN, a funded center of STARnet, a Semiconductor Research Corporation (SRC) program sponsored by MARCO and DARPA.

C-SPIN

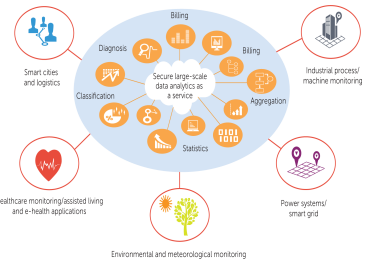
STARnet

From Applications to Devices

Applications/ Systems

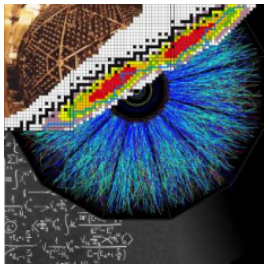
???

Devices/ Material



www.computer.org

Data/image analytics



www.nersc.gov

Scientific Computing

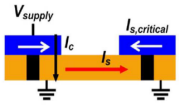
www.carandriver.com

Control & Decision making

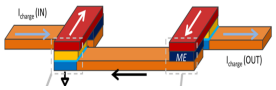
Edge computing

Architectures /Circuits

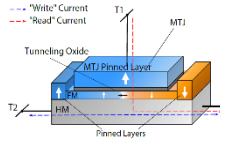
Focus of Theme 5



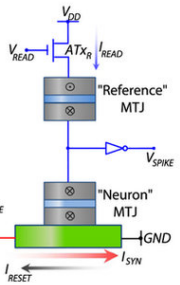
All-Spin Logic

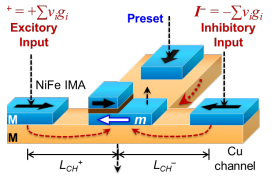


MESO device

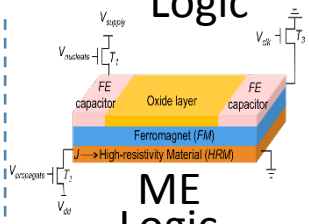


DW device

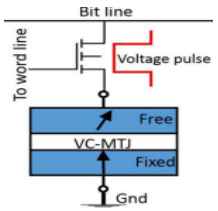




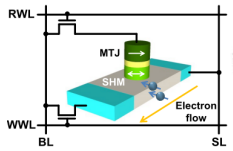
NLSV device



ME Logic



MeRAM



SHE MRAM

MTJ spiking Neuron

• • •

C-SPIN

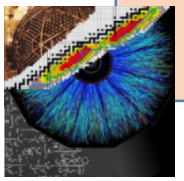
STARnet

Exploiting Unique Properties of Spintronic Devices

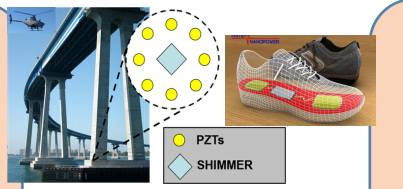
Applications/ Systems

???

Devices/ Material



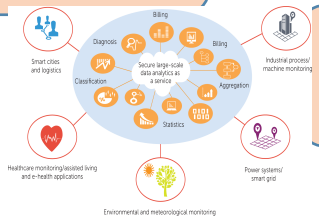
Energy proportional computing



Edge computing powered by harvested energy

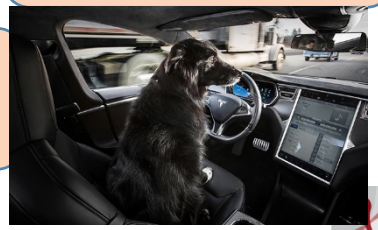
Non-volatility
High energy efficiency
Diverse functionality

Near/In-memory processing



Neuromorphic computing

Stochastic computing



From Applications to Devices: Example

www.campussafetymagzine.com

- Control and decision making
- Image and data analytics
- Sensing and communication
- Low power, real-time, …

Applications/ Systems

???

Devices/ Material

Energy sources

Sensors

Actuators

Comm

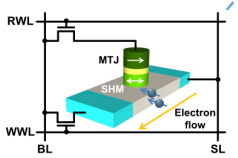
Compute engine

X-MRAM LL cache

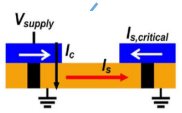
Multi-core CPU

Neural network/ Stochastic computing

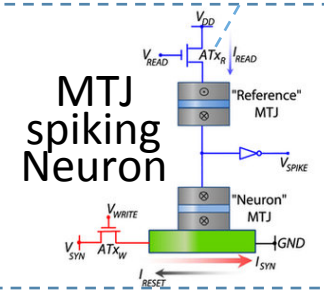
Logic-in-memory module



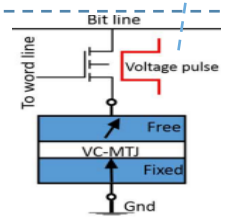
SHE MRAM



All-Spin Logic



MTJ spiking Neuron



MeRAM

Circuit and Architecture Example

Applications/ Systems

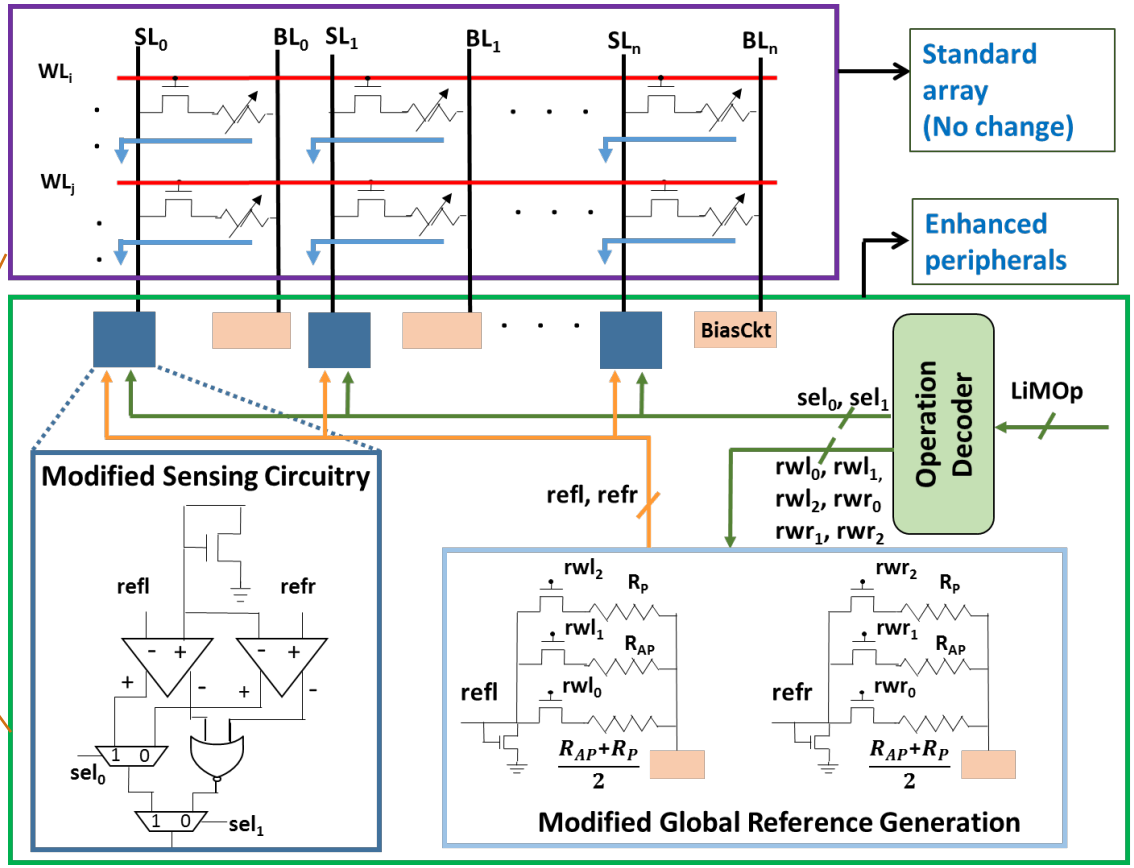
Architecture/ Circuit

Devices/ Material

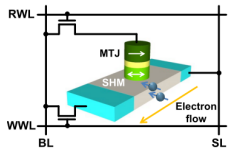
Pattern recognition/ image analysis

www.123rf.com

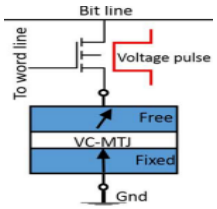
Logic-in-memory module



LiM work by Ragunathan



SHE MRAM

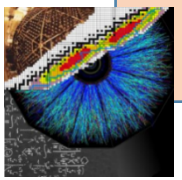


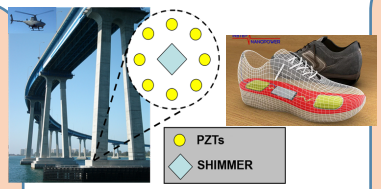
MeRAM

- Modifications only to memory's peripheral circuits

Exploiting Unique Properties of Spintronic Devices

Energy proportional computing

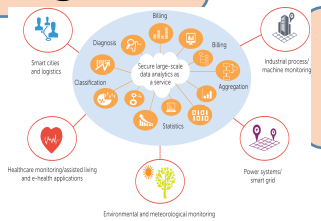




Edge computing powered by harvested energy

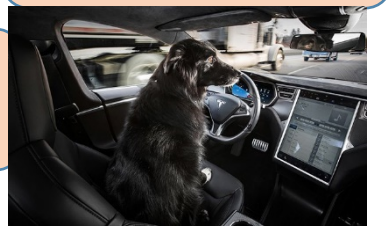
Non-volatility
High energy efficiency
Diverse functionality

Near/In-memory processing



Neuromorphic computing

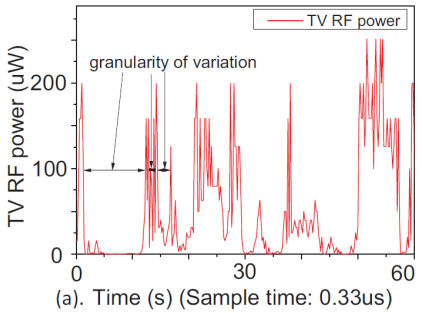
Stochastic computing



Systems Powered by Harvest Energy

- Many edge computing systems are powered by harvested energy

- Unstable power supply
  - Off time varies from cycle-to-cycle
  - Length outage depends on source
- Frequent backup/ recovery
  - Energy inefficiency
  - Slow progress



- NV components allows faster progress toward end result

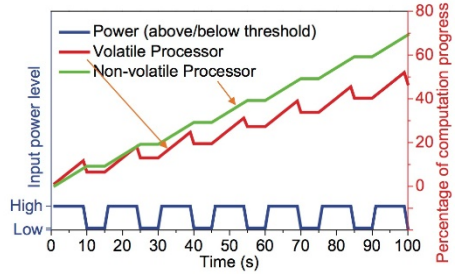


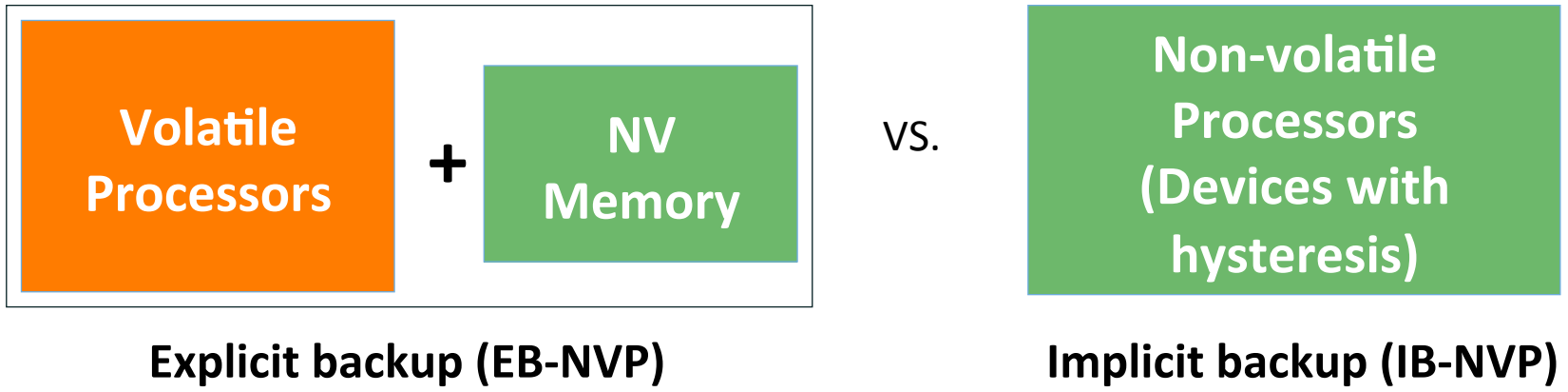
Fig. 4. VP vs. NVP processing progress comparison

Non-volatility of spintronic devices can be ideal alternatives

Power profile figure from: Ma, K., et al. "Architecture exploration for ambient energy harvesting nonvolatile processors." *IEEE Int'l Symposium on High Performance Computer Architecture (HPCA)*. IEEE, 2015.

Non-Volatile Processors (1)

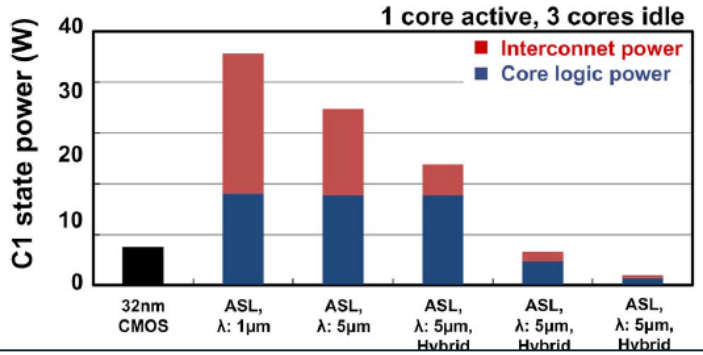
- Two basic designs



Explicit backup (EB-NVP) **Implicit backup (IB-NVP)**

- EB-NVP
  - NV memory for retaining data during power outage
  - C-SPIN memory devices (SHE-RAM, AFM-RAM, ME-RAM)
  - Write time/energy, read time/energy, retention time
- IB-NVP
  - NV logic devices themselves for retaining data during power outage
  - C-SPIN computing devices (ASL, MESO, SWD, etc.)
  - Processing energy, delay, retention time

Non-Volatile Processors (2)

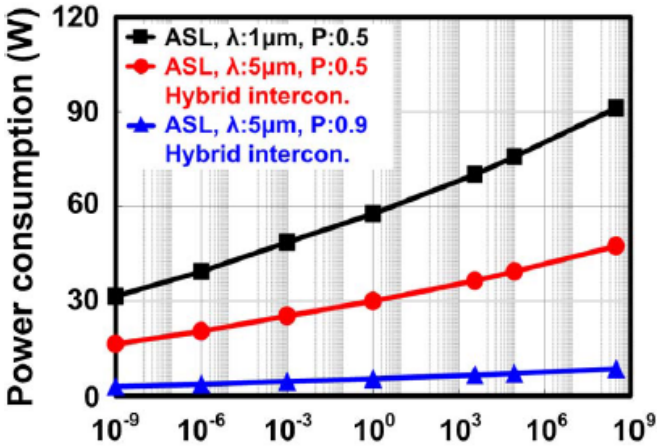


Energy may be less competitive for general purpose computing

NV processor with hybrid backup

"interim" Non-volatile Processors + **NV Memory**

Spin devices (s.t. ASL, MEL) are good candidates

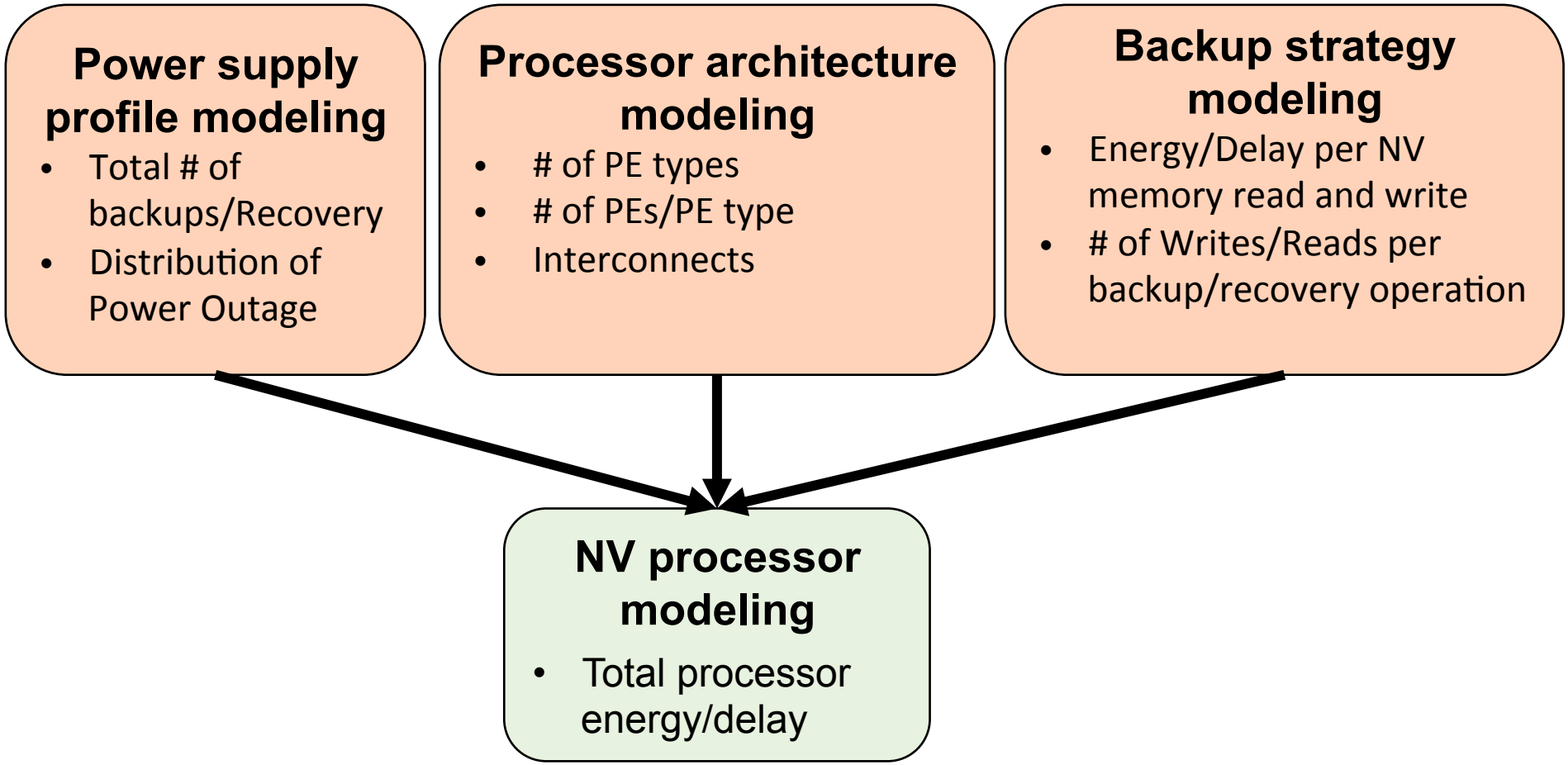


Trade off retention time vs. power

- Shorter retention time for NV processor to save energy
- NV memory recovery only needed when outage is long
- Use design space exploration to optimize

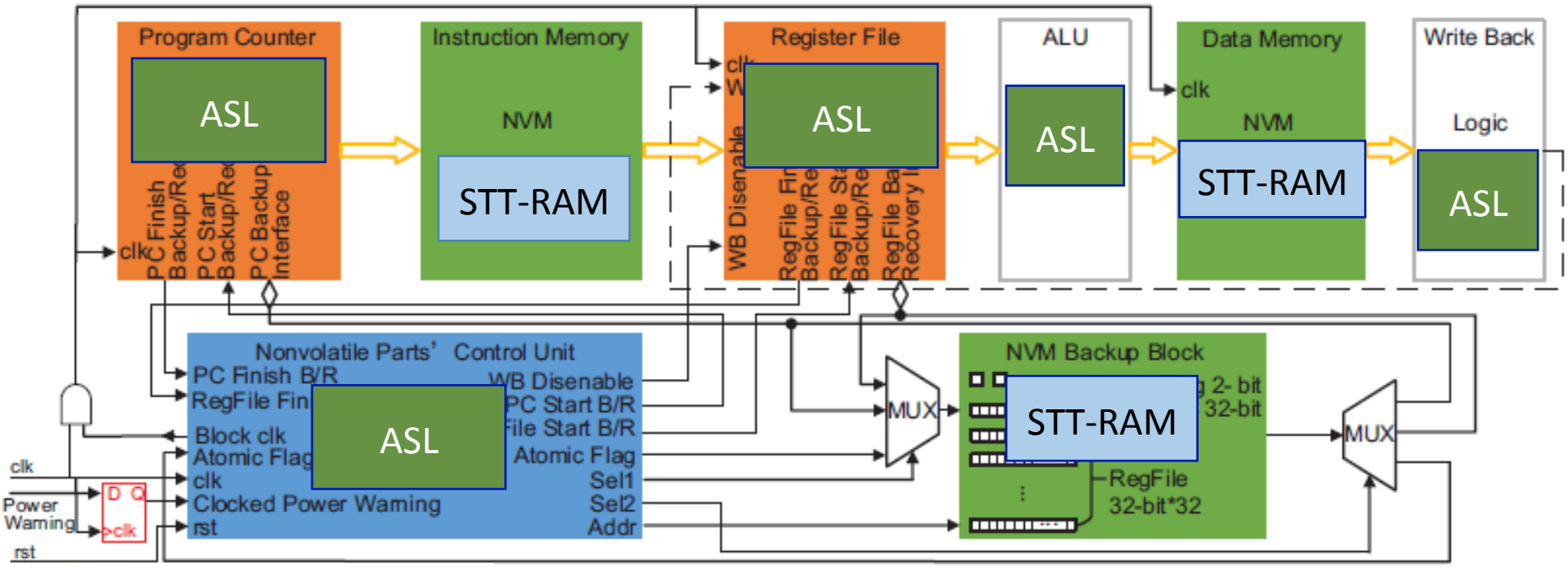
Figures taken from: Kim, J, et al. "Spin-based computing: device concepts, current status, and a case study on a high-performance microprocessor." *Proceedings of IEEE,* 2015..

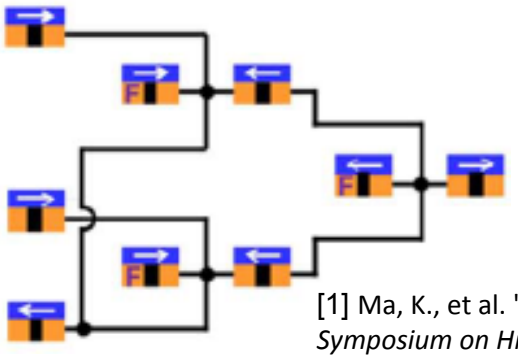
Framework for Benchmarking Non-Volatile Processors

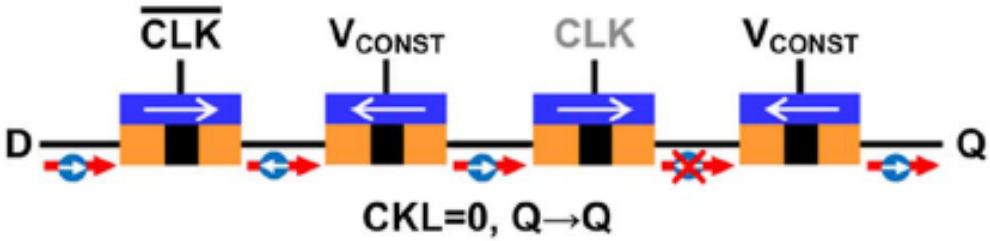


Case Study: 32-Bit MIPS Processor

- 32-bit non-pipelined MIPS processor [1]







[1] Ma, K., et al. "Architecture exploration for ambient energy harvesting nonvolatile processors." *IEEE Int'l Symposium on High Performance Computer Architecture (HPCA)*. IEEE, 2015.

[2] Kim, J, et al. "Spin-based computing: device concepts, current status, and a case study on a high-performance microprocessor." *Proceedings of IEEE,* 2015.

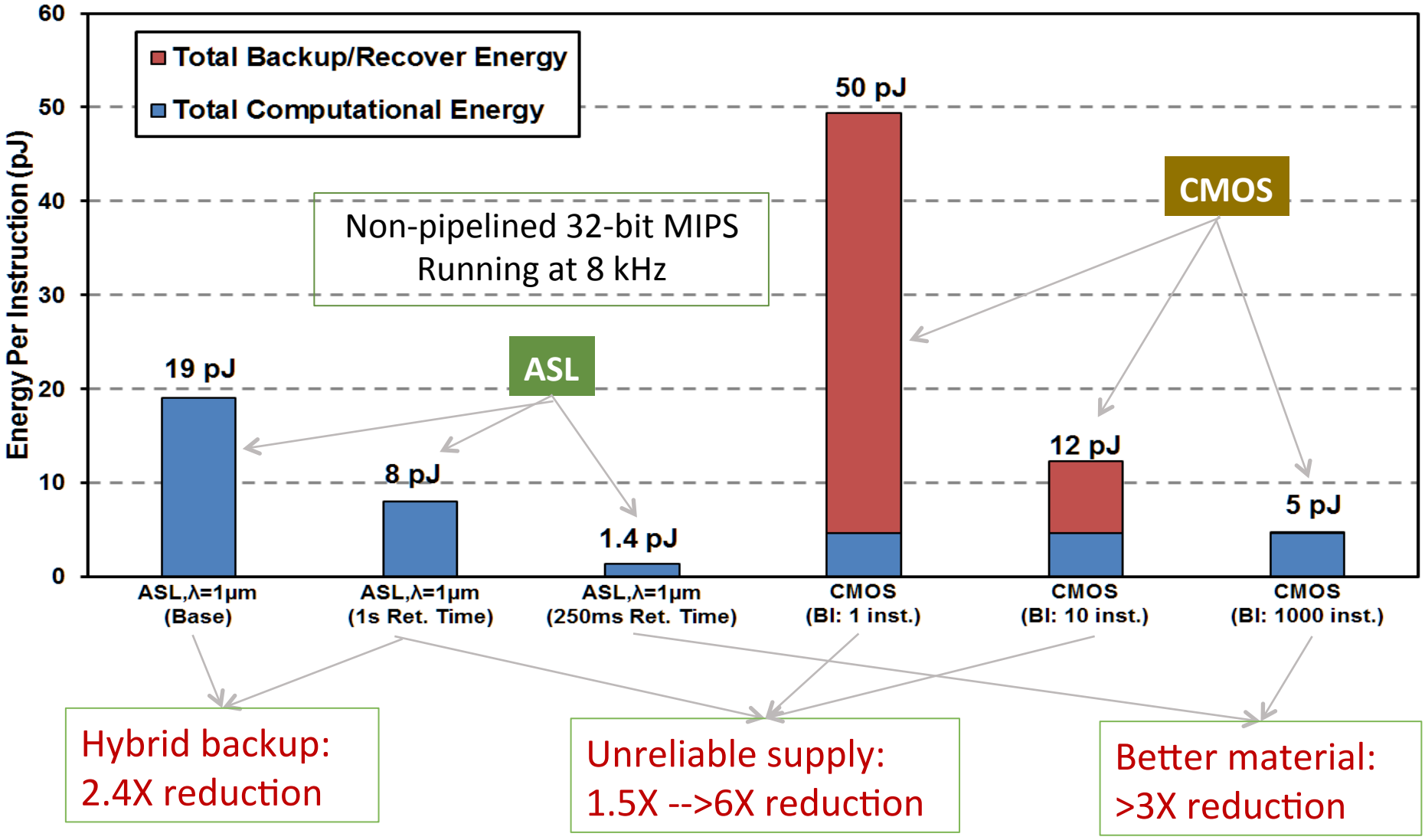
Case Study: ASL as Drop-In Replacement

- CMOS processor data derived from [1]
  - Original data in [1] based on 45nm technology
  - Used BCB model to scale down the processor to 15nm technology
  - Both transistors and STT-RAM are scaled
- ASL processor data derived from [2]
  - Number of ASL devices (for RF, PC, ALU, Control, etc.): 3500 (50% of total number of transistors)
  - IC Buffers: 0 (based on probability distribution function in [2])
  - Different diffusion lengths and materials are considered
  - $E_{total} = N_L(E_L) + N_{IC}(E_{IC})$
    - N_L and N_{IC} are # of logic and IC buffers, resp.
    - E_L and E_{IC} are the switching energy per device

[1] Ma, K., et al. "Architecture exploration for ambient energy harvesting nonvolatile processors." *IEEE Int'l Symposium on High Performance Computer Architecture (HPCA)*. IEEE, 2015.

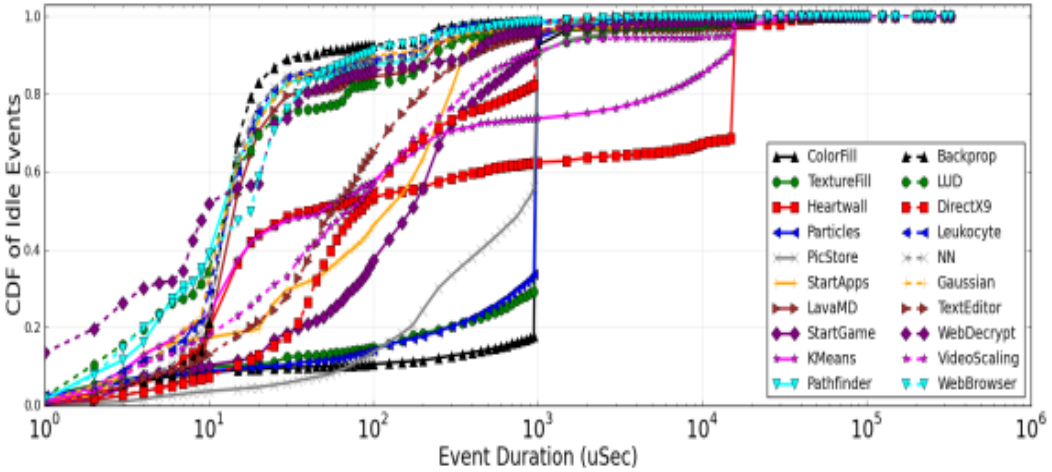
[2] Kim, J, et al. "Spin-based computing: device concepts, current status, and a case study on a high-performance microprocessor." *Proceedings of IEEE,* 2015.

Comparing ASL with CMOS NVP

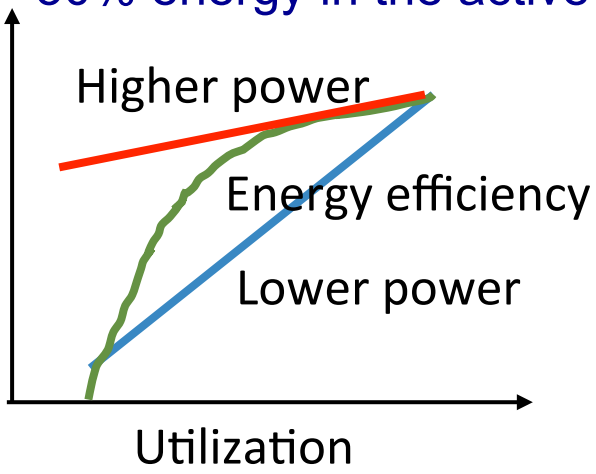


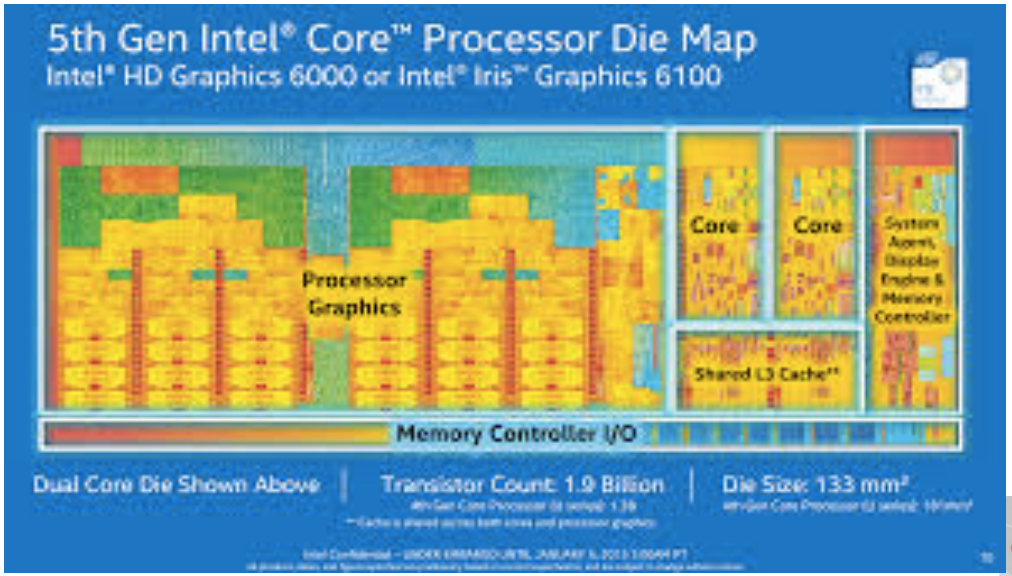
NV in Energy Proportional Computing

- Idle power in heterogeneous multi-core systems
  - Can be quite significant
  - Application dependent
- Aim to achieve energy proportional computing
- Our preliminary results show an Intel i5 processor running BFS only spends about 30% of time, 50% energy in the active mode



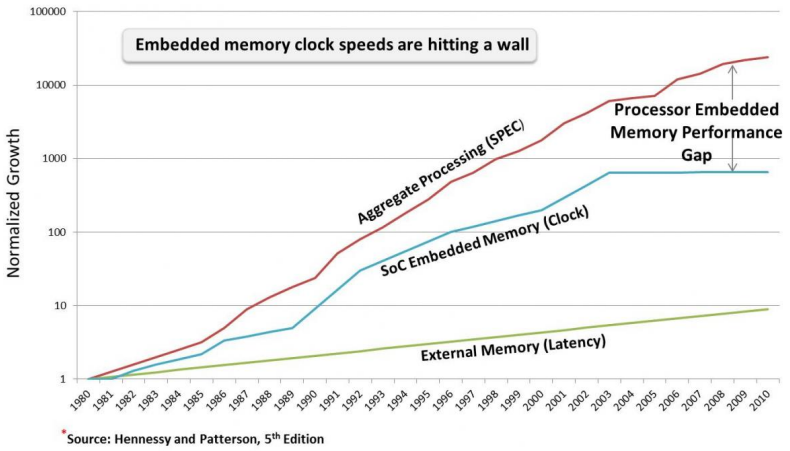
M. Aroraet al., "Understanding idle behavior and power gating mechanisms in the context of modern benchmarks on CPU-GPU Integrated systems," HPCA, 2015, pp. 366-377.

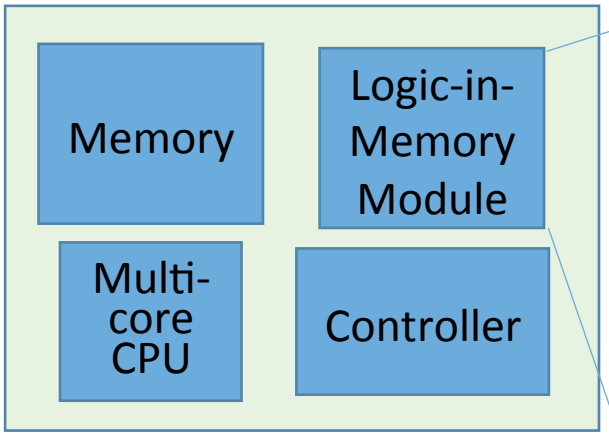


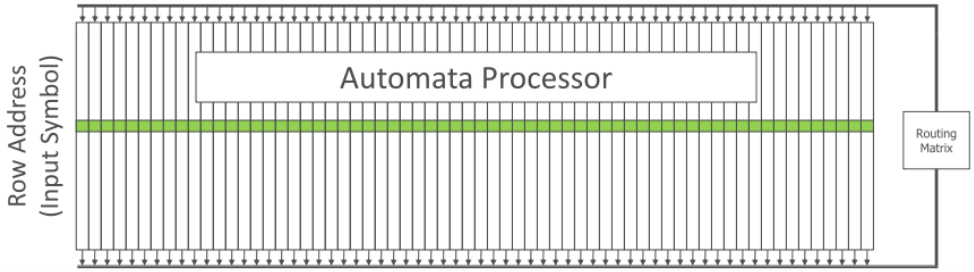


NV in Near/In-Memory Processing

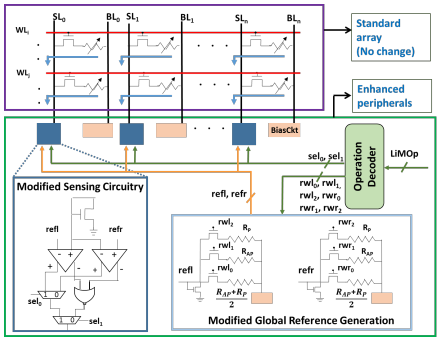
- Data analytics applications
  - Large amount of data
  - Simple operations
- Place operations close to data
  - Increase effective memory BW
  - Reduce energy consumption



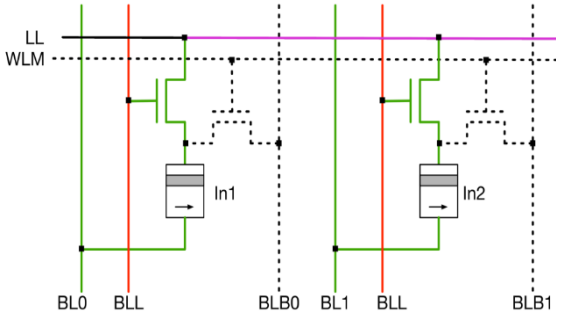




Micron's Automata Processor (Harold Noyes, 2014)

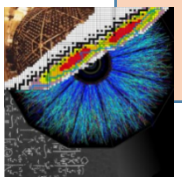


STT-LiM (Purdue)

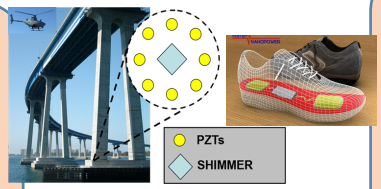


Computational RAM (Minnesota)

Exploiting Unique Properties of Spintronic Devices



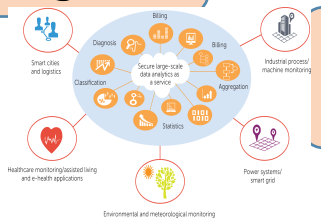
Energy proportional computing



Edge computing powered by harvested energy

Non-volatility
High energy efficiency
Diverse functionality

Near/In-memory processing



Neuromorphic computing

Stochastic computing