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Fast Tag Comparator Using Diode Partitioned Domino for 64b Microprocessors

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Abstract— **As the clock frequency and physical address space of 64b microprocessors continue to grow, one major critical path is the access to the on-die cache memory that includes a tag comparator, a tag SRAM and a data SRAM. To improve the delay of the tag comparator, a Diode Partitioned (DP) domino circuit is proposed. DP domino reduces the parasitic capacitance and enables a smaller keeper in high fan-in gates. The diode circuit is also improved by an enhanced diode that boosts up the gate voltage of the NMOS diode. Delay of a 40b tag comparator using the proposed scheme is 33% faster than an optimized complex domino circuit in 1.8V, 180nm CMOS technology.**

Index Terms— **High-speed domino circuit, keeper design, high-speed cache memory, tag comparator**

I. INTRODUCTION

Demands for high performance computing have boosted the clock frequency over 1 GHz and physical address space has reached up to 50b for 64b microprocessors. Access to the on-die cache memory consisting of a tag comparator, a tag SRAM and a data SRAM is one of the major critical paths. Since a tag comparator provides the hit/miss information to the cache controller, it cannot be executed in parallel with accessing a tag SRAM. A 64b microprocessor requires a 40b tag comparator due to the 50b physical address, which has been increasing every generation. Domino circuit style is widely used in conventional tag comparator designs. Innovative keeper and multiple-stage designs have been proposed to improve performance of such high fan-in domino circuits [1-4].

In this paper, we propose a Diode Partitioned (DP) domino for fast tag comparators. After discussing basic operations of the circuit, implementation of a 40b tag comparator using the proposed DP domino in a 1.8V, 180nm, 4-metal CMOS

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technology is presented. Simulation results on delay, power and noise robustness are also compared to those of conventional domino circuits. Scaling implications of the proposed technique is explored using predictive 130nm, 100nm and 70nm technologies [5].

II. CONVENTIONAL TAG COMPARATOR DESIGN

Fig. 1 shows a 40b tag comparator that is composed of a 2-input XOR and a 40b OR gate. Inputs $A[39:0]$ are from the tag field of the address register and $D[39:0]$ are from the tag SRAM. Since all the output signals from the SRAM are pre-charged signals, tag comparator is suitable for a footless domino design. Fig. 2 shows a 4b tag comparator using a conventional footless domino circuit. Because each 2-input exclusive OR consists of 2 legs, the 4b comparator is composed of 8 legs. The large number of legs causes the parasitic capacitance on the dynamic domino node $E[0]$ to increase significantly. In the worst case input pattern, only one out of eight NMOS paths discharges the domino node $E[0]$. Capacitance on $E[0]$ is mainly due the drain capacitance of the parallel NMOS's. In general, domino circuits are suitable for wide OR implementation. However, if the fan-in is very high, such as 80b parallel inputs for a 40b tag comparator, multiple stage design and strong keeper for a target noise robustness is needed to prevent the increased parasitic capacitance on $E[0]$ and a DC noise from the high fan-in, wide and parallel NMOS network.
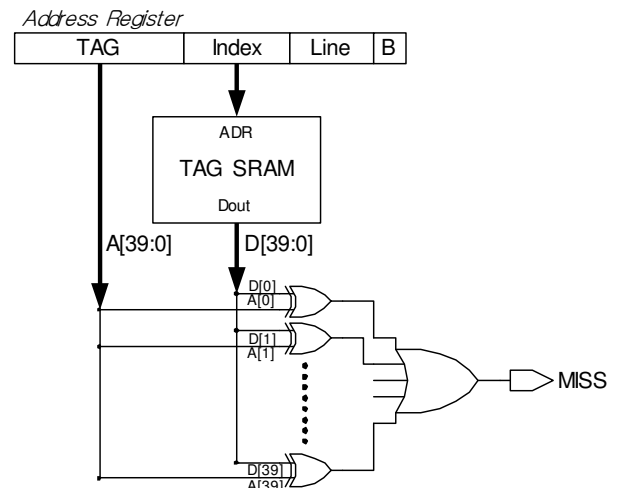

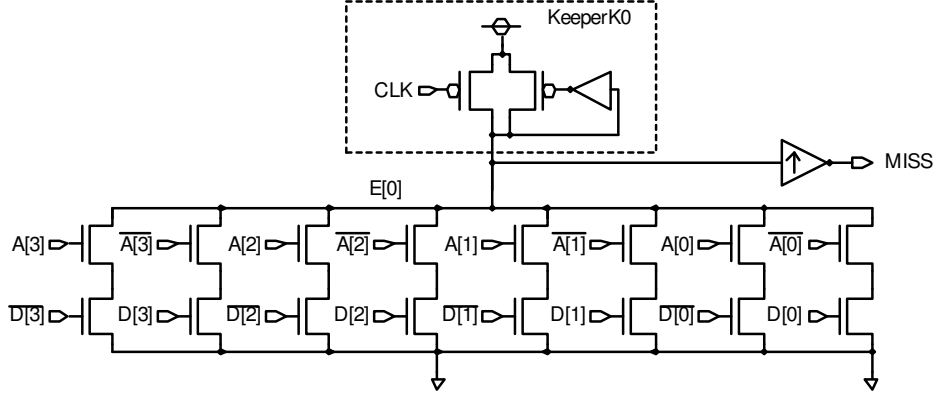Fig. 1. Block diagram of the tag memory and comparator.
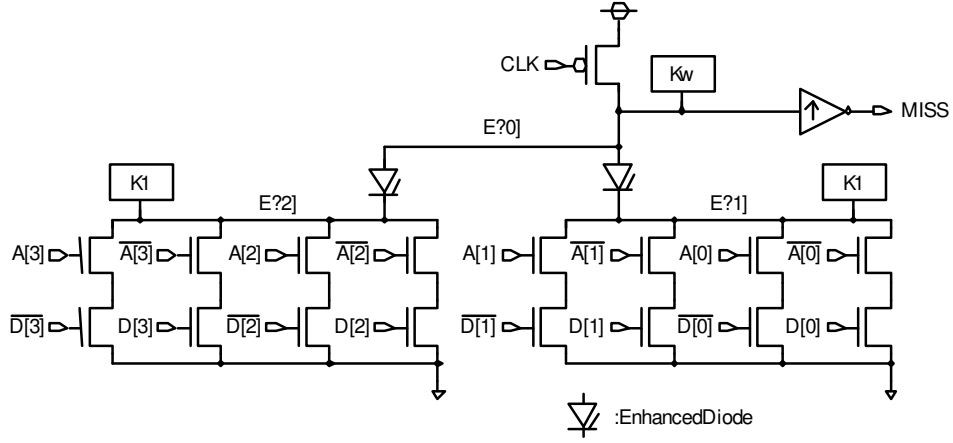
Fig. 2. Conventional footless domino circuit.

Fig. 3. Proposed Diode Partitioned (DP) domino circuit.

III. DIODE PARTITIONED (DP) DOMINO CIRCUIT

In the proposed DP domino, the enhanced diode divides and reduces the parasitic capacitance on the domino node as shown in Fig. 3. The diodes separates E[0] node into E'[0] and two partitions of E'[1] and E'[2]. With the worst case input, only $\overline{A[0]}$ – D[0] path turns on and E'[1] partition becomes active. The other NMOS paths are turned off. D[0] path discharges E'[1] and E'[0] but does not affect E'[2] due to the reverse connection of the diode. The parasitic capacitance of E[0] is divided into n ways via n diodes. The DP domino does not only divide the parasitic capacitance but also divides the keeper transistors. The $1/n$-sized keepers are distributed on each partition. That is, total size of K1 keepers is equal to that of K0. As for a NMOS driver in a partition, the contention current of the DP domino becomes $1/n$ times smaller than that of the conventional domino. This $1/n$-sized keeper can meet the same input-noise robustness because the fan-in of parallel NMOS at each partition is also $1/n$ of the original domino circuit. DP domino requires additional keeper Kw. However, its size can be very small because K1 prevents the major noise current from the NMOS networks.

In CMOS design, diode is usually implemented with an NMOS transistor. However, the small forward-bias current per transistor width W cannot be suitable for the proposed circuit because a large W would cause extra parasitic capacitance on E'[0]. To improve the forward-bias diode current, we propose an enhanced diode circuit that boosts up the gate voltage of the diode NMOS at forward-bias mode. Fig. 4 shows the schematic
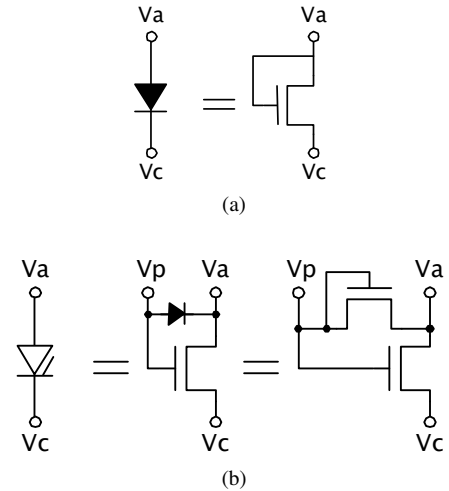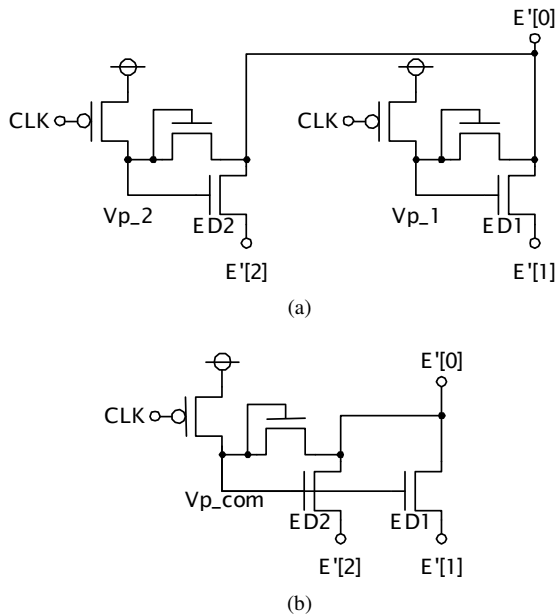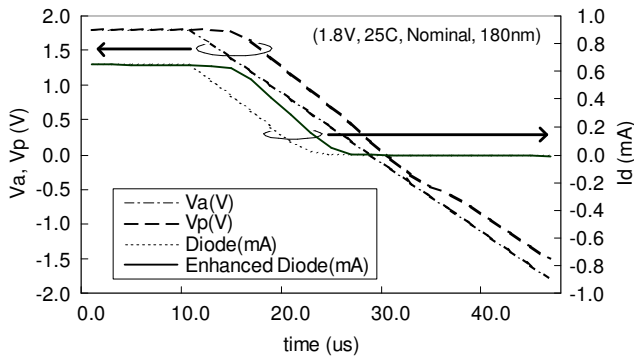

(a)

(b)

Fig. 4. Symbol and circuit schematics of (a) conventional diode and (b) enhanced diode.
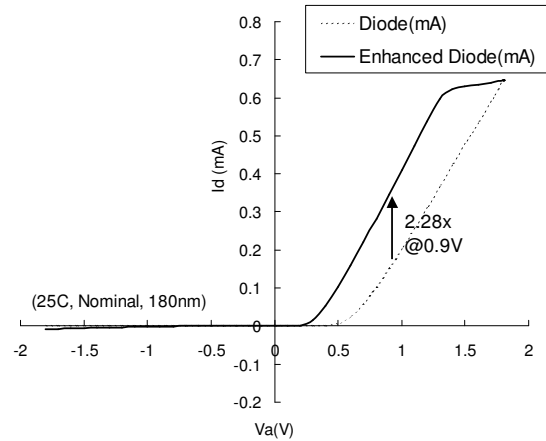
(a)

(b)

Fig. 5. Enhanced diode in the DP domino circuit, (a) individual extra diode and (b) shared extra diode.

Fig. 6. Transient characteristic of the pre-charged enhanced diode.

Fig. 7. I-V curve characteristics of the enhanced and conventional diodes. Current of enhanced diode is 2.28 times higher than NMOS diode at 0.9V.

of the conventional diode and proposed enhanced diode circuit. The gate node of the conventional NMOS diode is connected to the drain as shown in Fig. 4(a). To increase the forward bias current, an extra NMOS diode is inserted between the gate (Vp) and drain (Va) node in the enhanced diode circuit as shown in Fig. 4(b). The additional diode is also implemented using an NMOS with gate and drain connected. Node Vp must be pre-charged using the clock signal of the domino. Since node Vp is also pre-charged and dynamic node, it should be protected by a keeper or an additional capacitance. Since adding capacitance won't change DC characteristics of the DP domino, we recommend to use a capacitance. Fig. 5(a) shows the enhanced diode implemented in the proposed DP domino with 2 partitions. For compact layout, the NMOS diode between Vp and Va can be shared among each enhanced diode as shown in Fig. 5(b). Suppose E'[1] is being drove down while the E'[2] remains high. At the beginning, nodes E'[1], E'[2] and Vp_com is pre-charged at high or VDD level. When E'[1] is going down below (VDD-Vth) level, the ED1 device becomes ON and E'[0]

starts to go down. Lowering E'[0] drives down the Vp_com node. On the other hand, the ED2 device never turns ON because E'[2] is always higher than E'[0] and Vp_com. In addition, E'[0] doesn't drives E'[2] because the voltage level of (Vp_com - E'[0]) is equal or less than NMOS's Vth. Fig. 6 shows transient characteristics of the enhanced diode circuit. Node Vp is initially pre-charged similar to the domino circuit. If one of the NMOS partition starts to evaluate, the cathode voltage Vc starts to drop. Since the NMOS between Va and Vc turns on, the anode Va also drops as Vc is discharged. In a conventional NMOS diode, the diode current immediately decreases as Va drops since the gate voltage of the NMOS diode (Va) also reduces. In the proposed enhanced diode however, the gate voltage of the NMOS diode (Vp) remains at a higher voltage for an extended period of time because of the diode drop between Vp and Va. Therefore, the drive current of the enhanced diode becomes larger than the conventional NMOS diode. Fig. 7 shows the I-V curve of the enhanced diode versus the conventional diode indicating a 2.28X increase in diode forward-bias current at a Vac (=Va-Vc) of 0.9V (Fig. 7).

AC operation of the diodes with 1ns cycle is also simulated to further describe the operation of the proposed enhanced diode circuit. Fig. 8(a) shows the test circuit and Fig. 8(b) shows the full-cycle waveforms starting from the pre-charged state. The low to high transition of the CLK signal causes Vc to discharge through the NMOS footer. Nodes Va' and Va follow Vc as the diodes turn on. Because of the precharged NMOS gate node (Vp), node Va in the enhanced diode discharges quickly while the discharge of node Va' in the conventional diode slows down as Va' approaches Vthn which is approximately 0.4V. During the Va transition between 0.22 and 0.35ns, Va-Vc becomes 1.17V in maximum while it is 0V (shorted) in the conventional NMOS diode. This overdriving gate voltage increases the drain current and makes the sharp and fast transition of the proposed enhanced diode. In addition, it enables to support the pull-down for full swing on node Va, while node Va' on the conventional diode remains above 0.4 V.

(a)

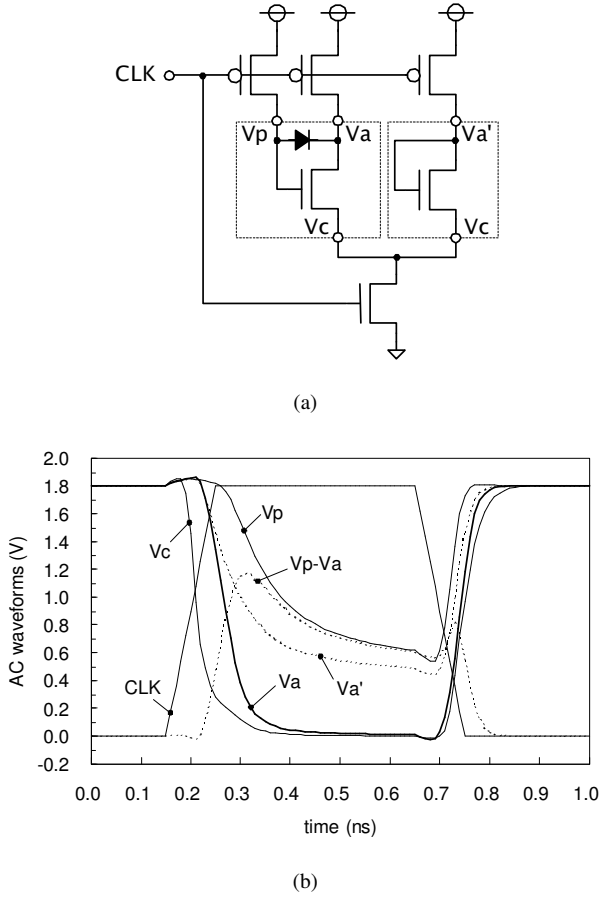
(b)

Fig. 8. AC simulation of the conventional and enhanced diode, (a) test circuit and (b) waveforms.

Fig. 9. Waveforms of 10b tag comparator.

Fig. 10. Delay Comparisons.

IV. SIMULATION RESULTS AND IMPLEMENTATION

The DP domino and conventional domino circuits are simulated in 1.8V, 180nm CMOS technology with a FO4 output load. Keeper ratio (=(W/L)$_{KEEPER}$/(W/L)$_{PULLDOWN}$) of 5% is used to meet a target DC noise robustness of VDD/4 [2]. Fig. 9 shows waveforms of each signal in Fig. 2 and Fig. 3 for 10b tag comparators. The trip point of the output inverter is skewed at 1.11V (=0.62*VDD) for fast sensing of E[0]. Due to the divided capacitance and keeper, E'[1] in the active partition sharply goes down. On the other hand, E'[2] in the inactive partition does not change. This isolation reduces delay and power by 22% and 40%, respectively. Here, power is evaluated for the same worst-case input pattern.

Fig. 10 compares delay of DP and conventional domino circuits for different fan-in sizes. For example, 12b tag comparator, which is composed of 24 legs, can be divided into 2 ways of 12-NMOS groups, 4 ways of 6-NMOS groups and so on. Here, the solid line of DP domino traces the smallest delays among n-way partitioned design on each fan-in. DP domino can operate at very large fan-in such as 48b while the conventional domino starts to fail at 20b. We simulated DP domino up to 120b and the circuit still operates at 387ps. The proposed DP domino can have several configurations in term of the number
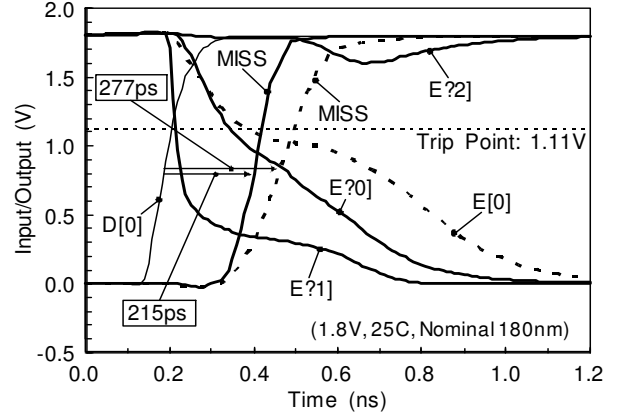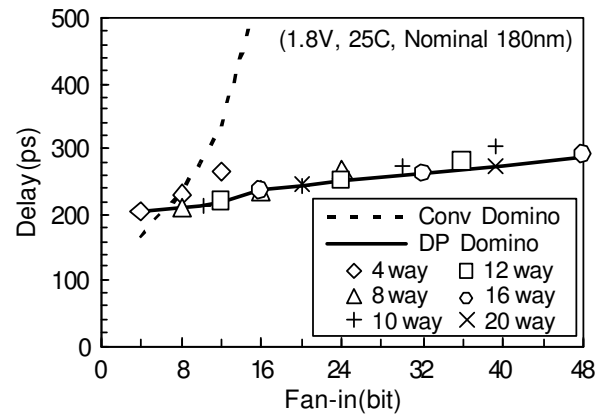
of partitions. For example, the 40b DP domino exclusive OR gate consisting of 80 legs can designed to be 10-way with 8 legs per partition or 20-way with 4 legs per partition. For the 40b tag comparator, the 20-way is the fastest design as shown in Fig. 10. To improve delay of DP domino, having many ways makes the distributed keeper small. That is, contention current of the keeper is reduced. On the other hand, having too many ways increases the parasitic capacitance on E'[0]. Although the 4 or 8 legs per partition were the fastest circuit configuration in our design, the best number of ways depends on the balance between the parasitic capacitance and keeper's contention current. That is, the optimal number of ways would be change depending on the process technology and target noise tolerance. For example, under the lower criteria of input DC noise tolerance, the required contention current of the keeper becomes smaller. In other words, one partition can contain more legs with the same size of a local keeper. Hence, having smaller number of ways can reduce the parasitic capacitance more effectively. In an SOI process with smaller source/drain capacitance, increased number of ways can effectively reduce contention current from the keepers while keeping the junction capacitance minimal. In addition, the impact on layout area must be considered when deciding the optimal number of partitions. Delay of a 16b comparator with 16-way partition for example, is very close to
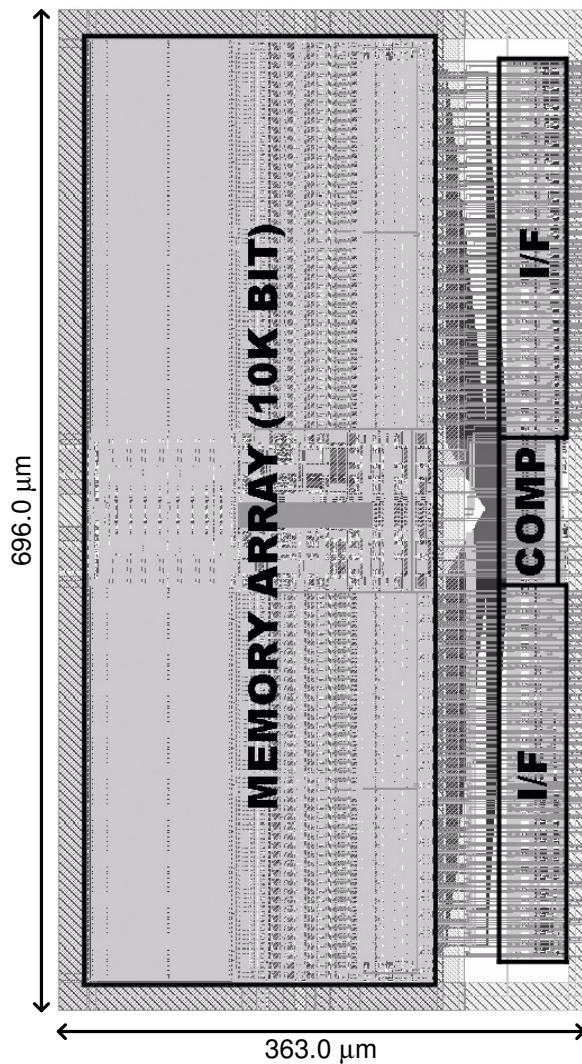
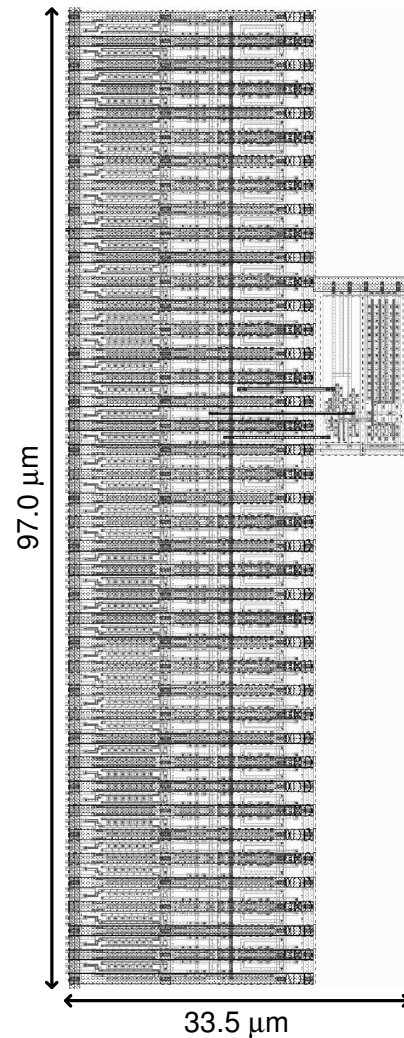**Fig. 11.** 256k-entry 40b tag memory layout.

Fig. 12. Layout of the 40b tag comparator block using DP domino.
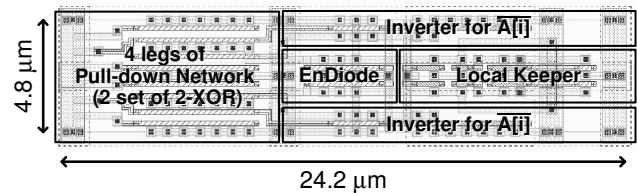
Fig. 13. Layout of one-partition leaf cell composed of four legs of NMOS network and a enhanced diode.

that of an 8-way partition. Hence, the 8-way design would be preferable for compact area.

A 40b tag comparator with a 256-entry tag memory array using the proposed DP domino technique is implemented in a 1.8V, 180nm, 4-metal CMOS technology. Fig. 11 shows the tag memory layout with area of 363.0 μm x 696.0 μm. The tag comparator, "COMP", is placed between the "I/F" circuits composed of data latches and selectors connecting to an instruction-fetch or a data-fetch unit. The tag comparator part is enlarged in Fig. 12. In order to minimize the parasitic capacitance at the dynamic node E'[0] inside the DP domino, we laid out all transistors of the NMOS network into a compact area of 35.5 μm x 97.0 μm. The metal lines that connect between the tag comparator and sense amps consume an additional 4.6% area due to the dual-rail-input circuit. This extra area can be significantly reduced when implemented in an advanced technology with more number of metal layers. The delay and power consumption of the proposed 40b tag comparator are 273 ps and 3.51 μW/MHz, respectively. Fig. 13 shows the layout of one partition cell. Four legs of NMOS network, or 2 sets of 2-input exclusive OR, is laid out on the left half. Inverters for

the address signals are located on the top and bottom on the right. The enhanced diode and local keeper is laid out at the center of the right half. Although the area penalty due to the enhanced diode and local keeper circuit is 30% of each partition cell, the impact on total tag memory area is less than 2% as shown in Fig. 11.

We also compared the delay and the power consumption to the conventional circuits. Conventionally, a 40b tag comparator is designed using (i) 2-stage domino with 4b tag comparator and 10b OR, or (ii) complex domino with 10b tag comparator and 4-input NAND output driver because conventional domino circuit technologies make a multiple-stage structure faster than

V. Conclusions

A fast 40b tag comparator for 64b microprocessors using DP domino has been proposed. DP domino reduces the parasitic capacitance and keeper size of a high fan-in gate. DP domino also offers a 33% delay improvement over a conventional complex domino circuit for fast tag comparison in 1.8V, 180nm CMOS technology. Scaling implications of the proposed technique is also simulated in predictive 130nm, 100nm and 70nm technologies. Even for the future technologies, the proposed DP domino circuit has significant advantages over the conventional domino techniques.

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