Distributed Active Decoupling Capacitors for On-Chip Supply Noise Cancellation in Digital VLSI Circuits

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Abstract

A distributed active decoupling capacitor (decap) circuit is proposed to suppress the on-chip power supply noise in digital VLSI circuits. Effectiveness on suppressing local supply noise is verified from a 0.18μm test chip using multiple on-chip supply noise generators and supply noise sensors. Measurements show 4-11X boost in decap value over conventional passive decaps for frequencies up to 1GHz. Decap area reduction of 40% is achieved.

Introduction

On-chip supply voltage fluctuations in digital VLSI circuits pose a major threat to robust circuit operation affecting speed, power, noise margin, and long term reliability [1]. Passive decoupling capacitors (decaps) implemented with MOS capacitors are no longer adequate in controlling the supply noise due to the effects of gate tunneling leakage through the thin insulating oxide and the large die area consumed. To overcome these major limitations of conventional passive decaps, this paper proposes and experimentally verifies a distributed active decap circuit that can efficiently reduce power supply fluctuations. Unlike prior work which deals with global resonant noise below 200MHz [2], this work can additionally suppress local supply noise with frequencies up to 2.7GHz.

Active Decap Circuit Design

Active decaps were previously used for the suppression of substrate crosstalk in mixed-signal ICs [3]. Fig. 1 shows the principle of our proposed active decap circuit that is targeted towards the suppression of supply noise due to finite on-chip and off-chip parasitic impedances in digital ICs. The proposed circuit consists of an operational amplifier (opamp) and a passive load capacitor C_{load}. The feedback loop detects changes in the voltage VDD-Gnd and drives the load capacitance, effectively amplifying the capacitance seen at the VDD input to $(1+A(\omega))\cdot C_{load}$ via the Miller effect, where $A(\omega)$ represents the gain of the opamp. Fig. 2 shows the opamp design. The noise on the VDD and Gnd lines are capacitive-coupled to the inputs of the differential stage. A source follower stage is used to drive the output capacitance load of 1 pF. Simulations verified a DC gain of 9.5, a bandwidth of 535 MHz, a unit gain frequency of 2.7GHz, and a phase margin of 42 degrees. The low frequency cutoff due to the two input capacitors is at 1 MHz and the current dissipation is 3.8mA during normal operation. The opamp is self-contained with no external bias voltage required so that the circuit can be easily distributed across the chip for local power supply regulation. Two multiplexers are inserted so that the opamp can be deactivated during standby mode using a select signal. HSPICE simulations confirm an 11X-1X boost in the effective decoupling capacitance for a frequency range of 1MHz-2.7GHz.

A 2.7mmx1.9mm test chip was fabricated in a 0.18μm, 1.8V, 6-metal, triple-well CMOS technology to verify the effectiveness of active decap circuit (Fig. 8). Fig. 3 shows the organization of the test chip with the circuit components. To generate switching noise on the supplies, two types of noise generation circuits were implemented: eight sets of 16-bit Linear Feedback Shift Register (LFSR) circuits and fifteen sets of external noise injection circuits as shown in Fig. 3. The noise injection circuit is capable of injecting noise into either VDD or Gnd or into both. Both noise generation circuits are controlled by an on-chip voltage controlled oscillator whose frequency can be varied up to 1.3GHz. By turning on different numbers of LFSR circuits or noise injection circuits, the magnitude of supply noise can be adjusted. Two types of sensors were placed at four different locations on the die to detect the local supply voltage droop with floorplan shown in Fig. 6. The differential supply noise VDD-Gnd was measured using a separate active decap circuit that drives an output pad instead of a load capacitor. The sensors shown in Fig. 3 are used to capture VDD and Gnd noise separately [4]. Finally, different numbers of passive and active decaps are evenly distributed around the noise sources to provide the decoupling effect.

Supply Noise Suppression Measurements

Fig. 4 shows the measured decoupling effects of active decaps and passive decaps up to 1GHz. The supply noises normalized to those without using any decaps are shown when either the LFSR circuits or the noise injection circuits are activated. The measurements show that the 10pF active decap offers the same decoupling effect as an 80-120pF passive decap up to 500MHz. The decoupling effect of active decaps decrease at frequencies above 500MHz offering similar performance as a 40pF passive decap at 1GHz. Fig. 4 also shows that the decoupling effect for both techniques increases with frequency up to 700MHz. This increase can be explained via an RLC model which shows that the decoupling effect is given by $(1+RC_0\omega j-LC_0\omega^2)/(1+R(C_d+C_0)\omega j-L(C_d+C_0)\omega^2)$, where C_0 is the capacitance from the non-switching circuit (~40pF in this work) and C_d denotes the additional decoupling capacitance. At higher frequencies, the decrease of decoupling effects is due to parasitic resistance and inductance in the passive decaps and due to the decrease of amplifier gain in the active decaps.

Fig. 5 shows measured waveforms of VDD, Gnd, and VDD-Gnd noises which were generated by a single 16-bit LFSR circuit operating at 120MHz. The differential noise is measured by the active decap sensor with a gain of 5 and output biased at 0.32V. The inset shows the VDD noise measured at different sensor locations. Similar decoupling effects can be observed from all four sensors. Note that the Gnd noise was measured to be less than 50% of VDD noise due to the substrate contact and extra number of Gnd pads in the I/O circuits. Fig. 6 shows the noise values when activating 120MHz LFSR blocks at different locations. Higher noise is observed at a location nearer to the active noise source. The results in Fig. 5 and Fig. 6 are consistent with those shown in Fig. 4 and confirm a 8-11x boost in decap value within the bandwidth of active decaps.

The power dissipation of the active decaps can be further reduced in standby mode by deactivating them using select signals. Fig. 7 shows the measured waveform of VDD noise and active decap output during switching events. The select signal toggles at 200kHz with rising and falling time of less than 10ns. The figure shows that the active decaps can be turned off immediately because of the deactivation of the opamp while the wake-up time is around 200ns due to the charging period of the input capacitors. Layout comparison of the active decap and an equivalent 10pF passive decap in Fig. 8 indicates a decap area reduction of 40%.

Acknowledgements

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Reference

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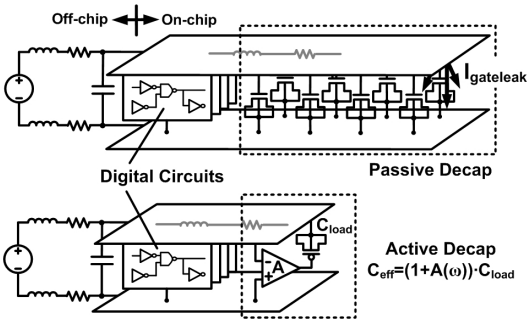

Fig. 1. Principle of proposed active decap circuit for supply noise suppression.

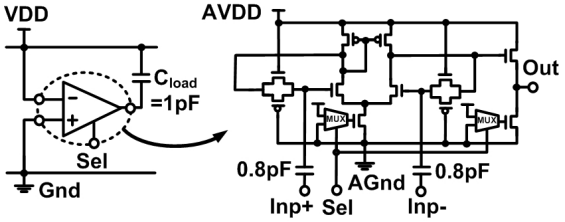

Fig. 2. Schematic of proposed active decap circuit.

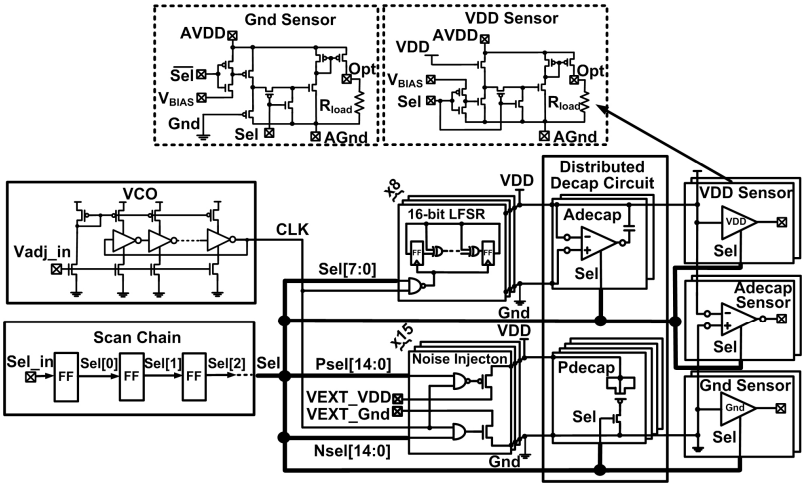

Fig. 3. Organization of the test chip.

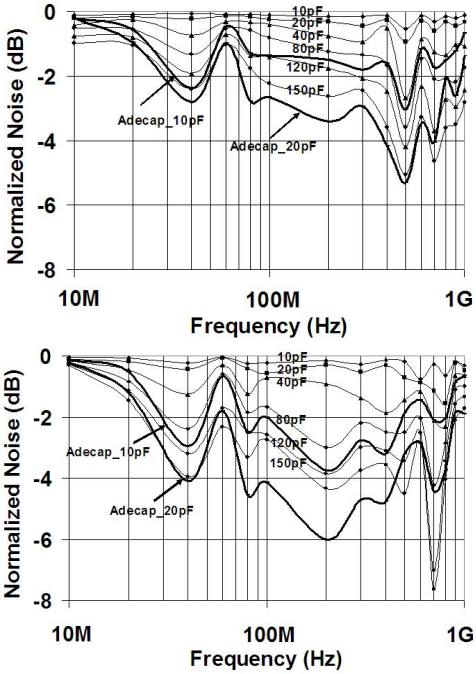

Fig. 4. Measured decoupling effect for noise generated by LFSR circuits (top) and noise injection circuits (bottom). Differential noise VDD-Gnd is measured.

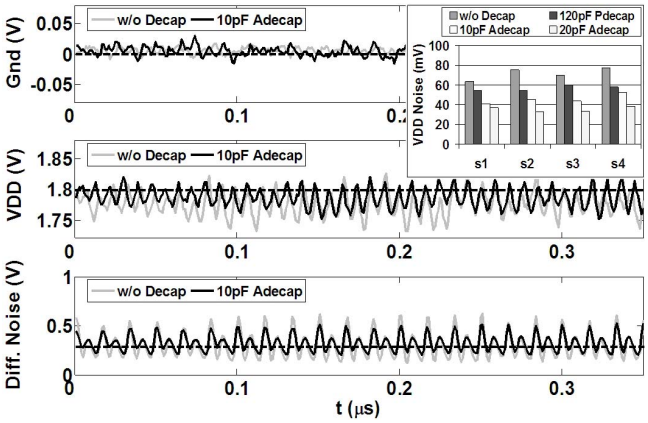

Fig. 5. Measured VDD, Gnd, and VDD-Gnd waveforms while a single LFSR circuit operates at 120MHz. The inset shows the measured VDD noise value at four different sensor locations s1, s2, s3, s4 as illustrated in Fig. 6.

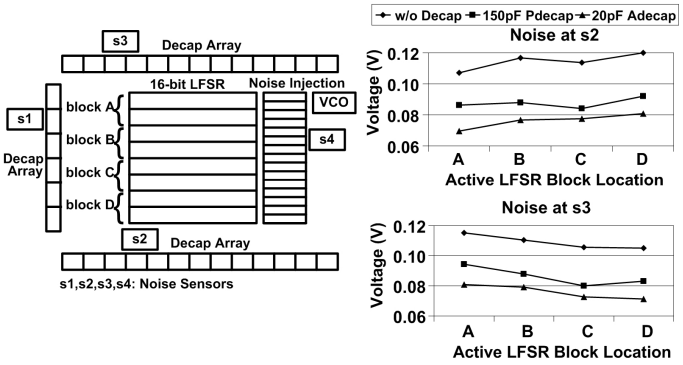

Fig. 6. Floorplan of the test chip (left) and measured noise from sensor 2 and 3 with various active LFSR block location (right). Each LFSR block contains two 16-bit LFSR circuits.

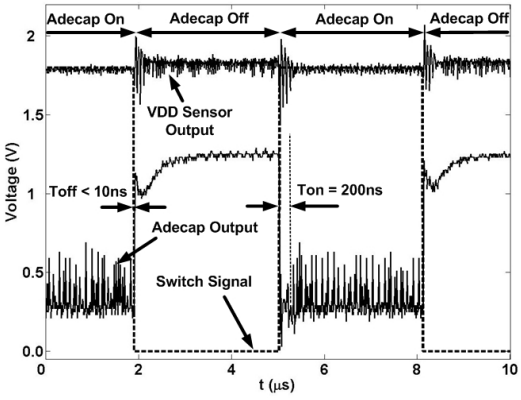

Fig. 7. Measured waveforms of VDD noise and active decap output when turning on and off the active decap circuit.

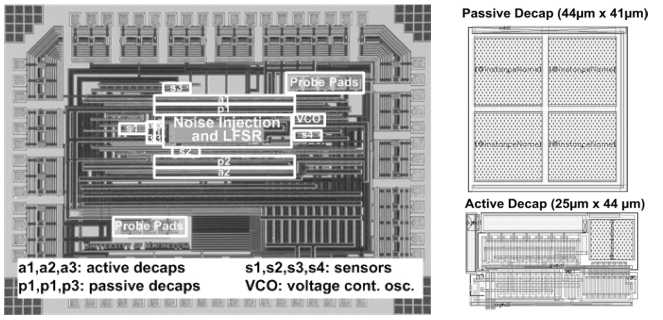

Fig. 8. Micrograph of the test chip (2.7mm×1.9mm) and layout comparison of active decap and equivalent 10pF passive decap.