An On-Die CMOS Leakage Current Sensor for Measuring Process Variation in Sub-90nm Generations

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Outline

- Motivation and prior art
- Proposed leakage sensing technique
- Leakage sensor test chip implementation in 90nm
- Leakage binning results
- Conclusions
- $I_{OFF}$ spread > 100X, $I_{ON}$ spread > 2X
- Device parameters are NOT deterministic any more
Process Variation Detection

Off-current meas.

- Sub-threshold CMOS device:
  - T. Kuroda, JSSC, Nov. 1996
- Test row devices
  - Process monitor
- Decay sensors

On-current meas.

- Strong inversion CMOS device:
  - M. Griffin, JSSC, Nov. 1998
  - Y. Kim, IEICE, Nov. 1999
- Delay line:
  - M. Miyazaki, ISLPED, Aug. 1998

- Process detection method optimized for each application
- Resolution, area, complexity, testing cost, etc.
Leakage Variations Impact

Dynamic circuit NMOS pull-down leakage variation:
- Keeper size determined for target robustness at worst-case leakage corner
- Excess leakage dies: fail to meet target robustness
- Lower leakage dies: over-designed for robustness

Dynamic 8-way Bitline

R. Krishnamurthy et al, VLSI Circuits Symp. 2001
Target Application: Process Compensating Dynamic Circuit

3-bit programmable conditional keeper

On-die leakage current sensor required to generate \( b[2:0] \) based on NMOS pull-down leakage

C. Kim, S. Hsu et al, VLSI Circuits Symp. 2003
Usage Model and Design Goal for On-Die Leakage Sensor

- High leakage sensing gain (> 3b resolution)
- No complicated timing control
- Compact analog design
Previous Leakage Current Sensing Circuits

- Susceptible to P/N skew and supply fluctuation
- Large area due to multiple analog bias circuits
- Limited leakage sensing gain

T. Kuroda et al., JSSC, Nov. 1996
M. Griffin et al., JSSC, Nov. 1998
Proposed Single Channel Leakage Sensing Circuit

- Basic principle: Drain induced barrier lowering
- Low sensitivity to P/N skew and supply fluctuation
PV Insensitive Current Reference ($I_{\text{REF}}$)

- Sub-1V process, voltage compensated MOS current generation concept
- Reference voltage, external resistor not required
- Scalable, low cost, flexible solution

S. Narendra et al., VLSI Circuits Symp. 2001
PV Insensitive Bias Voltage ($V_{BIAS}$)

\[ V_{BIAS} = \frac{kT}{q} \log \left( \frac{W_1}{W_2} \right) \]

($W_1 = 96 \mu\text{m}$, $W_2 = 2 \mu\text{m}$)

- PTAT containing no resistive dividers
- Based on weak inversion MOS characteristics
- Desired output voltage achieved via sizing

E. Vittoz et al., JSSC, June 1979
Comparator

- 2-stage differential amplifier
- Already designed $I_{REF}$ is used for bias current

Subtraction circuit

$I_{REF}$
PV Sensitivity of Designed $I_{\text{REF}}, V_{\text{BIAS}}$

- $I_{\text{REF}}$ variation < 4%, $V_{\text{BIAS}}$ variation < 2%
- Under realistic process skews, $\pm 100\text{mV}$ supply voltage fluctuations

1.2V, 90nm CMOS, 80°C
Proposed Leakage Current Sensing

\[ I_{REF} \]

M1 (saturation)

M2 (sub-threshold)

\[ V_{BIAS} \]

\[ V_{SEN} \]

\[ d0 \]

\[ V_{REF} \]

PMOS M1

NMOS M2

\[ I_{ds} \]

\[ V_{SEN} (V) \]

\[ 1.2V, 90nm \text{ CMOS, } 80^\circ C \]
Superimposed I-V Curves

- 1.9-10.2X higher V_{SEN} swing than prior-art
- Process-voltage insensitive design

1.2V, 90nm CMOS, 80°C

$\Delta V_{SEN} = 0.93V$
6-Channel Leakage Sensor Test Chip

- Incremental mirroring ratio for multi-bit resolution leakage sensing
- Shared bias generators → compact design
- Process-voltage insensitive $I_{\text{REF}}, V_{\text{BIAS}}$ gen.
Multi-Bit Resolution Leakage Sensing

1.2V, 90nm CMOS, 80°C

<table>
<thead>
<tr>
<th>Voltage (V)</th>
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<tr>
<td>1.2</td>
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<tr>
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</tr>
<tr>
<td>0.2</td>
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Process skew

- Leakage level determined by comparing $V_{\text{SEN1}}$ through $V_{\text{SEN6}}$ with $V_{\text{REF}}$
- 6-channel leakage sensor gives 7 level resolution
Example: Operation at Fast Process Corner

- Fast corner: output code ‘101’
Example: Operation at Typical Process Corner

• Typical corner: output code ‘010’
## On-Die Leakage Sensor Test Chip

### Key Features
- **Technology**: 90nm dual-$V_t$ CMOS
- **$V_{DD}$**: 1.2V
- **Resolution**: 6 channels (7 levels)
- **Power consumption**: 0.66 mW @ 80°C
- **Dimensions**: 83 X 73 $\mu$m²

<table>
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<tr>
<th>Feature</th>
<th>Specification</th>
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<tr>
<td>Technology</td>
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Leakage Sensor Results

- Effective leakage binning for PCD technique
- Scalable beyond 90nm generation

1.2V, 90nm CMOS, 80°C

Leakage current (normalized)

Output codes from leakage sensor

Die count (%)
Conclusions

- Post silicon tuning is becoming promising for process compensation
- On-die leakage current sensors assist inter/intra-die process compensation
- Multi-channel leakage current sensor
  - No complicated timing control
  - 1.9-10.2X higher sensitivity to leakage
  - Shared analog components for compact design