A Process Variation Compensating Technique for Sub-90nm Dynamic Circuits


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Outline

- Motivation
- Parameter Variation and Keeper Sizing
- Process Compensated Dynamic Circuit
- 90nm Delay, Robustness Squeeze
- 128x32b PCD Register File Results
- Summary
Motivation

- Substantial variation in leakage across dies
- 4X variation between nominal and worst-case leakage
- Performance determined at nominal leakage
- Robustness determined at worst-case leakage

(150nm CMOS Measurements, 110°C)

Normalized $I_{OFF}$

Number of dies

0 1 2 3 4 5 6 7

0 50 100 150 200

nominal corner

worst-case corner
Leakage Variations Impact

- Dynamic circuit NMOS pulldown leakage variation:
  - Keeper size determined for target robustness at worst-case leakage corner
  - Excess leakage dies: fail to meet target robustness
  - Lower leakage dies: over-designed for robustness
Fast corner keeper sizing is sub-optimal for delay.

90nm CMOS, 1.2V, 110°C simulations

DC robustness (normalized to Vcc)

Normalized delay

Target noise robustness
Nominal corner
Worst-case corner

● Fast corner keeper sizing is sub-optimal for delay
Variable Strength Keeper Size

Goal: downsize keeper on nominal leakage dies

90nm CMOS, 1.2V, 110°C simulations

Target noise robustness

Normalized delay

23% speedup

Nominal corner

Worst-case corner

DC robustness (normalized to Vcc)

Goal: downsize keeper on nominal leakage dies
Process Compensating Dynamic Circuit Technology: Evolution

- Secondary conditional keeper activated under excessive leakage conditions
- Deactivated during nominal mode operation

A. Alvandpour et al, CICC’02
Process Compensating Dynamic Circuit Technology

3-bit programmable conditional keeper

- b[2:0]
- clk
- RS0
- D0
- RS1
- D1
- RS7
- D7
- LBL0
- LBL1
- N0

Shared-NAND: 2 less NMOS devices, dense layout
Delay Penalty of PCD

90nm, 1.2V, 110°C

Normalized delay

- 3b keeper
- Ideal

Delay penalty

W\text{KEEPER}_1 = 1.7%
W\text{KEEPER}_2 = 3.4%
W\text{KEEPER}_3 = 6.8%

Delay penalty is offset by opportunistic speedup
Robustness Squeeze

5X reduction in robustness failing dies
Delay Squeeze

- 10% opportunistic speedup

- PCD $\mu = 0.90$
- Conv. $\mu = 1.00$
- $\mu$ : avg. delay

Legend:
- Conventional
- This work
Keeper Ratio Distribution

- Conventional: 8% keeper downsized (92% of dies)
- 8% keeper upsized (8% of dies)

- Keeper downsized in 92% of dies
## Effectiveness of PCD

90nm, 1.2V, 110°C

<table>
<thead>
<tr>
<th></th>
<th>Robustness</th>
<th>Delay</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>$\mu$</td>
<td>$\sigma/\mu$</td>
</tr>
<tr>
<td>Conventional</td>
<td>1.00</td>
<td>9.4%</td>
</tr>
<tr>
<td>This work</td>
<td>0.85</td>
<td>4.2%</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>% of robustness failing dies</th>
</tr>
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<tbody>
<tr>
<td>Conventional</td>
<td>1.1%</td>
</tr>
<tr>
<td>This work</td>
<td>0.2% (5X ▼)</td>
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### 2 bit Control vs. 3 bit Control

90nm, 1.2V, 110°C

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<tbody>
<tr>
<td></td>
<td>$\mu$</td>
<td>$\sigma/\mu$</td>
</tr>
<tr>
<td>PCD 2 bit</td>
<td>0.87</td>
<td>5.2 %</td>
</tr>
<tr>
<td>PCD 3 bit</td>
<td>0.85</td>
<td>4.2 %</td>
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- Less squeeze in robustness and delay
- Limited keeper range/resolution
- Lower delay penalty
- Smaller diffusion cap. on domino node
128x32b 2R2W PCD Register File

- Single-ended read, 8 bitcells/LBL, 8-way GBL
- Keeper folded into existing layout templates

x2 Read Ports

AD 7
7:128
RS<127:0>

x2 Write Ports

AD 7
7:128
WS<127:0>

3b KPR = Programmable 3 bit keeper

GBL
D<31:0>

3b KPR
LBL14
LBL15
...

x32 bits

x8 RF Cell

3b KPR
LBL0
LBL1
LBL14
LBL15

3b KPR
PCD Register File Delay, Energy

90nm, 1.2V, 110°C

Register file delay breakdown

- Speeds up 67% of RF critical path delay
- 2% worst-case total energy overhead
**PCD Register File Results**

- **Normalized Read Delay**: 0.8, 0.9, 1.0, 1.1, 1.2
- **Number of dies**

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<tr>
<th>Conventional Register File</th>
<th>PCD Register File</th>
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- **Read Delay Benefit**: 5.5%
- **Robustness Failing Dies**: 0.2% (5X ▼)
- **Read Delay Variation**: $\sigma/\mu$ → 6.1% → 2.3% (2.7X ▼)

**Chart Details**:
- PCD $\mu = 0.94$
- Conv. $\mu = 1.00$
- $\mu$: avg. delay

**Conditions**:
- 1.2V, 110°C
Summary

● Process Compensating Dynamic Circuit:
  – Prevents pessimistic keeper sizing
  – Digital keeper programmable based on die leakage measurements

● Delay, robustness squeeze in sub-90nm
  – 5X reduction in robustness failing dies
  – 10% opportunistic speedup

● 128x32b 2R2W PCD register file is implemented