Effectiveness of Using Supply Voltage as Back-Gate Bias in Ground Plane SOI MOSFET’s

Chris H. Kim\(^1\), Hari Ananthan\(^2\), Jae-Joon Kim\(^3\), and Kaushik Roy\(^2\)

\(^1\)Department of ECE, University of Minnesota, Minneapolis, MN 55455
\(^2\)School of ECE, Purdue University, West Lafayette, IN 47907
\(^3\)IBM TJ Watson Research Center, Yorktown Heights, NY 10598

Email: hyungil@ecn.purdue.edu

Introduction

Forward body biasing (FBB) has proven to effectively lower the threshold voltage \((V_t)\), suppress short channel effects, and reduce \(V_t\) variations in bulk CMOS \([1,2]\). Recently, a digital body biasing (DBB) technique shown in Fig. 1 has been proposed where a FBB of \(V_{db}\) is applied in active mode for high on-current and \(V_{dd}\) is applied in standby mode for low off-current \([3,4,5]\). The key advantages of the DBB scheme compared to conventional FBB is that it 1) does not require a separate body bias voltage, 2) eliminates the complicated body bias generators, and 3) achieves the desired \(V_t\) by simply adjusting the supply voltage. However, the swapped body bias in active mode causes the \(p-n\) junctions in bulk to be forward-biased, so the circuit designer has to ensure that this forward bias current through the p-sub-nwell and drain-body junctions (Fig. 2) is negligible during circuit operation. This becomes challenging even with a supply voltage \((0.5V)\) far below the \(p-n\) junction turn-on voltage \((V_{pn} > 0.9V\) at low temperatures) because \(V_{pn}\) reduces significantly with increase in temperature (Fig. 3). Thus, the DBB scheme in bulk CMOS technology is limited to either low temperature operations where \(V_{pn}\) is kept high or to ultra-low voltage applications where supply voltage is much lower than \(V_{cn}\).

Ground plane (GP) SOI MOSFET is similar to a bulk device in the sense that the back-gate bias can be used to tune the \(V_t\) depending on circuit activity \([6]\). It has further advantages over bulk such as better controllability of \(V_t\) and more importantly, the absence of \(p-n\) junctions which alleviates the issues related to forward-biased junction currents for swapped back biases. The purpose of this paper is to show that GP-SOI devices are optimal for the DBB technique due to the above-mentioned advantages, and to further compare it with double gate (DG) MOSFET’s which are considered as the most promising candidate for CMOS scaled to its ultimate limit of 20-30nm channel length.

Digital Back-Gate Biasing: Bulk vs. Ground Plane

Fig. 4 shows the device structure of the GP-SOI MOSFET with undoped body for MEDICI simulations. The back-gate insulator thickness (3nm) was chosen to be 1.5 times the front-gate insulator thickness (2nm) for low drain-to-back-gate capacitance and effective tuning of \(V_t\). The front gate has a work function same as n+ silicon while the back gate has a work function similar to that of p+ silicon. The bottom channel is not inverted when the DBB scheme is applied within the supply voltage range of interest \((0.4V-1.0V)\). Energy per cycle of a FO3 inverter in Fig. 5 shows that the DBB scheme in GP-SOI is more energy efficient than in bulk (see Fig. 3) due to the non-existing \(p-n\) forward bias current. In bulk devices, the \(p-n\) junction current not only aggravates the power dissipation but also shows impact on gate delay and signal rails when its magnitude becomes comparable to the device on-current. Fig. 6 shows the operating currents of a static inverter in bulk CMOS with FBB voltage equal to \(V_{dd}\). The exponentially increased forward-biased drain-body current \((I_{junc})\) fights the NMOS on-current \((I_{on})\) and slows down the charging/discharging of output nodes. This contention between \(I_{junc}\) and \(I_{on}\) also starts degrading the output high and low voltage levels. Output signal rails shown in Fig. 7 starts to collapse significantly for \(V_{dd} > 0.7V\) in bulk CMOS, whereas the signals continue to swing rail-to-rail in GP-SOI. Power dissipation and performance of a FO3 inverter is shown in Fig. 8 and Fig. 9 for bulk and GP-SOI technology. As the supply voltage is raised beyond 0.6V, the rate at which the power dissipation increases suddenly rises in the bulk CMOS case due to the turning on of the \(p-n\) junctions. On the other hand, power dissipation in GP-SOI increases moderately with \(V_{dd}\) mainly contributed by the larger switching and sub-threshold leakage power for higher frequency of operation. The DBB scheme in GP-SOI \((1.0GHz@0.4V \rightarrow 14.5GHz@1.0V)\) is more effective than in bulk \((1.6GHz@0.4V \rightarrow 4.8GHz@1.0V)\) for improving performance since the thin back-gate insulator in GP-SOI offers better modulation in device \(V_t\). The \(p-n\) junction current that fights with the on-current in bulk CMOS is not present in GP-SOI providing further improvement in operating frequency.

Ground Plane vs. Double Gate MOSFET

Device simulations were carried out using MEDICI to compare GP-SOI using DBB scheme with DG-SOI. Both GP-SOI and DG-SOI devices were designed to have same performance \((CV_{dd}/I_{on})\) by adjusting the work function of GP-SOI back-gate material. \(V_t\) roll-off in both devices was also carefully matched by using a slightly thicker body (8nm) for DG-SOI. Device dimensions of the GP and DG-SOI devices are listed in Fig. 10. DG-SOI device shows a near-ideal sub-threshold slope of 61mV/dec while the GP-SOI has a slightly larger slope of 90mV/dec (Fig. 10). Device I-V characteristics in Fig. 11 show that GP-SOI with DBB scheme has 31X higher leakage in active mode compared to DG-SOI due to the worse sub-threshold slope. By dynamically switching the back-gate bias to 0V in standby mode, GP-SOI achieves 90X lower standby leakage over DG-SOI. However, the DBB scheme is more sensitive to supply and ground noise as shown in Fig. 12.

Conclusion

GP-SOI MOSFET’s are optimal for the DBB scheme offering high on-current and low design complexity without having power/performance issues related to the forward-biased \(p-n\) junction current in bulk CMOS. It is also shown that GP-SOI can deliver same performance as DG-SOI at 90X lower standby leakage by dynamically switching the back-gate bias.

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References

[5] H. Ananthan et al., 2004 ISLPED, to be published
Fig. 1. Digital body biasing (DBB) scheme using $V_{dd}$ as FBB voltage [1,2,3].

Fig. 2. P-n junction forward bias current problem in bulk CMOS for DBB scheme.

Fig. 3. P-n junction forward bias current in bulk signifies at high temperatures for DBB scheme.

Fig. 4. Device structure of ground-plane (GP) SOI MOSFET with back-gate biasing.

Fig. 5. Energy per cycle for DBB scheme in GP-SOI technology.

Fig. 6. P-n junction current ($I_{junc}$) in bulk contends with $I_{on}$ aggravating performance, degrading signal rails, and increasing static power.

Fig. 7. Signal rails in bulk and GP-SOI for DBB scheme.

Fig. 8. Power dissipation and performance of DBB scheme in bulk CMOS.

Fig. 9. Power dissipation and performance of DBB scheme in GP-SOI technology.

Fig. 10. Sub-threshold slope of GP and DG-SOI devices for comparisons.

Fig. 11. I-V curves of GP ($V_{bg}$=0, $V_{dd}$) and DG SOI MOSFET’s.

Fig. 12. Sensitivity of gate delay to supply voltage in GP and DG-SOI.