Modeling and Analysis of Leakage Induced Damping Effect in Low Voltage LSIs

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ABSTRACT

Although there has been extensive research on controlling leakage power, the fact that leaky transistors can act as a damping element for supply noise has been long ignored or unnoticed in the design community. This paper investigates the leakage induced damping effect that helps suppress the supply noise. By developing physics-based impedance models for active and leakage currents, we show that leakage, particularly gate tunneling leakage, provides more damping than strong-inversion current. Simulations were performed in a 32nm CMOS technology to validate our models under PVT variations and to explore the voltage dependent behavior of this phenomenon. Design example utilizing leakage induced damping such as decap assignment is discussed with results showing 15.6% saving in decap area.

Categories and Subject Descriptors

B.7.2 [Hardware]: Integrated Circuits – Design Aides.

General Terms

Management, Performance, Design,

Keywords

Damping effect, subthreshold leakage, gate leakage, supply noise

1. INTRODUCTION

With aggressive CMOS scaling, the power density of microprocessors is increasing exponentially towards that of a nuclear reactor [1]. Power supply noise which includes *IR* and *Ldi/dt* components has become a major design concern due to the ever-increasing current density, higher switching speeds and reduced operating voltages with technology scaling. Uncontrolled supply noise threatens circuits in nanoscale technologies by causing problems such as timing violations, reduced noise margin in storage circuits, substrate noise coupled into analog devices, and reliability issues due to hot carrier injection.

One challenging task in designing robust power supply networks is the damping of supply noise, particularly at the resonant frequency determined by the bonding wire inductance and on-chip capacitance [2]. Resonant supply noise can be excited even by weak sub-harmonics of the clock signal [3]. Without sufficient damping, this noise can result in a severe degradation of circuit performance due to the large impedance of the supply network at the resonant frequency.

A common method for suppressing resonant noise is to lower the ac impedance of the supply network by adding a large amount of decoupling capacitors (decaps) [4]. However, this approach has limitations such as the significant increase in gate leakage, which has already been reported to account for 15% to 20% of the total power in current microprocessors [5]. Another commonly used method to suppress resonant noise is adding passive or active resistors in series or parallel to the supply and ground networks to provide more damping [6-7]. The drawback of adding resistors in series with the power line is the increase in *IR* droop, while adding resistors between V_{dd} and *Gnd* will introduce more static current. Circuit techniques have also been proposed to deal with the supply noise issue. Ang demonstrated a switched decoupling capacitor circuit to boost the effectiveness of decaps when resonant noise is excited [8]. Rahal-Arabi proposed a clock/data compensation scheme for resonant noise tolerance where extra timing margin is obtained by matching the clock delay with the circuit delay [9]. This scheme relies on the fact that for a sudden current spike, the supply voltage starts to oscillate at the resonant frequency and lasts a few clock cycles.

Leakage power consumption, including both subthreshold leakage and gate leakage, has become the major barrier for the continued scaling of CMOS devices. According to the International Technology Roadmap for Semiconductors (ITRS), leakage power consumption will take up as much as 50% of the total power consumption in deeply scaled CMOS technologies [10]. However, a commonly ignored fact is that a device conducting leakage current between V_{dd} and *Gnd* acts as a resistor (linear or nonlinear) that can help damp the supply noise. As will be shown in the paper, ignoring this effect can lead to a pessimistic power supply network design resulting in wasted area and power.

In this work, we study, model, and verify the damping effect induced by on-chip current components including both active and leakage current. To the best of our knowledge, the only previous publication that examined this phenomenon is [11]. However, no device level modeling was provided, and the simulation was only performed on a voltage-controlled resistor instead of real CMOS transistors. Here we have studied and examined this damping phenomenon in great detail. Simulations in this paper are based on a 32nm Predictive Technology Model with a supply voltage of 0.9V [12]. The contributions of this paper are as follows:

- For the first time, simple yet accurate damping models for active current, subthreshold leakage, and gate leakage are provided and verified by simulations.
- The voltage dependent behaviors of leakage induced damping effects are explored under Process-Voltage-Temperature (PVT) variations.

- Design issues such as decap assignment and supply mesh planning are discussed and simulation results are provided to support our conclusions.

The rest of this paper is organized as follows. In section 2, a power supply network model is introduced with the various resistance components. In section 3, physical models of damping resistance for various current components are derived. Section 4 shows simulations on damping effects under PVT variations. Section 5 discusses the associated circuit design issues. Finally, conclusions are drawn in section 6.

2. POWER SUPPLY MODELING AND RESONANT DAMPING

Fig.1 shows the *RLC* model of a power supply mesh with the supply noise spectrum. The peak response at f_{res} in Fig. 1(b) indicates the resonant frequency of the supply network, which is equal to $1/(2\pi\sqrt{LC})$, where L is the inductance of the bonding wire and C is the on-chip capacitance. Although on-chip power grids also introduce parasitic inductance which accounts for the small peaks at higher frequencies, the noise at f_{res} is a magnitude higher than the others. As a result, much of the design effort is put into suppressing the supply noise at the resonant frequency f_{res}.

A popular method used to reduce the resonant noise is to provide sufficient damping by adding more resistance to supply network. Fig.1 (b) shows the noise level before and after adding a damping resistor to the power lines. The resonant noise is shown to be greatly reduced with the additional damping. As mentioned, the drawback of adding more damping is increased *IR* droop and additional power consumption.

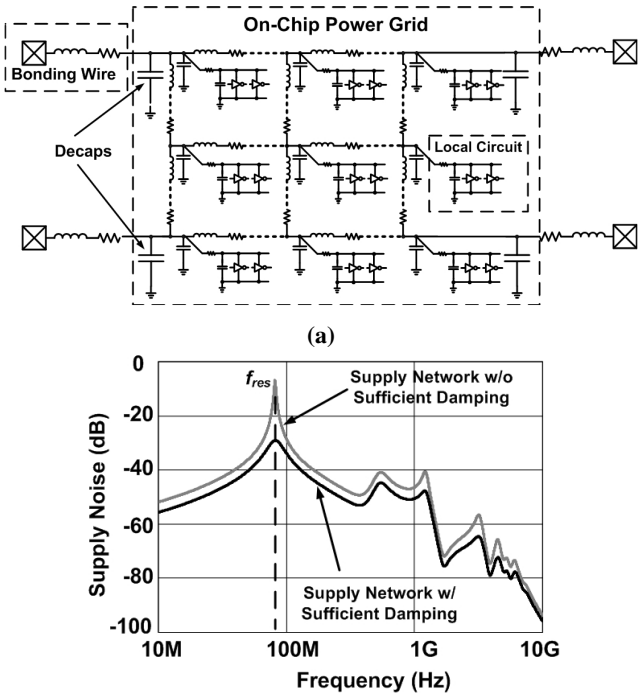

Fig. 1: (a) Model of power supply mesh; (b) Simulated frequency spectrum of supply noise from the model in (a).

Fig. 2(a) shows a simplified supply network model used in this paper. Fig. 2(b) shows the corresponding impedance models including bond wire inductance L, on-chip capacitance C, supply network resistance R_{wire-p}, and circuit resistance $R_{circuit}$. Note that for simplicity of calculation, the series connected wire resistance R_{wire} in Fig. 2(a) can be converted into a parallel resistor using equation $R_{wire-p}=R_{wire} \cdot (1+Q^2)$ where Q is the Q-factor given by $Q = \frac{1}{R_{wire}} \cdot \sqrt{\frac{L}{C}}$. The circuit resistor $R_{circuit}$ comes from the switching and non-switching devices which can have active current I_{on}, subthreshold leakage I_{sub}, or gate leakage I_{gate}. The resistance of each current component is equivalent to the inverse of the slope of the I-V curves in Fig. 2(b) at the nominal operating point. Inspecting the I-V curves of each current component, we find that the leakage current is highly nonlinear to supply voltage. Thus, the equivalent resistance value of leakage current cannot be treated as a constant. Furthermore, the fact that the gate leakage rises most rapidly as supply voltage increases, indicates substantial damping induced by gate leakage. The above observations tell us that the existence of $R_{circuit}$ can no longer be ignored and a correct model of each resistance component will be important for designing efficient on-chip power supply networks.

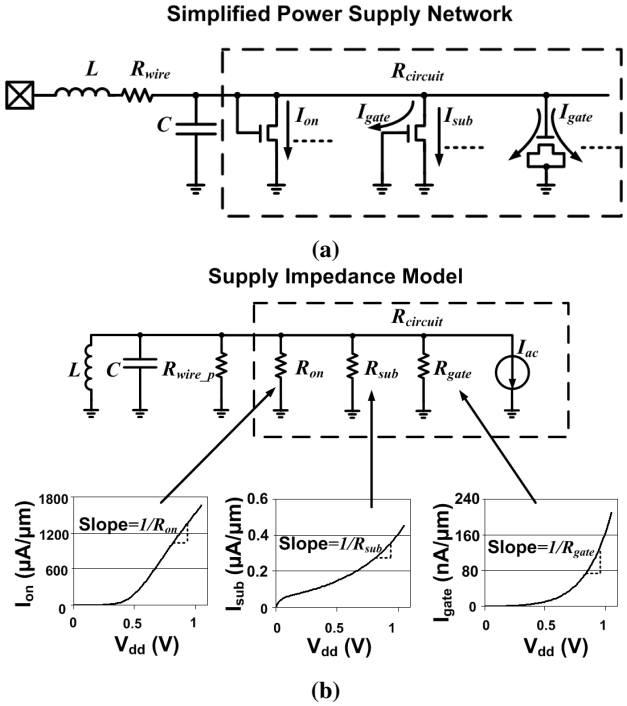

Fig. 2: (a) Simplified power supply model used in this paper; (b) Supply impedance model including the resistance of the circuit itself. Each current component has different damping effects due to the difference in equivalent resistance.

Given the impedance model in Fig. 2(b), the power supply noise at a particular frequency can be calculated as the multiplication of operating current at that frequency and the corresponding supply network impedance. At the resonant frequency, the impedance becomes $R_{wire-p}//R_{circuit}$ since the inductance and capacitance completely cancel each other out. The smaller this resistance is, the more damping is provided and the less supply noise we will have. Because of the small value of R_{wire} (or large corresponding R_{wire-p}), the damping provided from the power network wiring is

not sufficient. This means that additional damping has to be added to suppress the resonant noise. $R_{circuit}$ that comes from the existing circuits can actually provide this additional damping requirement. The goal of this paper is to develop a proper model for $R_{circuit}$ and investigate its variation under different conditions. It is also important to mention that the damping effect provided by R_{wire-p} and $R_{circuit}$ are effective for Ldi/dt noise at all frequencies as shown in Fig. 1(b) rather than for only that at f_{res}. However, since the supply noise is most pronounced at the resonant frequency, we will focus on the damping effect at f_{res} in this paper.

3. MODELING THE DAMPING EFFECT FOR ACTIVE AND LEAKAGE CURRENT

In this section, we discuss the modeling of equivalent resistance and conductance for various on-chip current components, including active current I_{on}, subthreshold leakage I_{sub} and gate leakage I_{gate}. Because supply noise is typically controlled below 15% of V_{dd}, the damping conductance will be calculated based on a small-signal analysis; i.e. the dI/dV_{dd} value will be derived at the nominal V_{dd} point, where I can be one of the following: I_{on}, I_{sub} and I_{gate}. The equivalent damping resistance is then simply the inverse of the calculated conductance.

3.1 Damping Model for Active Current

Active current can be modeled as:

$$\begin{aligned} I_{on} &= \mu_e \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^{\alpha} \\ &\approx \mu_e \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{dd} - (V_{th0} - \lambda V_{dd})) \end{aligned} \tag{1}$$

using the alpha-power law current equation from [13], with $\alpha \approx 1$. In this equation, V_{th0} is the zero-biased threshold voltage, and λ is the Drain Induced Barrier Lowering (DIBL) coefficient. From (1), we can calculate the damping conductance as:

$$\begin{aligned} dI_{on}/dV_{dd} &= \mu_e \cdot C_{ox} \cdot \frac{W}{L} \cdot (1+\lambda) \\ &= \frac{\overline{I_{on}}}{\overline{V_{dd}} - (V_{th0} - \lambda \overline{V_{dd}})} \cdot (1+\lambda) \\ &= \frac{(1+\lambda)}{(1+\lambda)\overline{V_{dd}} - V_{th0}} \cdot \overline{I_{on}} \end{aligned} \tag{2}$$

where $\overline{V_{dd}}$ is the nominal supply voltage and $\overline{I_{on}}$ is the nominal active current at $\overline{V_{dd}}$. A parameter denoted with a bar in this paper refers to the dc bias value, i.e. the operating point for small signal analysis. The V_{gs} (=V_{dd}) term in the current equation and DIBL contributes to the damping conductance. Equation (2) illustrates that the damping conductance of the active current is a constant determined only by its operating points $\overline{V_{dd}}$ and $\overline{I_{on}}$.

3.2 Damping Model for Subthreshold Leakage Current

Subthreshold leakage current can be described as:

$$\begin{aligned} I_{sub} &= \mu_e \cdot C_{ox} \cdot \frac{W}{L} \cdot (\frac{kT}{q})^2 \cdot (m-1) \cdot e^{q(0-V_{th})/mkT} \\ &= \mu_e \cdot C_{ox} \cdot \frac{W}{L} \cdot (\frac{kT}{q})^2 \cdot (m-1) \cdot e^{-q(V_{th0}-\lambda V_{dd})/mkT} \end{aligned} \tag{3}$$

where m is the body effect coefficient and kT/q is the thermal voltage. The derivative of I_{sub} is then calculated to be:

$$\begin{aligned} dI_{sub}/dV_{dd} &= \frac{q\lambda}{mkT} \cdot I_{sub} \\ &\approx \frac{q\lambda}{mkT} \cdot (1 + \frac{q\lambda}{mkT} \cdot \Delta V_{dd}) \cdot \overline{I_{sub}} \end{aligned} \tag{4}$$

where $\overline{I_{sub}}$ is the nominal leakage current at $\overline{V_{dd}}$ and ΔV_{dd} is the power supply noise. The finite damping conductance for subthreshold leakage mainly comes from the DIBL effect. Unlike active current, dI_{sub}/dV_{dd} has to be modeled as a function of supply noise ΔV_{dd} because of the nonlinear exponential relationship between I_{sub} and V_{dd}. The linearization of I_{sub} with respect to ΔV_{dd} in (4) is performed using the Taylor expansion around the nominal supply voltage $\overline{V_{dd}}$. Similar to the case for active current, equation (4) shows that the damping conductance from subthreshold leakage is proportional to the dc leakage current $\overline{I_{sub}}$. However, the damping conductance of subthreshold leakage is a linear function of ΔV_{dd}, so its value changes with supply voltage. This voltage dependent resistance behavior provides additional damping performance.

3.3 Damping Model for Gate Leakage Current

The gate leakage current can be expressed as:

$$I_{gate} = W \cdot L \cdot A \cdot \frac{V_{dd}^2}{T_{ox}^2} \cdot \exp\left(\frac{-B(1-(1-\frac{V_{dd}}{\phi_{ox}})^{3/2})}{\frac{V_{dd}}{T_{ox}}}\right) \tag{5}$$

where T_{ox} is the oxide thickness and ϕ_{ox} is the barrier height for tunneling electrons or holes [14]. A and B are given as:

$$A = \frac{q^3}{16\pi^2 \eta \phi_{ox}} \quad , \quad B = \frac{4\sqrt{2m^*}\phi_{ox}^{3/2}}{3\eta q}.$$

where m^* is the effective mass of tunneling electrons or holes and $\hbar$ is the reduced form of Plank's constant.

By performing a first order Taylor expansion on the derivative of I_{gate} and ignoring higher order terms, we find:

$$dI_{gate}/dV_{dd} = (\frac{2}{\overline{V_{dd}}} + C + (\frac{2}{\overline{V_{dd}}^2} + \frac{4}{\overline{V_{dd}}} \cdot C) \cdot \Delta V_{dd}) \cdot \overline{I_{gate}} \tag{6}$$

where $C = (1 - \sqrt{1 - \frac{\overline{V_{dd}}}{\phi_{ox}}} \cdot (1 + \frac{\overline{V_{dd}}}{2\phi_{ox}})) \cdot \frac{T_{ox} \cdot B}{\overline{V_{dd}}^2}$.

Although (6) requires a more involved calculation, the behavior of damping from gate leakage is similar to subthreshold leakage, in the sense that it is proportional to the dc bias current, and is dependent on the supply noise ΔV_{dd}.

3.4 Damping Effect Comparison for I_{on}, I_{sub}, and I_{gate}

Fig. 3 shows the current and damping conductance of each component (I_{on}, I_{sub}, I_{gate}) as a function of supply voltage. For the

purpose of comparison, results are shown when the three current values are set to be the same at the nominal condition (V_{dd}=0.9V). This figure shows that for an equal amount of current, gate leakage provides a much stronger damping effect than the other two current components. Our derivation models the effective conductance of subthreshold and gate leakage as linear function of V_{dd} as opposed to a constant value derived for the on-current. This is verified in Fig. 3(b) where the damping conductance increases almost linearly with supply voltage for both subthreshold and gate leakage.

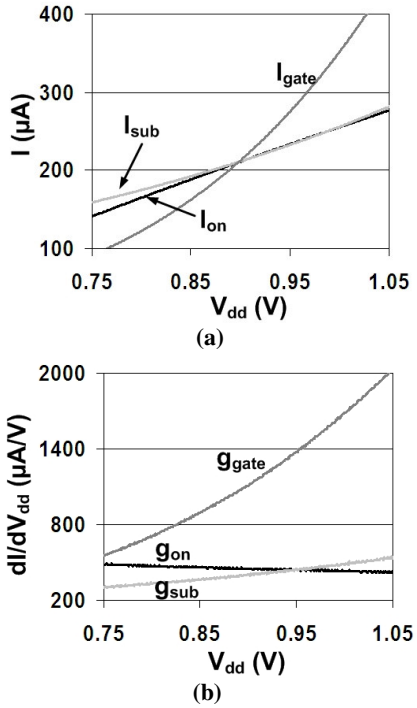

Fig. 3: (a) Simulated I_{on}, I_{sub} and I_{gate} as functions of V_{dd}; (b) Corresponding conductance of each current component.

Table 1 summaries the effective damping conductance for each current component. The coefficients calculated using the developed models are compared with the coefficients obtained from Hspice simulation. Our damping conductance models using physical parameters show a good fit with simulation results, which indicate that the developed model is capable of accurately capturing the behavior of the current induced damping effects. Small discrepancies between our model and the simulation exist due to the following reasons: (a) the α parameter in equation (1) is actually between 1 and 1.2 which leads to a smaller I_{on} conductance value predicted by the model; (b) the parasitic source/drain resistance in MOSFET device accounts for the slight drop on g_{on} in Fig. 3(b) but is not modeled in our simplified current equation; (c) the modeling of gate tunneling leakage for an ultra-thin oxide device involves a more complex mathematical representation and therefore an error exists when using the simple equation in (5) to obtain the solution. However, it is important to realize that the purpose of this modeling is to explore the physical principle of the leakage induced damping effect and to provide a simple closed-form equation for damping estimation. Hence the advantage of this model is that for a given leakage current consumption, the damping resistance can be easily obtained from table 1. For improved accuracy, extensive simulations can be performed at the cost of computation time.

Table 1. Comparison of the current induced damping conductance from derived model and Hspice simulation.

	Derived Model	Hspice Simulation
$g_{on}=1/R_{on}$	$1.80\cdot\overline{I_{on}}$	$2.13\cdot\overline{I_{on}}$
$g_{sub}=1/R_{sub}$	$(1.80+3.24\,\Delta V_{dd})\cdot\overline{I_{sub}}$	$(1.92+3.55\,\Delta V_{dd})\cdot\overline{I_{sub}}$
$g_{gate}=1/R_{gate}$	$(5.51+17.1\,\Delta V_{dd})\cdot\overline{I_{gate}}$	$(5.22+19.6\,\Delta V_{dd})\cdot\overline{I_{gate}}$

Below we evaluate the effect of voltage dependent conductance. At resonant frequency f_{res}, the supply noise is calculated as:

$$\Delta V_{dd} = I_{ac}\cdot R = I_{ac} /(g_0 + A\cdot\Delta V_{dd}) \quad (7)$$

where I_{ac} is the exciting current at frequency f_{res}. g_0 and A are the constant term and linear coefficient in our resistive model in table 1; i.e. $g = g_0 + A\cdot\Delta V_{dd}$. Solving (7), we find the supply noise as:

$$\Delta V_{dd} = \frac{-g_0 + \sqrt{g_0^2 + 4AI_{ac}}}{2A} \quad (8)$$

By using this expression, for a ΔV_{dd} of 0.1V, the voltage dependent term $A\cdot\Delta V_{dd}$ for subthreshold leakage provides an additional 14.5% reduction in power supply noise compared with a constant conductance g_0. Similarly, the voltage dependent term in gate leakage provides an extra 22% reduction in supply noise. In general, a larger A and larger noise amplitude make the voltage dependent resistance more beneficial for supply noise damping.

Fig. 4 shows the simulated transient damping performance at resonant frequency for different current components. Note that for subthreshold leakage test, a small positive gate biased is applied to amplify the subthreshold leakage so that the gate leakage becomes negligible in proportion. The results in Fig.4 are consistent with our resistive model given in table 1. Each current component provides significant damping effect with gate leakage being the strongest.

4. LEAKAGE INDUCED DAMPING EFFECT UNDER PVT VARIATION

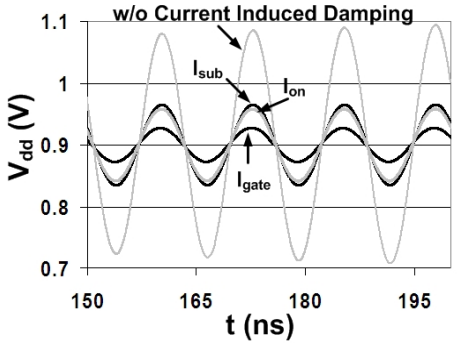

Fig. 4: Supply resonant noise damped by different current components. Gate leakage provides largest damping effect for the same amount of current.

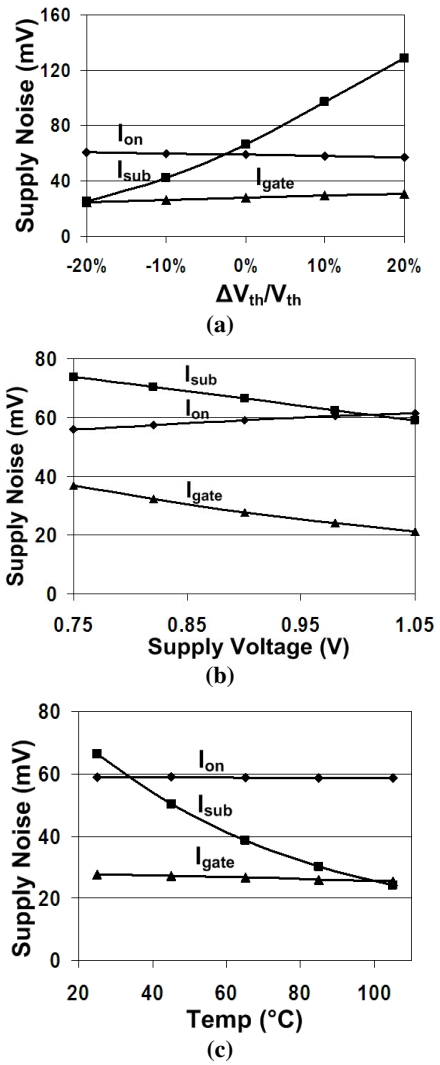

Fig. 5: Simulated damping effects under PVT variation. (a) Threshold voltage variation; (b) Supply voltage variation; (c) Temperature variation. Note that larger damping effect leads to smaller supply noise.

PVT variation has become an increasingly critical issue in deeply scaled LSI circuits. Due to the fact that different leakage components have different behaviors under PVT variation, it is necessary to evaluate the leakage induced damping effects under various operating conditions.

Fig. 5 compares the resonant supply noise for each damping current component while varying the PVT parameters. As before, all current components have equal current amplitude at the nominal condition (V_{th} at typical corner, 0.9V supply voltage, and room temperature). Fig. 5(a) shows the impact of threshold voltage variation on damping effects of each current component. The figure shows that the damping effect of subthreshold leakage varies the most under V_{th} variation because of its exponential dependency. This observation indicates that transistors in a fast corner die (lower V_{th}) will introduce a larger damping effect, which in turn can compensate for the increased *IR* and *Ldi/dt* droop due to larger transient currents. Fig. 5(b) shows the impact of supply voltage variations on damping effects. Both subthreshold leakage and gate leakage show an increased damping performance as V_{dd} rises while damping from active current is slightly reduced. This observation is consistent with Fig. 3(b) and can be explained by the models developed in the previous section. Fig. 5(c) shows the temperature dependency of the damping effects from each current component. With the increase in temperature, the damping from subthreshold leakage increases dramatically, resulting in a significantly reduced noise level as seen in the figure. By inspecting the subthreshold damping model in equation (4), we find that the damping coefficient actually decreases with temperature. However, the dc leakage current $\overline{I_{sub}}$ increases exponentially with temperature, and therefore the overall damping performance by subthreshold leakage increases. This positive temperature dependency can potentially compensate the slow-down of circuits at high temperatures.

Fig. 6 shows the comparison of transient noise waveforms at 25°C and 110°C. We used an ISCAS85 benchmark circuit (C3540, 8-bit ALU) clocked at 640MHz for generating the supply noise. Six additional circuit blocks of the same kind are placed in idle mode to provide the subthreshold and gate leakage. To excite the resonant noise at 80MHz (=640MHz/8), a large capacitive load is driven by a divided clock that is 8 times slower than the system clock. Fig. 6 confirms the increased damping effect at a higher temperature due to the increase in subthreshold leakage as explained in Fig. 5(c).

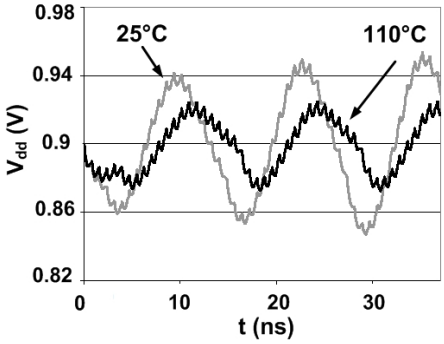

Fig. 6: Simulated noise waveforms at 25°C and 110°C for ISCAS benchmark circuits.

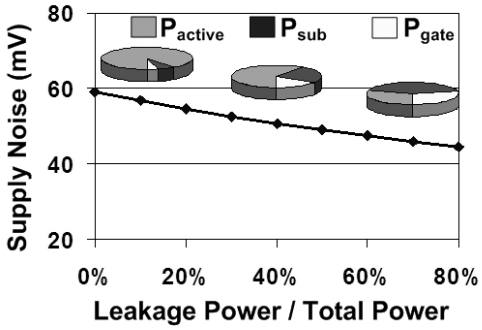

Fig. 7: Resonant supply noise versus leakage power ratio.

The overall damping effect in a realistic VLSI system depends on the ratio between leakage power and active power. For the same current amplitude, leakage currents have larger damping coefficients than active current as shown in table 1. Fig. 7 displays how the resonant supply noise changes when varying the leakage versus active current ratio. For simplicity, we assumed a

fixed ratio (60%:40%) between the subthreshold and gate leakage. The figure shows increased damping and less supply noise in leakier chips. For example, a chip with 70% leakage power has 19% less resonant noise compared to a chip with 10% leakage power, due to the leakage induced damping effect.

5. DESIGN CONSIDERATIONS WITH LEAKAGE INDUCED DAMPING EFFECT

The phenomenon of leakage induced damping has normally been ignored or unnoticed in previous IC designs. However, as leakage becomes the dominant component of total power dissipation, this effect can no longer be ignored. In fact, since leakage induced damping helps to suppress the power supply noise, a design which does not consider this phenomenon can be too pessimistic. The issues associated with leakage induced damping effects include (1) design of power grid with proper resistive damping (2) decap assignment. The first issue is obvious because considering the damping effect discussed in this paper can alleviate the amount of effort of putting sufficient damping in power grid. Leakage induced damping effect also plays an important role in decap assignment. Detailed discussion with an example is given below.

In order to meet the supply noise constraints, the most common solution was to add more on-chip decaps [5]. Adding decaps is inefficient because one has to pay a huge amount of area overhead to bring down the Q factor of the RLC network which is given as $Q = \frac{1}{R} \cdot \sqrt{\frac{L}{C}}$. This is especially the case when the supply network resistance R is small. Fig. 8 shows simulation results on a medium-scale circuit with the parameters given in table 2. Decap of the original circuit is approximately 80nF causing the resonant supply noise to reach 15% of the nominal supply voltage. However, to meet a supply noise target of 8%, an additional 80nF of decap has to be added if the leakage induced damping effect is not considered. Our simulation results show that when leakage induced damping is considered, only 55nF of decap needs to be added, which results in a total decap saving of 15.6%.

Table 2. Simulation parameters for decaps assignments.

Technology	32nm CMOS	**# of min. sized transistors**	8.4M
P_{total}	0.4W	I_{sub}	120mA
I_{gate}	80mA	f_{res}	80MHz
R_{wire}	2mΩ	L	0.1nH
Decap w/o Leak. Damp.	160nF	Decap w/ Leak. Damp.	135nF

6. CONCLUSIONS

Leakage in modern VLSI circuits is becoming comparable to active power. A fact that has generally gone unnoticed is that on-chip leakage current can provide damping for power supply noise, especially resonant noise, which can severely degrade the circuit performance once excited. This paper studies the phenomenon of leakage induced damping in low voltage ICs where leakage and noise are the two most important design constraints. Models for the damping effect induced by the on-chip active current, subthreshold leakage, and gate leakage are developed and verified with Hspice simulations in a 32nm CMOS technology. The impact of PVT variations on damping effect was also investigated to gain a better understanding of the damping behavior. Simulation shows that under normal conditions gate leakage provides more damping than the other two components. Damping effect of subthreshold leakage varies the most with PVT variations, and can compensate for the performance loss at high temperatures and high transient noise situations. Finally, the associated design issues are discussed. By considering the leakage induced damping effect, decap saving of 15.6% can be achieved which prevents over-design of power supply networks.

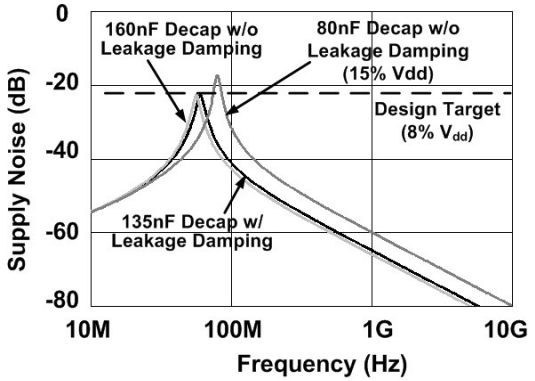

Fig. 8: Frequency diagram of supply noise w/ and w/o considering the leakage damping effects for decap assignment.

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