A High-Speed Variation-Tolerant Sub-Threshold Interconnect Technique Using Capacitive Boosting

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Presentation Agenda

- Global Interconnect in Sub-threshold
- Proposed Sub-threshold Interconnect Technique
- Application on Sub-threshold Clocking
- Performance and Power Results
- Test Chip Measurements
- Conclusions
Subthreshold Operation

- **Main Benefit**
  - Super-linear power savings
  
  \[ P_{\text{total}} = \alpha \cdot f \cdot C \cdot V_{dd}^2 + I_{\text{leak}} \cdot V_{dd} \]
  
  - Minimum energy solution for low-performance designs

- **Limitations**
  - PVT variation
  - Interconnect delay
  - Lack of a systematic design methodology
Global interconnect delay dictates system performance

Multiple clock cycles required for global signals to propagate across die
Interconnect Delay in Sub-threshold

- Global interconnect problem worsens in sub-threshold
  - Device resistance dominates over wire resistance
  - Wire capacitance is constant while MOS capacitance reduces at lower voltages
Proposed Sub-threshold Interconnect Technique

Operating region is shifted from sub-threshold to super-threshold

Charge pump circuitry to boost the gate voltage of drivers

100X+ increase in drive current at the expense of leakage current
Circuit Operation: Active Mode

Vdd=0.4V

Preset Signal Generator (N-driver)

Preset Signal Generator (P-driver)

*Output holders not shown

NMOS boosted

V_{IN} 0.4V 0V 0.4V

C_{1} 0.8V 0.4V 0V

C_{2} 0V -0.4V

V_{OUT} 0.4V 0V 0V

0.8V

-0.4V

0V
Circuit Operation: Active Mode
Circuit Operation: Standby Mode

- Half cycle start-up time
- No start-up required for inactive periods up to 200 cycles (@ 0.4V, 4MHz, 20°C)
- Level holders can be used for restoring output level
Boosting Capacitance in Sub-threshold

Gate capacitance

Capacitance changes

Below Vt

Source

Drain

depletion width

N well

Operates in weak inversion region

Strong inversion

Moderate

Sub-threshold Operating region

Accumulation

Depletion

\[ C_{gate} \]

\[ Vgs \]

\[ -Vt \]
Boosting Efficiency

\[ \Delta V_B = \frac{C_{\text{boost}}}{C_{\text{boost}} + C_{\text{node}}} \times \Delta V_A \]

**Pull-up:**
- Boosting cap: \( C_2 \)
- Node cap: \( P_5, N_4, N_3 \) and \( P_1 \)

**Pull-down:**
- Boosting cap: \( C_1 \)
- Node cap: \( N_5, P_4, P_3 \) and \( N_2 \)

**Boosting efficiency**
\[ = (\Delta V_B / \Delta V_A) \times 100 \]

<table>
<thead>
<tr>
<th>( V_{\text{cap}} ) (V)</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>65%</td>
</tr>
<tr>
<td>0.3</td>
<td>59%</td>
</tr>
<tr>
<td>0.4</td>
<td>70%</td>
</tr>
<tr>
<td>0.5</td>
<td>89%</td>
</tr>
<tr>
<td>0.6</td>
<td>90%</td>
</tr>
</tbody>
</table>

\( V_{\text{cap}} \): voltage across MOS cap.
Operating Waveforms

- 2.6X delay improvement for 1pF load
Delay and Power Consumption

- 2X+ delay improvement for different interconnect loads
- Comparable power consumption once the frequencies are high enough that active and short circuit power dominate over leakage current
Sensitivity to Variation

- Delay variation reduced by 2X under supply (0.4V ± 5%) and temperature (20~80°C) variations
- The driver transistors are no longer in the sub-threshold region
Sub-threshold Clocking

Four clock buffer stages with each buffer driving four clock buffers and the long interconnects

Clock signal paths are symmetrically routed across the chip for minimum skew

D. Harris, TVLSI 2001
Clock Skew Comparison

0.18μm, 20°C, 0.4V(±5%), Vth(±5%)

- **This work**
- **Conventional**

- **Proposed driver**
  - Average delay: 52ns
  - Standard deviation: 5.2ns

- **Conventional driver**
  - Average delay: 251ns
  - Standard deviation: 30.7ns

- **8.3X reduction in 3σ clock skew and 22% reduction in σ/μ using the proposed driver**
The number of transistors per driver increased from 4 to 18 leading to 30% area overhead.

40% of the driver area is occupied by boosting capacitors.
Test Chip Schematic

Level-down converter: NMOS transistor is employed to pull down node A1

Level-up converter: PMOS transistors (P7 and P8) used to reduce the contention
Performance Measurements

Supply voltage:
- core (0.4V)
- level converter (1.0V)
- IO buffer (1.8V)

Rise (fall) delay improved by 2.6X (2.9X)
Proposed boosting technique is efficient in reducing the PVT impact at lower supply voltages.
Variability and Power Measurements

- Temperature sensitivity reduced from 1.6X to 0.7X
- Proposed driver operated with 41% less power dissipation at 4MHz or 49% higher performance at 5.1µW
Conclusions

• Global interconnects in sub-threshold region suffer from increased delay and large sensitivity to PVT variations

• Proposed capacitive boosting technique
  – Effective for high activity long line drivers
  – 70% boosting efficiency at 0.4V

• Measurements from a 0.18µm test chip show
  – 1.7-2.9X delay improvement
  – 2.3X reduced delay variability at 0.4V
  – 41% power saving at 4MHz
  – 49% performance improvement at 5.1µW