Studying the Impact of Temperature Gradient on Electromigration Lifetime Using a Power Grid Test Structure with On-Chip Heaters

Yong Hyeon Yi and Chris Kim
Department of Electrical and Computer Engineering
University of Minnesota
Minneapolis, USA
phone: +1-(651)-353-2181, email: yi000055@umn.edu

Chen Zhou
Nvidia
Santa Clara, CA, USA

Armen Kteyan
Siemens EDA
Yerevan, Armenia

Valeriy Sukharev
Siemens EDA
Santa Clara, CA, USA

***Abstract*—This work presents statistical data collected from 38 power grid test structures showing the detailed impact of temperature gradient on electromigration (EM) lifetime. The failure time, order, and location under different temperature gradients were compared to show that unexpected early EM failures can occur at temperature gradient regions due to accelerated tensile stress evolution inside the wire.**

Keywords—Electromigration, power grid, on-chip heater, temperature gradient, reliability, void, TTF

I. INTRODUCTION

Electromigration (EM) in power grids is a critical reliability concern due to the short DC stress lifetime and excessive IR drop caused by EM voids which may lead to circuit timing failures. While state-of-art electronic design automation (EDA) tools are currently being developed to more accurately predict EM lifetime of power grids, only limited silicon data is available to verify the accuracy of the power grid EM models and simulation tools. As part of the extensive EM silicon data collection, previous works have shown on-chip heater based AC [1][2] and DC [3] EM lifetime characterization results, as well as signal behaviors in damaged circuit interconnects [4][5]. However, such EM test structures are limited to metal wire segments rather than power-grid-like mesh structures with multiple redundant current paths. Several other works presented voltage evolution at various locations in a power grid, which helped reveal the true nature of EM voids in a complex mesh structure with redundant/alternative current paths [6-8]. These efforts have helped build confidence in the EM models as well as our collective understanding on EM, and will facilitate the adoption of new EM tools by the semiconductor industry [9]. However, a critical shortcoming of these works is that most EM data were collected under a spatially uniform (or close to uniform) stress temperature, which is not representative of a real power grid. Instead, a real power grid is exposed to thermal hot spots and local Joule heating effects as shown in the thermal gradient profile in Fig. 1 [10]. Such non-uniform temperature accelerates a void formation in metal wires due to the faster tensile stress growth resulting from larger atomic flux divergence [11] (Fig. 2). In this work, we carried out the first-of-its-kind experiments to study the impact of local temperature gradient on the power grid EM lifetime.

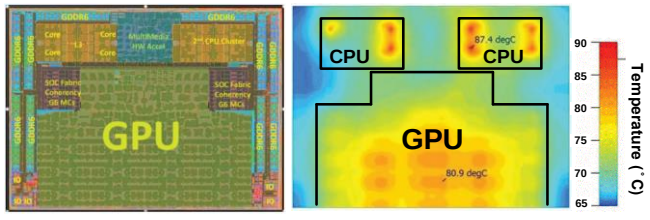


Fig. 1. Thermal gradient profile of a 7nm System on Chip (SoC) [10].

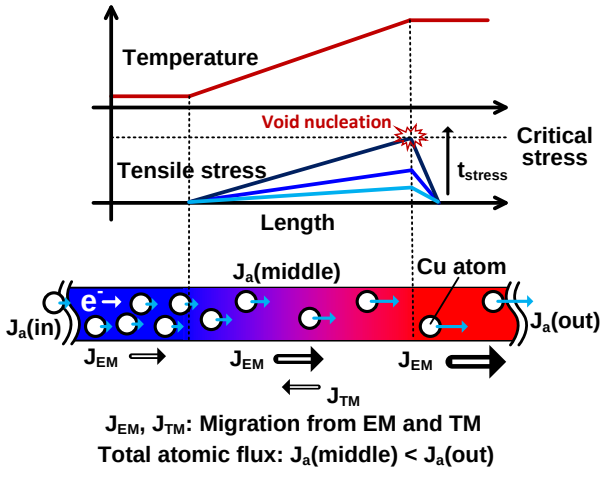


Fig. 2. Tensile stress grows faster when a temperature gradient is present in a metal wire, due to the presence of larger atomic flux divergence.

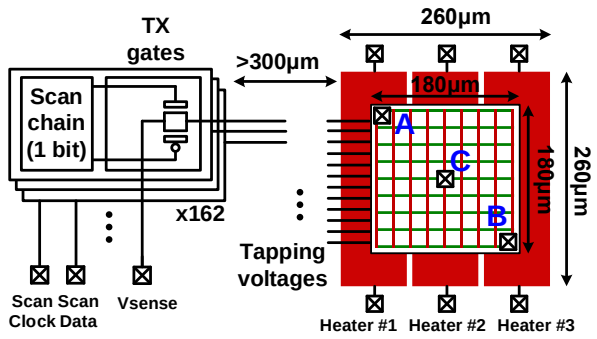


Fig. 3. EM test vehicle for studying temperature gradient effects within a chip which includes a 9x9 metal grid DUT, three poly heaters, and a 162:1 multiplexer for tapping out local voltages [7].

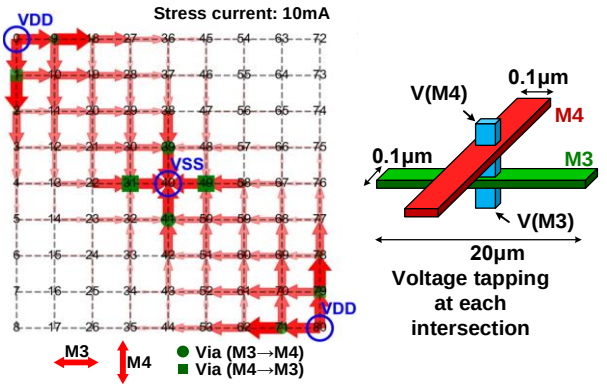


Fig. 4. (Left) Measured voltage drop of a fresh chip. The size of the arrows and dots denote voltage drops in the wires and vias. (Right) Each cross section has top and bottom tapping nodes.

The test vehicle comprises a custom-designed 9x9 M3-M4 power grid mesh, three integrated heaters, and a voltage tapping scheme capable of measuring the voltage at each intersection of the 2D mesh. The temperature gradient, along with the stress temperature needed for accelerating EM, was applied by individually controlling the power of the three integrated heaters. The average temperatures of the three heaters and the power grid were monitored using the temperature coefficient of the resistance (TCR) method. The time to failure (TTF) distributions were collected under three test modes to understand the impact of temperature gradient on the failure location, failure order, and failure type. To our knowledge, this paper presents the first experimental evidence of temperature gradient induced EM failures in a power grid like test structure.

II. Test Chip Description

The basic overview of the EM monitoring test vehicle is shown in Fig. 3 [7]. The design under test (DUT) is a metal mesh structure composed of horizontal M3 and vertical M4 layers. The width of the wires is 0.1µm (minimum), where the length of each branch segment is 20µm (Fig. 4 (right)). The cross-sections of the metals are connected by single M3 to M4 vias. Each cross-section has two voltage tapping nodes above

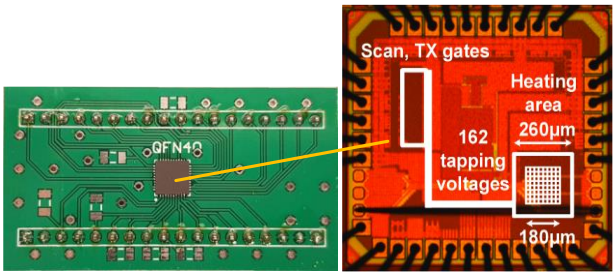


Fig. 5. Test board and die photo

and below the via that enable direct voltage measurement. The 9x9 grid has 162 tapping points in total, and the internal nodes are connected to the IO device-based voltage scanning circuit. The scanning circuit is far away from the heating area (>300µm) to minimize the leakage current that may degrade the measurement accuracy. The three on-chip heaters are located beneath the DUT to raise the die temperature beyond 350˚C. The silicided poly heaters are separately controlled, enabling a configuration of different temperature gradient conditions. For example, if the three heaters have the same temperature, the lateral thermal distribution is almost uniform, whereas operating only the side heaters (heater #1, #3) forces the thermal gradient between the side and the middle area of the DUT. Fig. 4 (left) is the voltage drop map of the fresh chip after a 10mA stress current is applied. The magnitude of the arrow on the segments and the dots on the vias denotes the relative voltage drop throughout the mesh. This profile mimics a current distribution scenario of power grids in an IC block that contains complicated branches with numerous redundant paths. Since the temperature distribution throughout the die is highly affected by the heat sinking capability, PCBs (Fig. 5 (left)) from two separate vendors were ordered to measure any difference in the failure trend.

III. Experiment Methodology

A. Temperature Control

EM testing under various temperature gradient conditions requires accurate control and temperature tracking of the individual heaters. Due to this requirement, the TCR of the three heaters and the power grid DUT are characterized prior to the experiment. The TCRs of the heaters (left) and the DUTs (right) in Fig. 6 confirm an R^2 value of 0.9999 or higher. We measured the temperatures of DUTs and heaters based on the linear TCR extrapolation, which allows the local temperature to be estimated by measuring the resistance values. Fig. 7 shows the DUT and heater temperatures

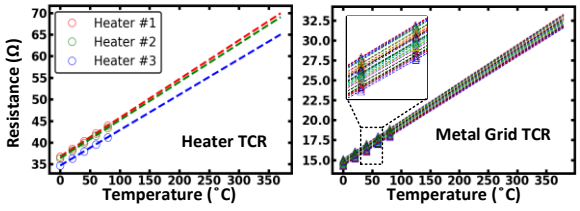
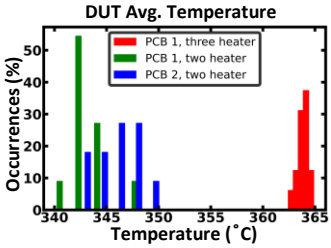


Fig. 6. (Left) TCR of three on-chip heaters measured from the same chip. (Right) TCR of all 38 tested DUTs used for extracting the average DUT temperature.



Heater Temperature

Test mode	Heater #1	Heater #2	Heater #3
PCB vendor #1 Three heater (16 chips)	350.8˚C	350.7˚C	350.7˚C
PCB vendor #1 Two heater (11 chips)	350.8˚C	323.1˚C	350.7˚C
PCB vendor #2 Two heater (11 chips)	350.2˚C	332.3˚C	349.9˚C

Fig. 7. (Left) Histogram of DUT temperatures for the 38 chips measured in this work. (Right) Average heater temperatures for each test mode measured from 38 test chips.

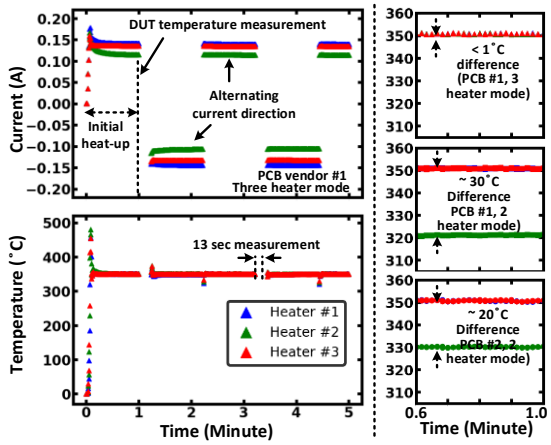


Fig. 8. (Upper left) Heater current control for the three heater mode. (Lower left) Heater temperatures for the three heater mode. (Right) Heater temperatures for the different modes

recorded before the stress for the three test modes. The temperature difference between the side heaters and the middle heater is 0˚C, 30˚C, and 20˚C, respectively, for the three test modes. The number of chips tested for each mode is 16, 11, and 11, respectively. The two heater modes represent a realistic chip operating scenario where thermal distributions are nonuniform due to the local hotspots. Also, the histogram of the DUT temperature is presented in Fig. 7 (left), which shows the average and variation of the DUT temperature for the three different modes.

Note that the measured temperatures of the DUTs (> 360˚C) are higher than that of the heaters (350˚C) for the uniform temperature mode. We suspect this error comes from nonlinearity of the heater TCRs at the high temperature region. Due to the combined resistivity of the p+ polysilicon (negative TCR) and the silicide (positive TCR) in the heaters, a perfect linearity of the silicided poly heater cannot be guaranteed at extreme temperatures. Such deviation from the linear trend can underestimate the die temperature, which explains the higher DUT temperatures in the histogram.

The die temperature is configured by applying high currents to each heater. As illustrated in Fig. 8, a software-based automated control loop was developed to reach the target temperature during the initial heat-up phase. After that, the metal grid temperature is measured, and the current direction is periodically toggled to prevent EM in the heaters

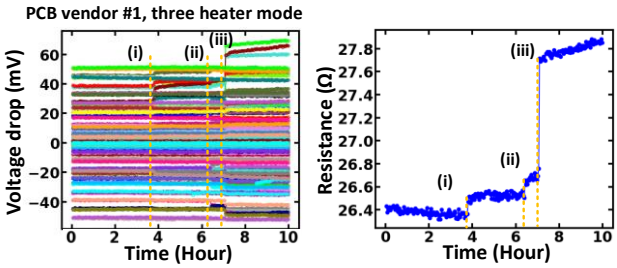


Fig. 9. Experimental results from a chip with median TTF lifetime. (Left) 192 voltage traces and (Right) DUT resistance versus stress time.

themselves. Thanks to the accurate heater control capability, three different temperature gradient conditions were attained, as displayed in Fig. 8 (right).

B. EM Failure Measurement

After the temperature become stabilized a 10mA EM stress current was applied to the metal grid. At the same time, 162 voltages of the internal tapping nodes are recorded every 2 minutes. When a voltage shift greater than 10% is detected, the time and location of the EM failures are recorded for data analysis. For example, as shown in Fig. 9, once a void formation inside the grid results in changing of the voltage drop profile, the first (i), second (ii), and third (iii) time-to-failures (TTF) and the node numbers with maximum abrupt shifts are recorded.

IV. EM Failure Results and Discussions

A. Time to Failure Statistics

Fig. 10 compares the cumulative TTF plots of the 1st to 4th failure for each test mode. In the 1st failure trend, the uniform temperature condition is close to the typical lognormal

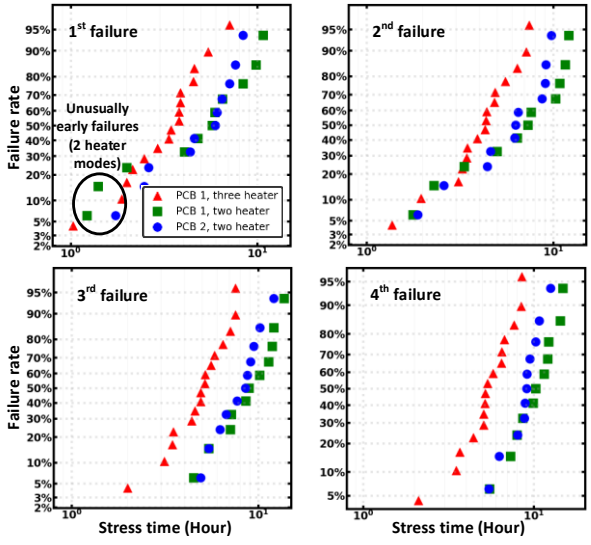


Fig. 10. Time to failure distributions for first, second, third, and fourth failures of each test condition. The two heater mode in green shows a bimodal behavior owing to the temperature gradient. For subsequent failures, the distributions revert to the standard lognormal shapes.

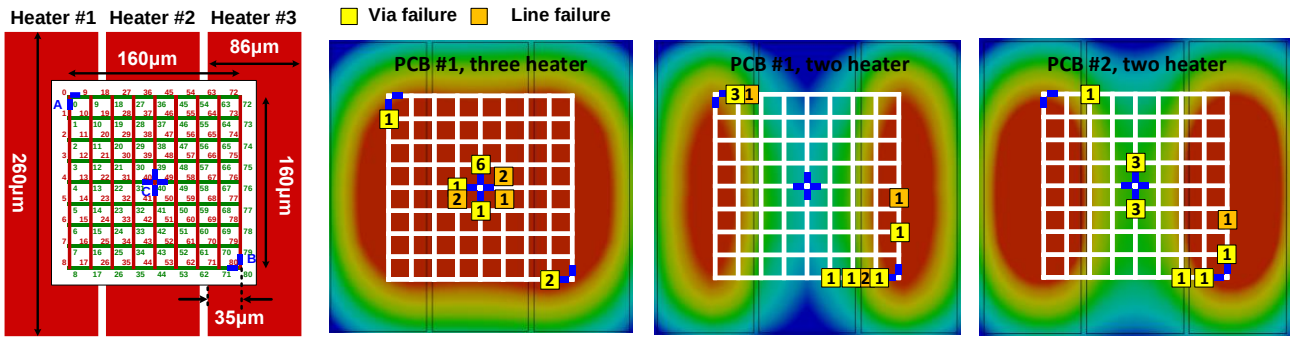


Fig. 11. (Left) On-chip heater and power grid layout and dimensions, drawn to scale. (Right) Location and occurrences of the first EM failures for each test condition. Early failures can be seen in the right figures along the bottom horizontal wire where the temperature gradient is the highest.

distribution, while the other nonuniform modes have bimodal distributions. Furthermore, a comparison between the three heater (red) and the two heater cases (green and blue) suggests that a larger thermal gradient is likely to be responsible for the unusually early failures, as experimented in [12]. Note that the TTF trends return to the typical lognormal distribution by the 3rd and 4th failure. We suspect this is due to the stress currents being redirected away from the earlier failure locations, which may have occurred in the temperature gradient regions.

B. Failure Locations

Fig. 11 shows the first failure locations of all 38 chips for each test condition, overlayed with temperature maps of each experiment mode. The layout of the power grid and voltage tapping node numbers are illustrated in Fig. 11 (left). The temperature gradient nearby the boundaries of the three heater strips (e.g., node 62 and 15 in Fig. 11) is highest with the middle heater turned off. This thermal gradient explains the different failure location trends in Fig. 11. For the uniform temperature case (Fig. 11 (PCB #1, three heater)), EM events are concentrated near the center due to the high current density (Fig. 4 (left)). However, as shown in Fig. 11 (PCB #1, two heater), even both the uniform and the gradient experiments show similar current density profiles, failures occur not only in the high temperature or current density regions but also at locations with a high thermal gradient. The voltage drop and failure analysis of the bottom branch of the grid in Fig. 12 show the clear impact of the gradient. Even though the voltage drops are drastically reduced from node 71 to the inner nodes (node 62, 53), the two heater mode's first failures occur in vias and wires with less current densities. This suggests that the temperature gradient accelerates the growth of tensile stress resulting in faster void formation.

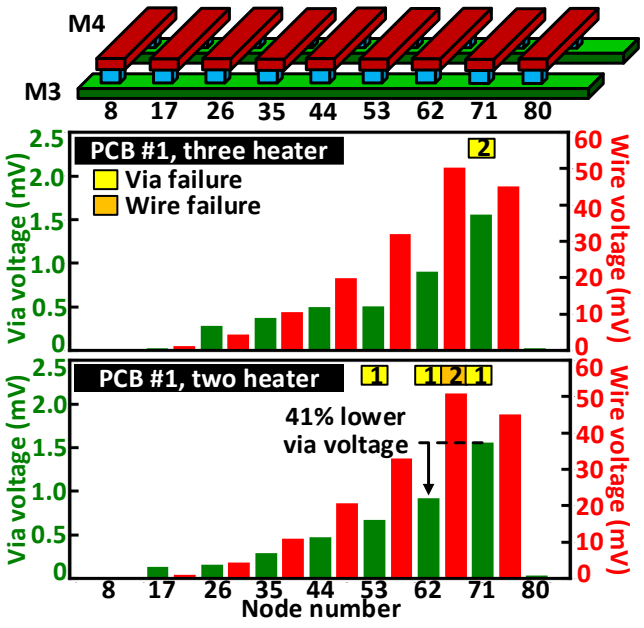


Fig. 12. Failure location anlaysis on the bottom branch of the grids. Comparison between three (uniform temperature) and two heater (with temperature gradient) modes in terms of via/wire voltage drops is shown with number and location of first failures. The two heater mode has EM failures near the heater boundary region even with weaker voltage stresses.

V. Conclusion

This work presents EM failure time and location statistics to show the impact of a temperature gradient on void forming trends in the metal grid structure. The three different experiments show that the failure locations change, and the void nucleation is boosted with the increase of the temperature difference. The results imply that the thermal difference formed by local hotspots cannot be ignored in terms of power grid EM lifetime.

Acknowledgment

This work was supported in part by Semiconductor Research Corporation (SRC) through the Texas Analog Center of Excellence (TxACE).

References

[1] C. Zhou, X. Wang, R. Fung, et al., "A Circuit based Approach for Characterizing High Frequency Electromigration Effects," *IEEE Trans. on Device and Materials Reliability (TDMR)*, 2018.

[2] C. Zhou, X. Wang, R. Fung, S. Wen, et al., "High Frequency AC Electromigration Lifetime Measurements from a 32nm Test Chip", *IEEE Symposium on VLSI Technology*, Jun. 2015.

[3] N. Pande, C. Zhou, MH Lin, et al., "Characterizing Electromigration Effects in a 16nm FinFET Process Using a Circuit Based Test Vehicle", *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019.

[4] N. Pande, C. Zhou, MH Lin, et al., "A 16nm All-digital Hardware Monitor for Evaluating Electromigration effects in Signal Interconnects through Bit-Error-Rate Tracking", *IEEE Trans. on Device and Materials Reliability (TDMR)*, 2022.

[5] N. Pande, C. Zhou, M.H. Lin, et al., “Electromigration-Induced Bit-Error-Rate Degradation of Interconnect Signal Paths Characterized from a 16nm Test Chip”, *IEEE Synposium on VLSI Technology*, 2021.

[6] B. Li, A. Kim, P. McLaughlin, et al., “Electromigration characteristics of power grid like structures”, *IEEE International Reliability Physics Symposium (IRPS)*, March 2018.

[7] C. Zhou, R. Wong. S Wen, et al., “Electromigration Effects in Power Grids Characterized Using an On-Chip Test Structure with Poly Heaters and Voltage Tapping Points”, *IEEE Symposium on VLSI Technology*, June 2018.

[8] C. Zhou, R. Fung, S. Wen, et al., "Electromigration Effects in Power Grids Characterized from a 65 nm Test Chip", *IEEE Trans. On Device and Materials Reliabiltiy (TDMR)*, 2019.

[9] V. Sukharev, A. Kteyan, F. Najm, et al., “Experimental Validation of a Novel Methodology for Electromigration Assessment in On-chip Power Grids”, *IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems*, December 2021.

[10] P. Paternoster, A. Maki, A. Hernandez, et al., “XBOX Series X: A Next-Generation Gaming Console SoC”, *IEEE International Solid-State Circuits (ISSCC)*, February 2021.

[11] A. Kteyan, V. Sukharev, Y, Yi, et al., “Novel methodology for temperature-aware electromigration assessment in on-chip power grid: simulations and experimental validation”, *IEEE International Reliability Physics Symposium (IRPS)*, 2022.

[12] H.V. Nguyen, C. Salm, B. Krabbenborg, et al., “Effect of thermal gradients on the electromigrationi life-time in power electronics”, *IEEE International Reliability Physics Symposium (IRPS)*, April 2004.