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A 16nm All-digital Hardware Monitor for Evaluating Electromigration effects in Signal Interconnects through Bit-Error-Rate Tracking

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Abstract—**The impact of Electromigration (EM) on the Bit-Error-Rate (BER) of signal interconnect paths was experimentally examined. An array-based test-vehicle for tracking Bit-Error-Rate (BER) degradation of signal interconnects subject to Direct-Current (DC) EM stress was implemented in a 16nm FinFET process. A unit interconnect path comprises five identical interconnect stages where each wire is driven by inverter based buffers. Accelerated EM stress testing is achieved entirely on-chip using metal heaters located directly above the devices-under-test (DUTs) and separate stress circuits driving both ends of the wire. The proposed test structure features a ring-based Voltage-Controlled-Oscillator (VCO), a bit-pattern generator and local BER sampling monitors which enable bitwise tracking of '0' and '1' errors separately, further simplifying the overall test-setup and allowing for high precision characterization of EM induced resistance shifts using only digital circuits. Measurement data collected from the 16nm prototype reveals unique insights into EM induced signal path degradation that was not available prior to this work. Our experimental studies suggest that monitoring the BER of an interconnect path could be used as a new metric for capturing EM induced resistance shifts in a real system, in lieu of the conventional approach which focuses on monitoring standalone wire resistances. Supplemental simulations showcasing the projected degradation in the interconnect path operating frequency as a function of stress time constructed from resistance traces sampled from identical wires implemented in the same process reaffirm the measurement trends.**

Index Terms—**All-Digital, Array-based, Bit-Error-Rate, Circuit reliability, Datapath, Digital-Intensive, Electromigration, FinFETs, Median-Time-To-Failure, Signal-Interconnects.**

I. Introduction

Continuous innovations at the device and process fronts have allowed CMOS feature sizes to progressively scale over the years, witnessing the foreseen benefits of power, performance and area in the manufactured hardware every generation. However, the resulting miniaturization of dimensions coupled with the change in transistor structure from planar to FinFET and then to gate-all-around FET has also presented the semiconductor industry with additional reliability

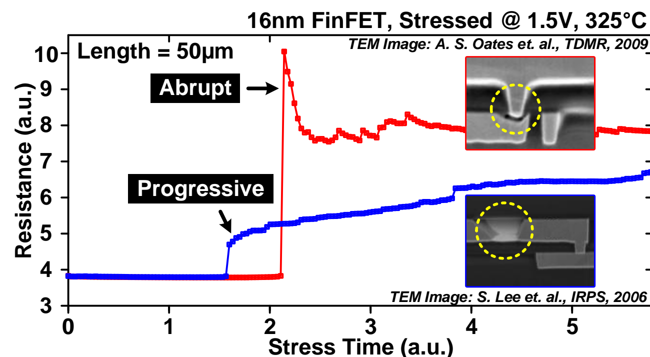

Fig. 1. Experimentally obtained wire resistance traces from a circuit based characterization-vehicle implemented in a 16nm technology node [7], illustrating 'abrupt' and 'progressive' EM induced resistance shifts for identical wire types, as a function of the stress duration. Depending upon the wire geometry and the metal stack specifics, one or the other of the failure modes may dominate, leading to void formations either in the via or in the wire segment itself.

challenges. The increase in on-chip current densities in conjunction with issues unique to FinFET such as self-heating effects (SHE) [1-2], further degrading every upcoming process generation [3], are pressing concerns in particular for the Back-End-Of-Line (BEOL) metallization processes, making interconnect reliability and hence electromigration (EM), a crucial concern in today's emerging ultra-scaled technology nodes [4-6].

EM is the displacement of material forming the interconnect (essentially Copper, in contemporary Cu/low-k dual damascene processes [8]), as a consequence of the momentum imparted to the metal atoms by electrons moving under the influence of an applied electric field, forming the current flow through the conductor. The associated material depletion results in distinct void geometries (Fig. 1), which may either lead to an abrupt or a gradual change in the conductor resistance overtime. Abrupt failures, wherein the resistance instantaneously jumps to a value typically several times that of the original, are associated with void formations directly underneath the via, also referred to as

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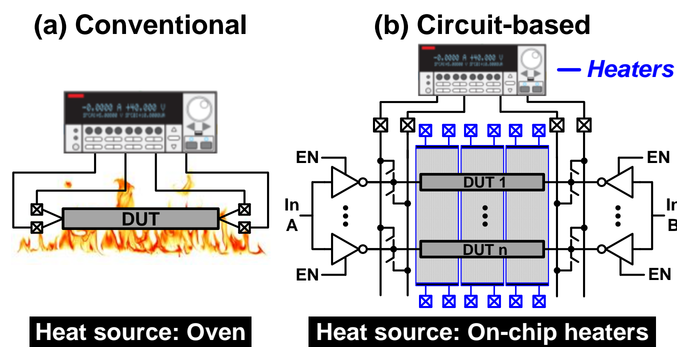

Fig. 2. (a) Traditional and (b) Circuit-based approaches for characterizing EM effects. The on-chip approach not only simplifies the overall test-setup by eliminating the need of cumbersome oven-based setups used conventionally, but also allows detailed high-frequency characterization of the failure characteristics which would otherwise be impossible using conventional device probing. Additionally, stressing the DUTs in parallel as well as periodically monitoring their resistances requires only a few shared pads in total, thereby also improving the overall area efficiency.

'slit-voids' [9], whereas progressive failures are the ones wherein the resistance first jumps to around 0.5X or so typically (depending upon the process specifics), followed by monotonic increases over the stress duration. This is a consequence of the voids nucleating within the metal line, which continue to grow under the influence of applied stress. Such voids have also been referred to as 'trench-voids' in the literature [10]. Regardless of whether the shift in the conductor resistance is abrupt or progressive, EM lifetime is a strong function of the stress temperature, the stress current density, direction in which the stress is applied, as well as the material properties and the geometry of the interconnect, governing the mechanical stresses operating within. Black's empirical formulation [11], expressing the interconnect reliability as a function of various stress factors, outlines a strong exponential relationship between the interconnect Mean-Time-To-Failure (MTTF) and its stress temperature, and a linear to square relationship, depending upon an empirical constant, to its stress current density. For VLSI circuits, EM may manifest as an increased parasitic (R-C) delay for signal interconnections or may translate to a reduced operating voltage for circuit blocks across a power grid.

Conventionally, EM effects have been characterized by monitoring the resistances of individual wires under stress using a probe station based setup. However, since EM lifetime is a stronger function of temperature as compared to stress voltage or current, for accelerated stress testing the temperature must be raised to 300°C or beyond using an extensive oven-based setup. Moreover, to avoid statistical artifacts, EM data must be collected from a large sample population of Devices-Under-Test (DUTs), which is time consuming due to the limited number of wires that can be stressed together in such setups. For instance [12], featuring three ovens per cabinet, can stress 80 DUTs per oven, allowing for a total of 240 DUTs to be characterized in parallel using a single such setup. In addition to this, the available test area on the shuttle is largely I/O pad dominated, which imposes an upper limit on the number of test-structures actually feasible on-die. In contrast, the circuit-based approach [7] (Fig. 2 (b)), utilizes an on-chip heater to establish and maintain a stress temperature locally, using the Temperature-Coefficient-Of-Resistance (TCR) of the metal. This then allows for stressing multiple DUTs simultaneously while also periodically monitoring their resistances using only a few shared pads, thereby enhancing the overall test-efficiency. Compared to an extensive oven-based setup, the approach involves the use of a simple temperature chamber which performs the task of heater TCR extraction together with cooling the active circuits during stress. Depending upon the end user requirement, the impact of realistic circuit aging effects (for instance, stress driver aging) can optionally be further accounted for.

Both the conventional as well as the circuit-based methodologies outlined above are similar in that they both rely on 4-wire Kelvin sensing using dedicated Source-Measure-Units (SMUs) to monitor the resistances of individual wires in isolation following discrete intervals of stress. Instead, this work proposes monitoring the BER of a signal interconnect path for capturing the corresponding EM induced resistance shifts directly in terms of the measured BER. The concept is demonstrated using a dedicated array-based characterization vehicle implemented in a 16nm FinFET technology node, employing a number of novel on-chip monitoring circuit techniques including on-chip heaters, a bit pattern generator and local BER sampling monitors which enable bitwise tracking of '0' and '1' errors separately, resulting in a simplified overall test setup which allows for high precision characterization of EM induced resistance shifts using only digital circuits.

The proposed approach has a number of favorable features which makes it effective for evaluating EM effects, the primary being that the BER is essentially the metric of choice for signal interconnections, directly translating an EM induced resistance shift to a measurable loss in the transmission capability of the interconnect path is particularly relevant to data transmission applications / systems. Second, it eliminates the need of 4-wire Kelvin sensing for the circuit-based approach (Fig. 2(b)) which often imposes either a lower limit on the size of current sourcing switches (implemented using transmission gates) or requires them to operate at a higher VDDs to maintain an appreciable signal to noise ratio, which is typically the case for analog sensing at elevated temperatures, while also eliminating the dedicated SMUs required for these, further simplifying the overall test-setup. Finally, the approach is not limited to a specific interconnect path design and can be easily extended for evaluating EM effects in a real system, directly translating the EM End of Life (EOL) to a corresponding degradation in the circuit performance, rather than guard banded extrapolations based on resistance degradation data obtained from stressing individual wires in isolation.

The remainder of this paper is organized as follows: In section II, we present the digital-intensive macro architecture detailing the on-chip heaters, the datapath specifics and the error sampling circuits together with the silicon implementation summary. Section III outlines our measurement methodology, describing the automated test-sequence adopted for sequentially recording the BER corresponding to selected datapaths in the array. In section IV, measurement results from four independent datapaths are presented and analyzed in detail,

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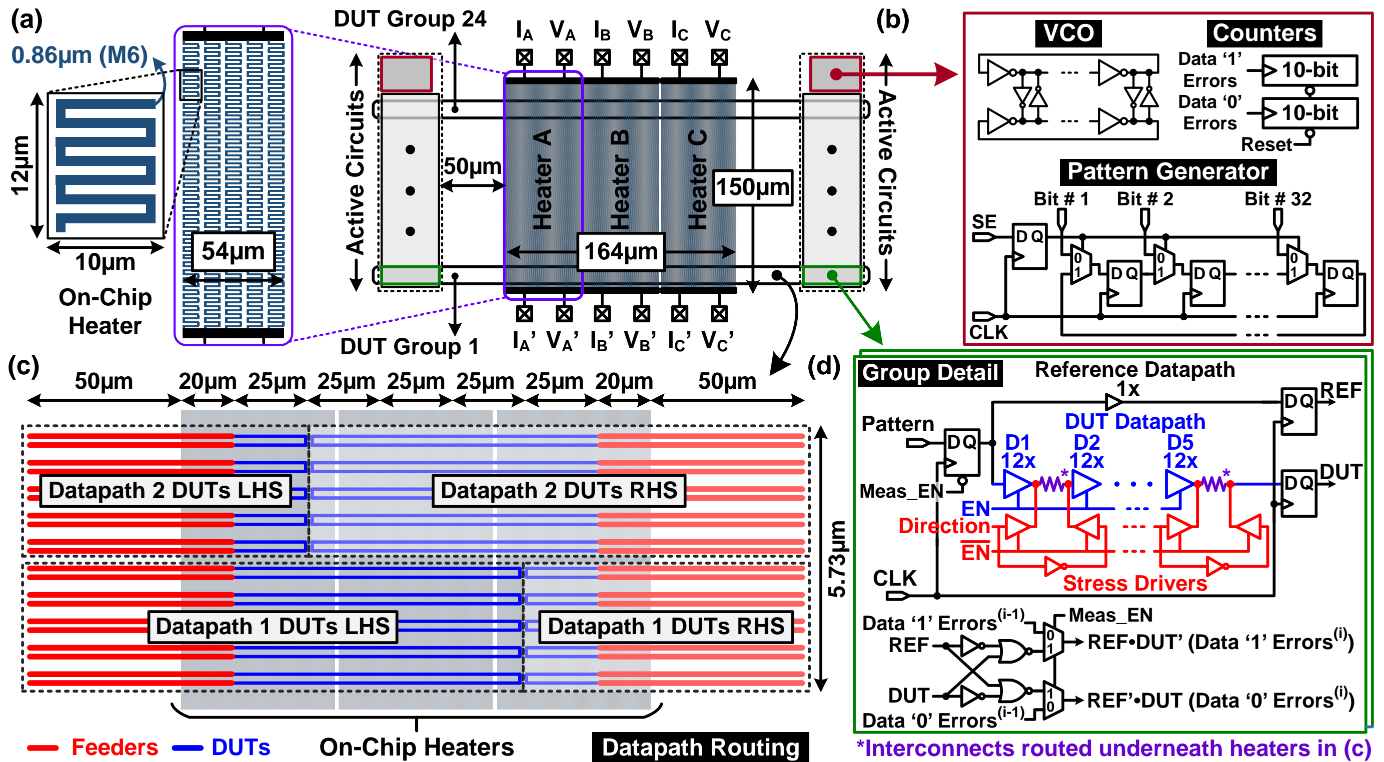

Fig. 3. (a) Overview of the 16nm EM induced BER shift characterization monitor and on-chip heater specifics; (b) Measurement circuit consisting of VCO, error counters, and 32-bit data pattern generator; (c) Datapath routing details comprising one DUT group underneath the heating area; (d) Unit tileable DUT group details: Reference and DUT datapaths, with separate error counters for data '0' and data '1'.

highlighting the efficacy of the proposed approach in capturing the distinct EM resistance shift signatures in terms of the measured degradation in the BER. Section V presents simulation-based analysis, utilizing resistance degradation traces sampled from a test-structure featuring identical wires in the same process [7], showcasing the projected degradation in path operating frequency as a function of stress time for a randomly chosen set of wires. Section VI presents a discussion on the significance of the measured results and the broader scope of application of the proposed technique. Finally, section VII presents the conclusions drawn. To the best of our knowledge, this paper presents the first study experimentally demonstrating the impact of EM on the BER of signal interconnect paths, with the measured trends further analyzed using simulation-based analysis. This paper is an extended version of our previously published conference paper [13].

II. Proposed EM Characterization Vehicle And Silicon Implementation Specifics

A. *The BER-based EM Degradation Monitor*

Fig. 3 presents an overview of the proposed test-chip architecture detailing the on-chip metal heater and the interconnects comprising the datapath routed underneath it, together with the error sampling monitors local to a group and the measurement circuitry specifics. The test-chip is similar in organization to our previous resistance-sensing EM characterization macro [7], with the heating area consisting of the three on-chip metal heaters centrally located, and the active circuits kept at a distance of 50µm away from the heater edges, to avoid any possible damage to core circuits during stress. Architecturally, a unit tileable cell-based approach is followed throughout, both in designing the heaters as well as the left and right arrays housing the local datapath circuits and the error sampling monitors.

Fig. 3 (a) further illustrates the details of the on-chip metal heater, constructed by cascading the unit-cell employing wide Metal-6 (M6) tracks, coiled symmetrically in a serpentine fashion to ensure uniform heat distribution underneath. The local temperature on-die was both sensed and regulated using the 4-wire Kelvin sensing arrangement (I_X, V_X, $I_{X'}$, $V_{X'}$) embedded per heater. This was implemented using bare I/O pads and matched feeders comprising wide Metal-9 (M9) tracks to allow for the application of voltages or currents needed to reach the desired stress temperature, as well as to ensure precise sensing of the actual heating area resistance during testing.

Fig. 3(b) presents the measurement circuitry, located towards the top corner of either array, housing the clock and pattern generator, together with the 10-bit asynchronous counters for separately accumulating the incoming locally sampled errors, corresponding to data '0' and data '1', for a selected datapath in the array. The clock generator is a supply-tuned, 7-staged cross-coupled ring-based voltage-controlled-oscillator (VCO), whereas the pattern generator is implemented as a 32-bit circular shift-register, with a scan-based parallel load

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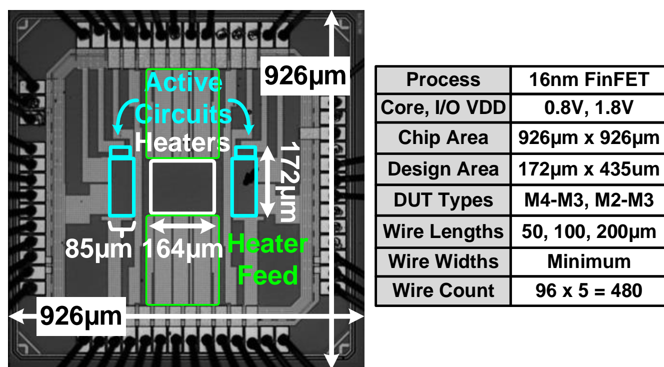

Process	16nm FinFET
Core, I/O VDD	0.8V, 1.8V
Chip Area	926µm x 926µm
Design Area	172µm x 435um
DUT Types	M4-M3, M2-M3
Wire Lengths	50, 100, 200µm
Wire Widths	Minimum
Wire Count	96 x 5 = 480

Fig. 4. 16nm test chip die-micrograph and feature summary.

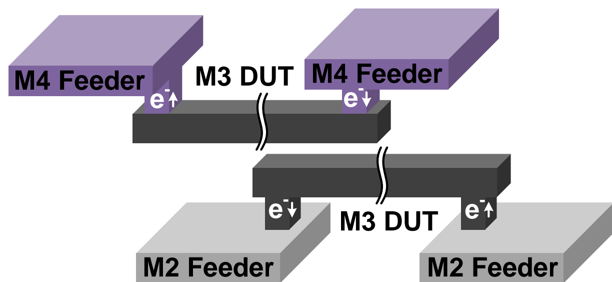

Fig. 5. Implemented metal test structure specifics.

capability.

The DUT groups consist of two separate datapaths per array (Fig. 3 (c, d)), each further consisting of five identical stages comprising a tri-state buffer driving an identical flavor of the interconnect per stage. Fig. 3 (c) illustrates the layout details for one such DUT group, with the interconnect test structures routed underneath the heaters using wide feeder tracks to minimize the IR drop and prevent EM problems outside of the DUT. Furthermore, the DUTs themselves are folded and mirrored so as to maximize the area utilization underneath the on-chip heaters. The BER sampling circuity local to a datapath (Fig. 3 (d)) consists of a reference datapath comprising a signal buffer, along with the actual datapath consisting of the five interconnect stages, both driven by the same incoming pattern sequence. Their outputs are then sampled on the next rising edge of the clock to generate the REF and DUT signals. To enable separate bitwise monitoring of data ‘1’ and data ‘0’ error rates, we perform the logic operations of REF•DUT’ and REF’•DUT for the selected datapath locally, which increment the two 10-bit asynchronous counters housed at the corresponding array top, respectively. The interconnects are DC stressed using separate tri-state stress drivers placed at both ends of the DUTs, with programmable control to allow for a unidirectional current flow in the desired polarity for stressing the DUTs. A scan-based control is used for selecting one or multiple datapaths in parallel during stress, automatically disabling the corresponding datapath drivers. Additionally, a 1-bit control (MEAS_EN) allows for selection of a single datapath for the BER measurement pre- and post-stress. The scan chain providing for a simplistic digital control on-chip is implemented using D-Flipflops (DFFs) employing staggered two phase clocking for added robustness at elevated temperatures during stress.

B. 16nm Test-Chip Implementation

Fig. 4 presents the die-microphotograph together with the test chip implementation summary. The design is implemented in a 16nm bulk-FinFET process with a total of 96 datapaths implemented per chip. The DUTs comprising the datapath are implemented as standard EM upstream - downstream / downstream - upstream interconnect test-structures (Fig. 5) in two distinct metal stacks: Metal-4 (M4) Feeder – Metal-3 (M3) DUT and Metal-2 (M2) Feeder - M3 DUT and in three M3 wire lengths: 50, 100 & 200µm, whereas their widths are kept at minimum allowed by the process. The non-minimum sized feeders routing the DUTs are connected using multiple vias at the driver end (to ensure redundancy) and a single via at the DUT end (Fig. 5).

III. Test Setup And Experiment Flow

Fig. 6 (a) illustrates the measurement flow. Beginning with the on-chip VCO characterization, time-zero (T-0) BER measurements are recorded for the selected datapaths of interest. The BER measurement flow begins with a coarse, initial readout-based estimate of the range of frequencies where the BER is finite. Starting with the highest frequency in this range, and with the measurement window set to the smallest (1µs), the error counts are sampled ‘N’ times (typically 75-100) and averaged. In the high frequency range, this typically results in a ‘saturated’ BER (flat part of the curve, Fig. 9), where all the received bits are in error, with respect to the reference. To ensure statistical confidence in the measured BER, thresholds are defined for both the count average and the coefficient of variation. These targets are relatively straightforward to meet, even with smaller measurement window sizes in the high frequency range. However, they become particularly necessary to track in the low frequency range (represented by the sloped part of the curve in Fig. 9). This is due to insufficient counts sampled at smaller measurement window sizes, which may result in the BER to fluctuate by more than an order of magnitude in some cases. To ensure statistical confidence in the measured BER, the algorithm keeps updating the window size until the specified statistical targets are met, finally updating the initial window size for the next lower frequency. The measurement automatically concludes when no errors are sampled in multiple runs for window sizes ranging in tens of seconds (BER $< 10^{-12}$).

Fig. 6 (b) showcases the linearity in the sampled mean error counts for a range of linearly increasing window sizes. Fig. 6 (c) further illustrates the sampled counter outputs for data ‘0’ corresponding to two windows, differing in size by 45 times, clearly showcasing the improvement in the coefficient of variation for the larger measurement window size, bringing in the statistical confidence to the measured BER. The algorithm also selects between linear and exponential window sizes for faster convergence, depending on the sampled error counts. The BER is calculated using the formulation:

$$BER = \frac{Sampled\ Error\ Count\ Average}{Sampled\ VCO\ Frequency \times 0.5 \times Error\ Window\ Size}$$

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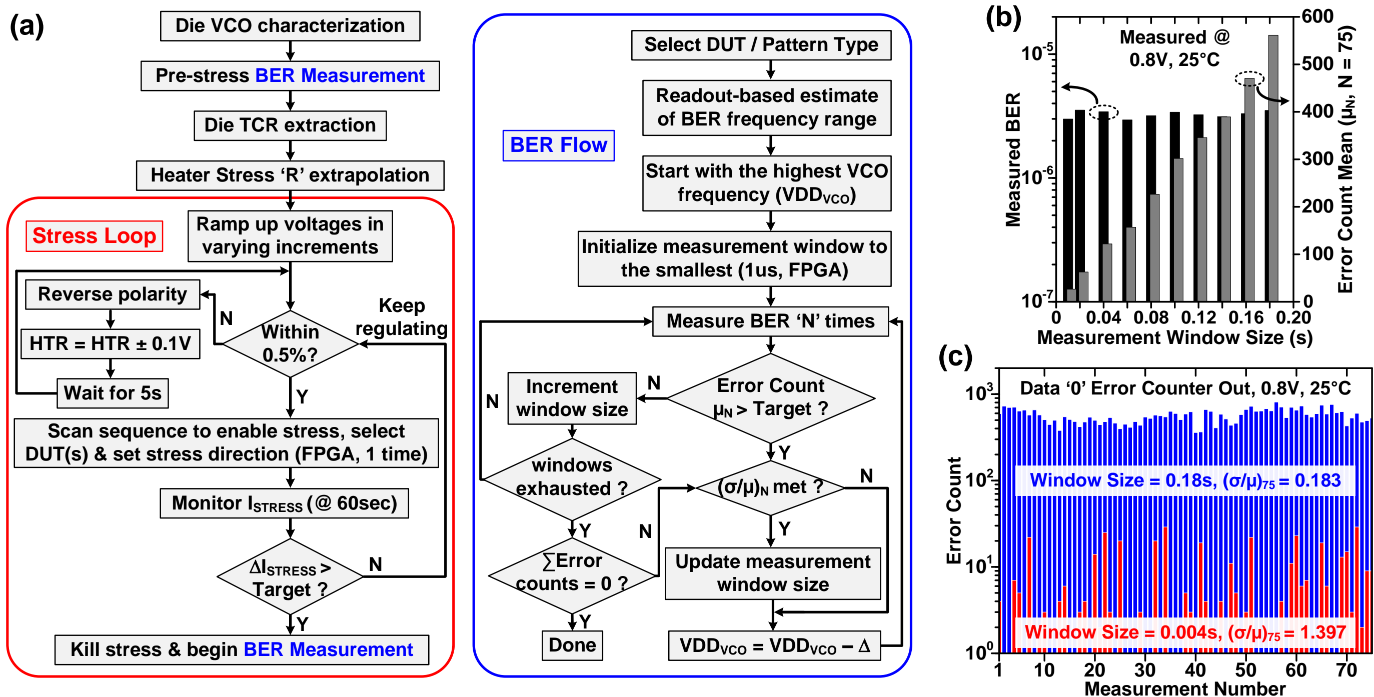

Fig. 6. (a) Automated measurement flow for die TCR extraction, on-chip stress regulation and datapath BER characterization. (b) Measured BER and the linearity in the sampled error count average vs. the chosen window size. (c) Sampled counter outputs for two distinct window sizes differing by 45X, clearly showcasing the improvement in the coefficient of variation (σ/μ) for the larger window size.

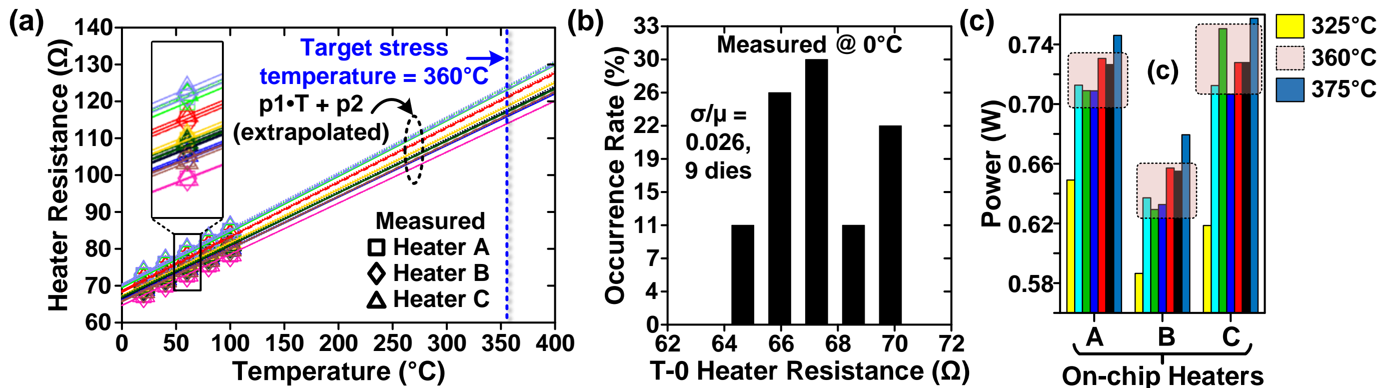

Fig. 7. (a) TCR characterization for the individual on-chip heaters (with distinct colors representing separate dies) together with the extrapolation to the targeted stress temperature of 360°C, (b) the corresponding time-zero (T-0) heater resistance distributions sampled at 0°C and, (c) Heater power required to reach different on-chip stress temperatures obtained from multiple test-chips.

i.e., the BER is essentially equivalent to the ratio of bits received in error to the total number of bits transmitted. The factor 0.5 accounts for the data rate being half that of the clock rate.

The next step in the measurement flow involves the TCR extraction for the on-chip heaters. This is accomplished by ramping up the temperature chamber from 0–100°C in linear steps of 20°C and sampling the individual heater resistances at each temperature step. Fig. 7 (a) presents the extracted TCR obtained from nine test-chips, comprising a total of 27 on-chip heaters, showcasing excellent linearity in the measured TCR for each individual on-chip heater, as well as the extrapolation to the target stress temperature (360°C), obtained using a linear curve fit. Fig. 7 (b) presents the corresponding fresh heater resistance distributions recorded at 0°C, showing a mean heater resistance of 67.3Ω and a standard deviation of 1.75Ω for the measured distribution. Variations in the fresh heater resistances at 0°C result in different target resistance values for different heaters given the same stress temperature, emphasizing the need of precise TCR characterization for each individual on-chip heater prior to the stress measurements. With the per heater stress resistance targets known, the voltages across these are ramped up in varying increments [7] to reach within 1.5-2°C of the final temperature and are continuously regulated thereafter. However, it should be noted that this version of the test vehicle does not feature an arrangement for sensing the DUT resistance itself, such as in [7]. It is assumed that the vertical temperature gradient from M6 to M3 is limited to only a couple of degrees and therefore, the temperature of the DUTs is still in excess of 350°C for accelerated stress purposes. Fig. 7 (c) presents the heater

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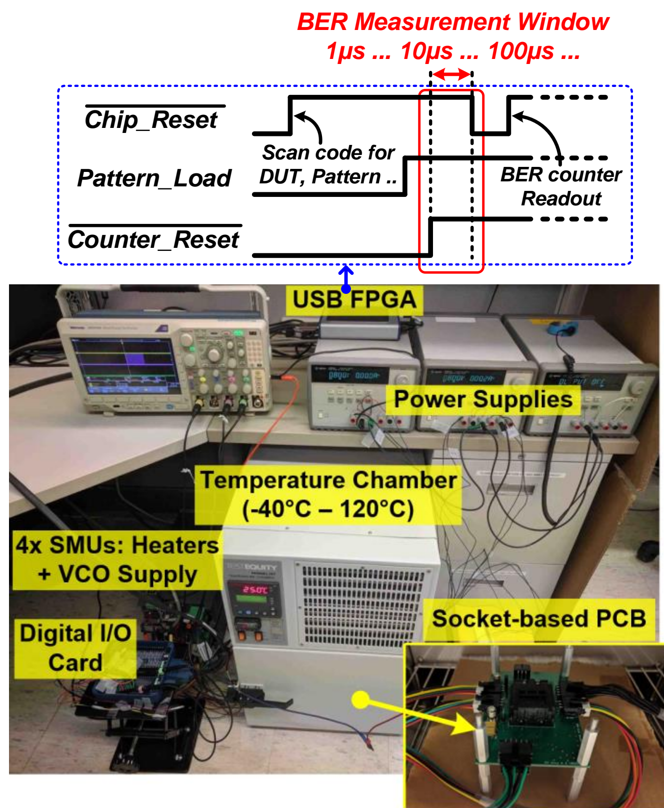

Fig. 8. Measurement setup detailing the FPGA and the test sequence defining the error collection window, the benchtop temperature chamber used for heater TCR extraction and cooling the active circuits during stress mode, as well as the SMUs and the socket-based PCB used for interfacing the test-chips.

power required to reach different on-chip stress temperatures, for the three individual heaters corresponding to distinct test-chips. From Fig. 7 (c), it can be observed that heater 'B' requires a comparatively lower power to reach a target stress temperature, on account of the additional heat it receives from its neighbors. From here on, the shift in stress current is monitored every minute, until it falls below a set target, after which the stress is turned off and the BER for the selected datapaths are characterized again, with the process repeated for the entire duration of the experiment.

Fig. 8 shows the details of our measurement setup. An FPGA board is used for digital signal generation and acquisition activities, for instance, defining the time window for error collection (highlighted), scan-based digital control, on-chip VCO characterization, acquiring counter outputs etc. The on-chip heater regulation and VCO power supply are controlled using SMUs accurate to ±20µV. A benchtop temperature chamber is used for the heater TCR extraction as well as maintaining an ambient temperature of 20°C for cooling the active circuits during periods of stress. The 16nm test-chip is interfaced using a socket-based PCB (inset).

IV. Measurement Results From 16nm Test Chip

We first show experimental data verifying the basic functionality of the 16nm test chip. Fig. 9 presents the time-zero

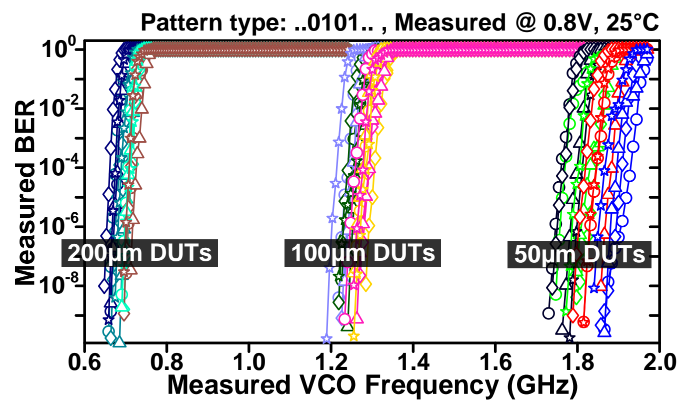

Fig. 9. Time zero BER characterization results corresponding to signal paths featuring distinct interconnect lengths (50, 100, 200µm) and metal stack flavors (M4-M3, M2-M3).

(T-0) BER measurements corresponding to a total of 24 datapaths, in varying flavors of interconnect lengths (50, 100, 200µm) and metal stacks (M4-M3-M4, M2-M3-M2), characterized using a pattern sequence with alternating '0's and '1's. As the clock frequency is swept from low to a high values, the BER increases exponentially and then plateaus, giving rise to the typical BER curve shape shown in Fig. 9. As expected, the BER curves saturate at lower VCO frequencies for interconnects with longer lengths. With parameters such as the driver strength, the feeder length and width, as well as the parasitic circuit loading identical between the datapaths, a degradation of nearly 1.5 times in the mean path operating frequency (for a measured BER of 10^{-6} between interconnect paths featuring identical lengths), is observed for an increase in the interconnect length by a factor of two. The measured separation in the path operating frequency between data '0' and data '1' BERs for a selected datapath (δ, Fig. 10 (a)), is a function of the accumulated delay mismatch stemming from the five buffer stages (Fig. 10 (b)) as a consequence of device variations and varies datapath to datapath. From Fig. 9 and Fig. 10 (c), it can also be observed that datapaths featuring longer interconnect lengths have a tighter distribution compared to the shorter datapaths, on account of the interconnect delay dominating the overall delay, offsetting any transistor variations.

Fig. 11 presents the measured BER results corresponding to patterns with differing numbers of consecutive '0's / '1's, performed as a sanity check on the same 50µm M4-M3 datapath. The BER saturates at a level that corresponds to the ratio between the number of 0-to-1 or 1-to-0 transitions in the data stream to the total number of bits transmitted. As expected, this is because the error only occurs at the point where the data changes, for instance, every bit for .. 0101 .., every other bit for .. 001100 .., every four bits for .. 000011110 .. etc.

For the stress experiments, we have chosen the pattern with alternating '0's and '1's. From our previous resistance-sensing based experiments [7], it was observed that both the M4-M3 and the M2-M3 wires exhibit void formation induced subtle shifts, followed by sudden 3-10X increase in the conductor resistance shortly thereafter, as the predominant EM failure mode, owing primarily to slit-void formations, with a select few DUTs also exhibiting rare progressive shifts overtime (trench-voiding).

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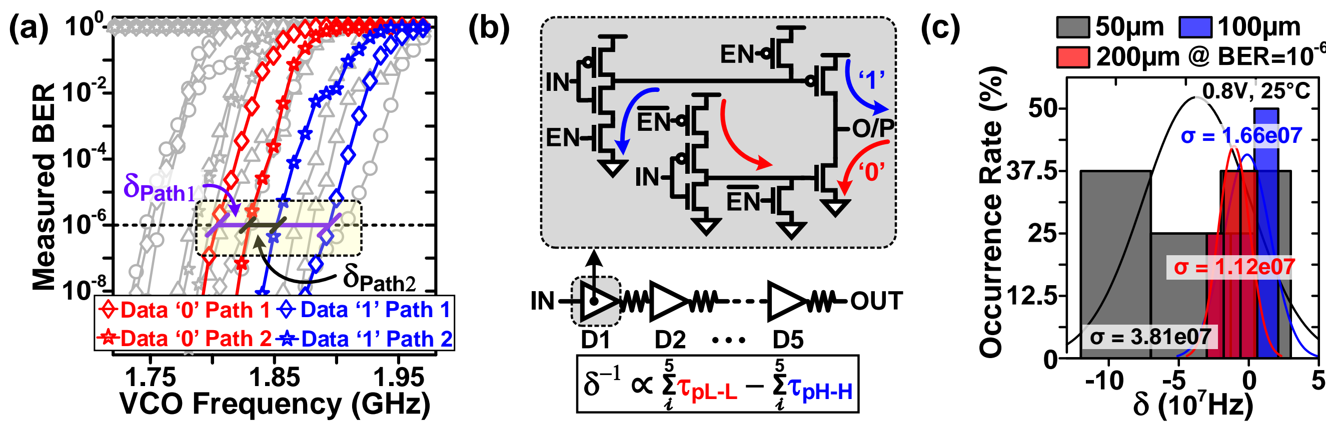

Fig. 10. (a) Zoomed-in version of Fig. 9, detailing the variation induced differences in the measured path operating frequency between data '0' and data '1' BERs, highlighted for two distinct 50μm datapaths, (b) Details of the tri-state buffer design driving a single interconnect stage, illustrating the distinct circuit paths traversed by data '0' & data '1' respectively, amounting to the cumulative variation induced difference and, (c) Histograms for δ, showcasing tighter distributions at longer interconnect lengths, as a consequence of the increased interconnect delay offsetting any device variations.

Furthermore, very few failures were observed at longer wires lengths of 100μm and 200μm [7], as a consequence of the reduced stress current density in the longer interconnect even at the accelerated stress conditions used in this study (1.5V, 340°C). The possibility of stressmigration [14] can be ruled out due to experimental evidence of ample failures in the shorter 50μm DUTs. We therefore focus on studying the EM effects in the 50μm M4-M3 signal interconnects for the remainder of this work.

A total of 8 datapaths, comprising only the 50μm M4-M3 interconnects, are stressed in parallel, with the stress current flowing from the receiver end to the driver end of the wire. Since EM induced void formations typically first nucleate at the electron source or alternately at the current sink (which is essentially the driver end of the wire in this case), this stress direction presents the worst case scenario from the interconnect delay degradation perspective, as per the Elmore delay model [15]. The 40 wire DUTs are stressed while elevating the heater temperature to 360°C. A Proportional-Integral-Derivative (PID) loop, implemented entirely in software, monitors and regulates each on-chip heater individually. To avoid any possibility of degradation in the drivers themselves, a nominal voltage of 0.8V was used for the DC stress. Moreover, the measurement circuits were also powered down during the stress mode. Fig. 12 (a) presents the degradation in stress current I_{STRESS} over the experiment duration, as a consequence of the EM induced DUT resistance degradation over time. Fine shifts in I_{STRESS}, with the threshold set between 1-1.5% are monitored every stress cycle (except for the final two), following which the heaters and stress current are turned off, and the VCO and datapath BER are re-characterized at an ambient temperature of 25°C, regulated using the temperature chamber. VCO characterization results presented in Fig. 12 (b) confirm that the output clock frequency remains constant over the experiment duration, with no signs of device degradation.

Fig. 13 showcases the BER characterization results from four independent datapaths, together with the degradation in path operating frequency for a measured BER of 10^{-6}, plotted as a function of the stress time. The BER curves remain relatively constant with no appreciable shifts for the first 96 to 248 minutes, depending on the datapath number. This represents the initial phase of EM wherein the vacancies are moving towards driver end of the wire. As the EM voids nucleate and grow, distinct abrupt and progressive failure signatures are observed over the experiment duration in different datapaths. For instance, datapath 1 exhibits a slow EM failure rate, with little to no degradation for the first four hours, followed by an abrupt shift and a slow progressive deterioration thereafter. In contrast, datapath 4 presents the fastest degradation over time, exhibiting distinctly evident fast abrupt shifts over the same stress duration, followed finally by slow progressive degradation. Datapaths 2 and 3 also behave similarly, exhibiting abrupt BER shifts as the predominant interconnect failure mode interspersed by progressive deteriorations over time, as one would expect looking at the resistance degradation traces for this DUT type [7]. The significant variation between the degradation behaviors of different datapaths underscores the importance of measuring

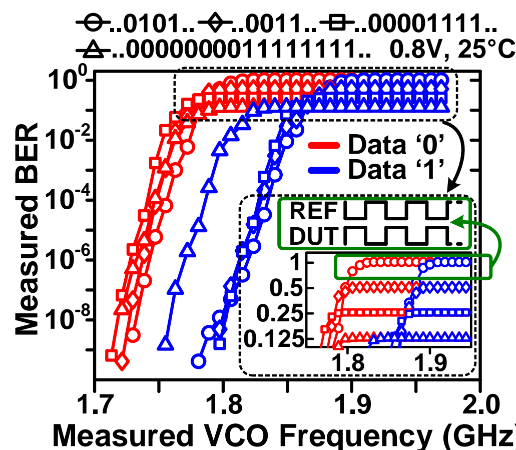

Fig. 11. BER sanity check performed on the same M4-M3 interconnect path, with distinct pattern types featuring differing numbers of consecutive '0's / '1's.

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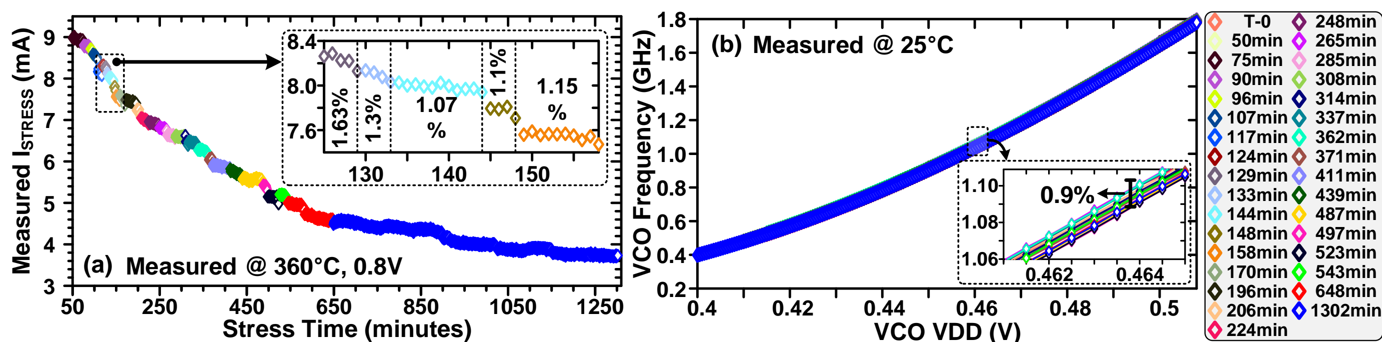

Fig. 12. (a) Measured stress current (I_{STRESS}) degradation and (b) on-chip VCO characterization between multiple stress cycles.

multiple DUTs to understand the overall time-to-failure statistics.

One difference, however, from our previous resistance characterization results is the absence of partial or full recovery in the measured BER, observed in the resistance degradation traces for most wires, following abrupt resistance increases (Fig. 1). This can be attributed to the sharp temperature cycling enabled by the on-chip heater, from a stress temperature of 325°C to a measurement temperature of 100°C, back and forth every 20 minutes, causing some of the wire segments to undergo an annealing-like effect and reconnect. This was primarily needed in the previous work to suppress leakage for reliable analog-sensing of the DUT resistances.

The measured results presented in Fig. 13 clearly establish the efficacy of the BER as a useful metric, in both diagnosing as well as directly translating EM induced resistance shifts to a measurable loss in the transmission capability of the interconnect. As discussed previously, the proposed methodology is not limited to a specific circuit topology or an interconnect path and can be readily extended for monitoring EM effects in a real system.

V. Comparison With Individual Wire EM Test Results

This section presents supplemental simulations incorporating measured wire resistance degradation data from identical M4-M3 wires characterized in the same process, for the purpose of reconstructing the projected degradation in the datapath operating frequency as a function of stress time, using a spice-based analysis. Fig. 14 graphically illustrates the details of our spice-based simulation flow. First, using a sampled resistance trace from a single identical 50µm M4-M3 interconnect, measured using our resistance based EM characterization vehicle [7], together with the associated layout parasitics and loading, a spice sweep is performed to simulate the delay of a single interconnect stage as a function of stress time. Linear curve fitting is then used to extract the coefficients translating the interconnect resistance degradation as a function of stress time to the simulated single stage delay deterioration as a function of stress time. Five out of several identical M4-M3 interconnect resistance degradation traces (corresponding to the same test-chip and stressed in the same run together) are chosen using a random number generator implemented in software. The corresponding single stage delay for each individual wire is then obtained using the linear model derived earlier. Finally, the resulting delays are summed up to obtain the projected degradation in the path operating frequency as a function of stress time. Fig. 14 (lower right) presents ten iterations of randomly choosing five wires and reconstructing the degradation in the operating frequency of the datapath as a function of stress time thereafter. The difference in stress conditions between the two experiments (1.5V vs. 0.8V and 325°C vs. 360°C), together with the fast temperature cycling enabled by the on-chip heater for the resistance-sensing vehicle causing recovery effects results in vastly different failure rates and stress times for the same DUT type. However, as can be observed from Fig. 14, the simulation results showcase a similar projected degradation trend as the measured results presented in Fig. 13, reaffirming the proposed methodology.

VI. Significance And Scope Of Work

In this work, the EM-induced resistance shift was directly translated in high precision to a degradation in the overall circuit performance using in-situ digital error-monitoring circuits, in lieu of the conventional analog-sensing approaches which rely on monitoring the resistance of individual wires in isolation for the purposes of developing a generalized predictive failure model. The goal behind the measurement results presented in this work was to experimentally validate the hypothesis of a strong correlation between an EM-induced resistance shift event and the associated change in the BER, thereby directly translating the former to a relevant performance loss for the circuit-under-test, as well as establishing the efficacy of the latter as a metric diagnosing these effects. As discussed in the introduction, the proposed digital on-chip approach has numerous advantages including a simplified test-setup, an improved test-efficiency leading to efficient collection of failure statistics, elimination of leakage artifacts compared to the previously proposed on-chip sensing approach [7], measurement results capturing relevant at-speed performance loss, elimination of unnecessary guard-bands stemming from generalized modeling and ease of in-situ integration.

The proposed technique of monitoring EM-induced degradations using the BER has been employed in the current work for analyzing the degradation in the transmission capability of an arbitrary datapath comprising five interconnects. However, from a broader perspective, the technique can be extended for an accurate and statistically efficient assessment of EM reliability in actual circuit settings involving both signal and power interconnects alike. First, it is

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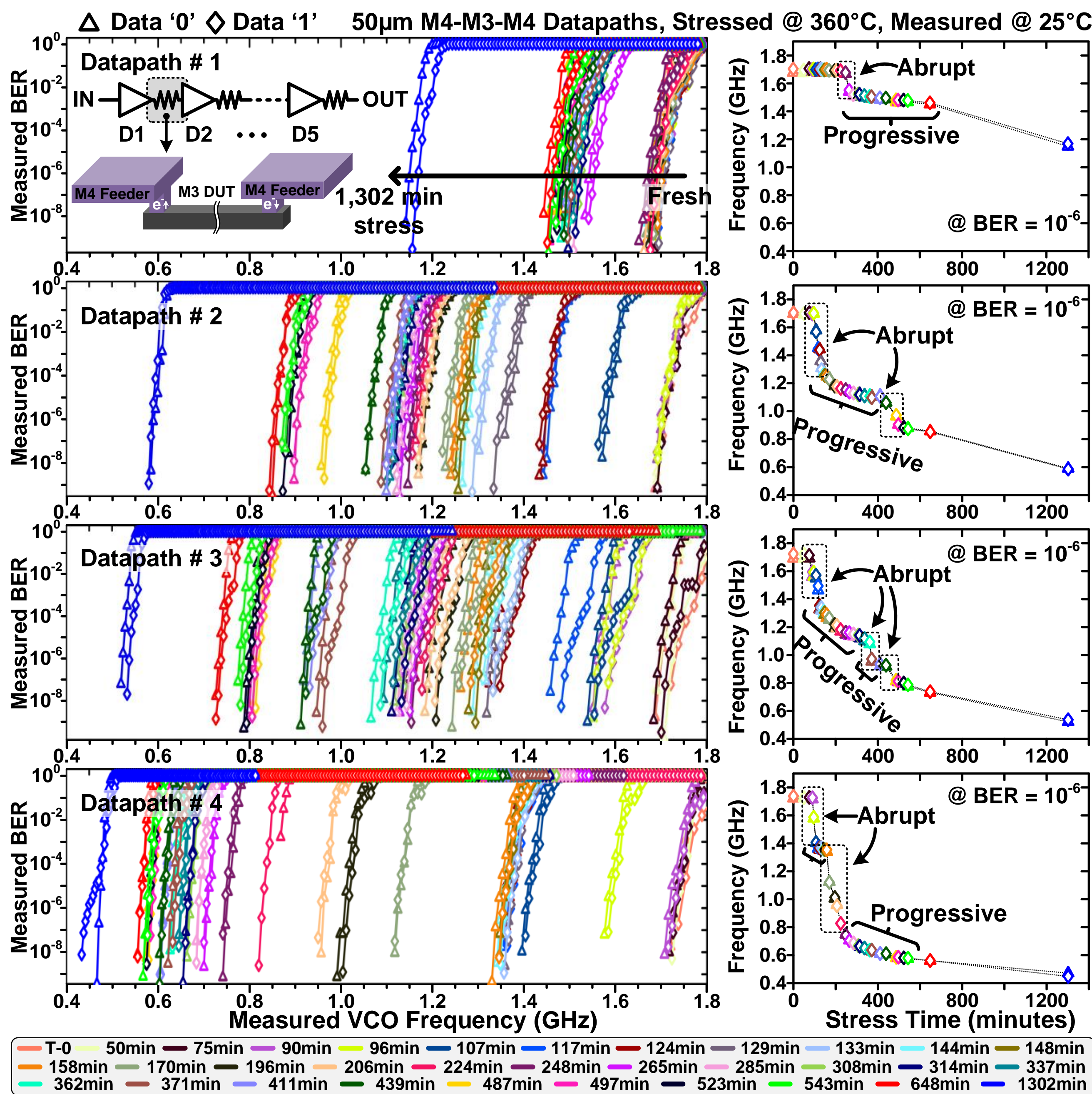

Fig. 13. Left: Measured shift in the BER captured over a 1,302 minute stress period and, Right: Degradation in the path operating frequency vs. the stress time, for a BER of 10^{-6}.

important to note that the formation of EM-induced voids and hillocks not only impacts the resistance but also the capacitance of a metal test-structure, which becomes particularly important to account for in sub-nanometer design nodes wherein the interconnects are typically spaced minimum pitch apart. The impact of capacitive effects becomes dominant at higher test-frequencies and BER tracking allows for quantifying the effect of cumulative phase shift introduced by both R & C changes in a metal line as a consequence of an EM event on the actual circuit performance degradation at-speed. Although the measurements in this work have been done at a relatively low test-frequency of 1.8GHz (limited by the datapath design), the frequency may exceed several GHz in actual scenarios involving single driver / interconnect stages in close proximity. High frequency functionality testing using the BER as a metric will then become useful in such scenarios in diagnosing the overall performance impact dictating the separation between metal lines.

Second, the proposed methodology is still attractive from the point of view of efficient collection of failures from a large sample population of DUTs for accurate estimation of MTTF statistics, since the BER can track both fine progressive as well as abrupt resistance changes. As discussed previously, the digital-intensive nature of the test-structure forgoes the leakage-artifacts present during 4-wire sensing in the previously proposed on-chip approach [7], thereby bringing greater

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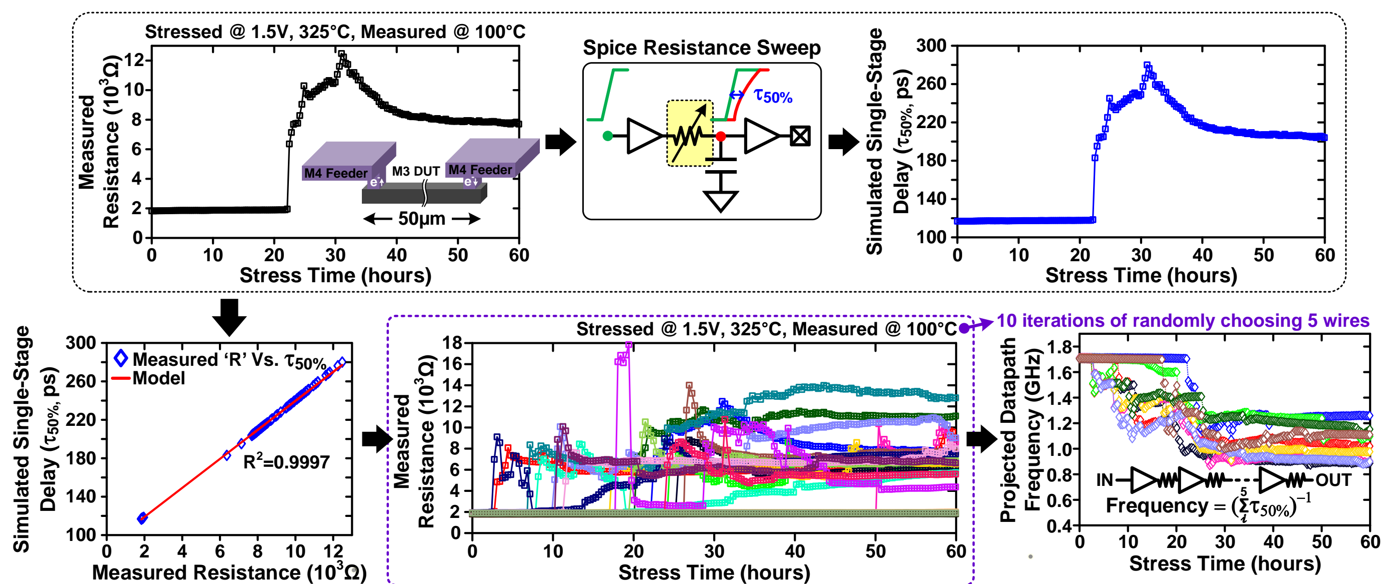

Fig. 14. Graphical illustration detailing the simulation flow used for estimating the projected degradation in the path operating frequency as a function of stress time, incorporating measured wire resistance traces fabricated in the same 16nm process [7]. A single stage spice simulation incorporating the sampled wire resistances as a function of stress time corresponding to a single DUT together with capacitance parasitics loading the stage, is used for obtaining the degradation in delay as a function of stress time. A linear curve fit between the two coupled with resistance traces sampled from several identical M4-M3 DUTs are randomly picked for constructing the projected degradation in the simulated operating frequency for a five staged interconnect path, identical to the one studied in this work.

precision in the measured results. Moreover, these measurements can easily be made arbitrarily sensitive to the interconnect resistance changes by further reducing the driver resistance (by either increasing the supply voltage or the driver device width), thus allowing the user to accurately study subtle EM-induced void nucleation and subsequent growth.

Third, the technique can be readily extended to monitoring realistic EM effects on-die in an stressed power-grid supplying power to circuits underneath. One way to do this by keeping the reference datapath and associated BER monitoring circuits as part of a separate unstressed power-grid sharing the same clock and data inputs. The resistance increase due to EM effects in the stressed power-grid would then be translated to an equivalent phase-shift at the output of the circuit-under-test, thereby resulting in a degradation in the T-0 BER with respect to the reference.

To emphasize, the key benefit of the proposed methodology is that it translates EM reliability directly to define an acceptable circuit failure criterion for the designer, rather than an generalized failure criterion, for instance, a 10% shift in the interconnect resistance. The actual circuit may well work as expected for a 10% shift depending upon the application requirements and therefore the technique maybe more fitting for assessment of EM-reliability in a real circuit setting as compared to conventional sensing approaches.

VII. Conclusion

In this work, we experimentally studied the impact of EM effects on the BER of signaling interconnections using a dedicated array-based characterization vehicle. An interconnect path comprising five buffer stages each driving an identical interconnect load, was subjected to DC stress. Accelerated stress testing was enabled entirely on-chip using metal heaters, forgoing the need of extensive oven-based equipment conventionally used for achieving stress temperatures in excess of 300°C. Rather than periodically sensing the DUT resistances using a 4-wire arrangement, the degradation in BER with respect to a reference path was instead utilized as a metric for both diagnosing and capturing EM induced resistance shifts. Measured results were presented from four independent datapaths, validating the efficacy of the proposed approach in capturing distinct EM resistance shift signatures in terms of BER shifts. Simulations, incorporating interconnect degradation traces from individual wire segments, reconstructing the project degradation in the datapath operating frequency were presented further to supplement the observed measurement trends. The digital-intensive nature of the proposed on-chip approach, utilizing simple error monitoring circuits to translate EM induced resistance shifts to an associated degradation in the measured BER, makes it an effective tool for characterizing EM effects in signal and power interconnections alike.

Acknowledgement

The data collection and analysis was supported in part by Semiconductor Research Corporation (SRC).

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