A Calibration-Free Synthesizable Odometer Featuring Automatic Frequency Dead Zone Escape and Start-up Glitch Removal

Tahmida Islam, Junkyu Kim and Chris H. Kim
Department of Electrical and Computer Engineering, University of Minnesota
200 Union Street SE, Minneapolis, MN 55455, USA

David Tipple, Michael Nelson, Robert Jin and Anis Jarrar
NXP Semiconductors
6501 W William Cannon Dr., Austin, TX 78735

***Abstract*— This paper presents a synthesized version of the silicon odometer aging sensor for measuring the frequency degradation caused by device degradation mechanisms in high volume semiconductor products. In the design, three ring oscillators (ROSCs) composed of inverter, NAND, and NOR gates are implemented in register-transfer-level (RTL), with the ability to be stressed in an AC or DC stress condition. The new odometer has product level features such as calibration-free operation, automatic frequency dead zone escape, and start-up glitch removal. The odometer verilog code was synthesized and automatically placed-and-routed in three different technologies using standard ASIC design tools. As a proof of concept, we show aging data collected from a 65nm test chip with 12 synthesized odometer instances. The open-source RTL files and testbench of the synthesizable odometer can be downloaded from https://github.com/reliability-research/odometer.**

***Index Terms*—Silicon odometer, aging sensor, ring oscillators, RTL, ASIC, synthesized.**

I. Introduction

In this work, the beat frequency detection based silicon odometer aging sensor [1, 2, 3] was implemented fully in Register-Transfer Level (RTL) and taped out using a standard ASIC design flow. The new synthesizable odometer does not require any custom layout blocks such as power gates or frequency trimming circuits, and is built using a combination of structural and behavioral Verilog. This RTL code can transfer the design to any planar or FinFET technologies with Place-and-Route (PnR) tools requiring no custom-designed schematic or layout. PnR tools can use available standard cell library files to construct odometer circuits with different gate types, device flavors, and ring oscillator lengths, based on the needs of the design team. Setup and hold time of each flip-flop can be checked using static timing analysis tools. In terms of the core odometer functionality, as in our previous odometer designs, the new synthesizable design enables picosecond resolution within microsecond-order measurement times, preventing unwanted stress or recovery from affecting the measurement accuracy.

We also made critical updates to the original "academic" odometer design to ensure the odometer IP can operate reliably across a wide range of process-voltage-temperature conditions with no calibration required. The improved design features include a calibration-free power supply to the ring oscillators driven by four parallel 8X inverters in lieu of custom-designed power gates. Existing power gates used for ASIC chip power management were too large to shut down virtual supply voltage of the fresh ring oscillator. Without calibration, frequency degradation measurement may undergo a dead zone when frequencies for stress and reference oscillators are very close (e.g. within 0.1% of each other for a maximum beat frequency count of 1,000). In that case, the beat frequency detector in the previous odometer design will continue counting a very high count value which can result in a count overflow. To address this operational issue, a Verilog module for enabling the circuit to automatically come out of the dead zone was added in the RTL. The design also includes a technique to remove glitches in the ring oscillators at the beginning of the measurement phase, when the ring oscillator loop is enabled at the same time the virtual power supply is turned on. The three aforementioned features added in this work (i.e. no calibration, frequency dead zone escape, and glitch removal) make the proposed synthesizable odometer amenable to being implemented in high-volume semiconductor products.

The remainder of the paper is organized as follows. In section II, the prior silicon odometers are briefly discussed. In section III the design modifications in the new synthesizable design have been explained. Section IV shows the experimental results of the new design implementation and section V contains the concluding remarks.

II. Previous Odometer Designs

This work builds on the silicon odometer aging sensor based on the beat frequency measurement technique developed in [1, 2, 3]. Stress is applied on the logic gates in a ring oscillator by

Tahmida Islam, Junkyu Kim and Chris H. Kim are with the Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455, USA (email: islam112@umn.edu)

David Tipple, Michael Nelson, Robert Jin and Anis Jarrar are with NXP Semiconductors, Austin, TX 78735, USA

applying a stress voltage, and the frequency of the stressed oscillator is compared to the frequency of a fresh ring oscillator (which is only active during frequency measurement). An internal counter counts the beat frequency values, so these measurements are free of any static or common mode noise issues. An all-in-one odometer structure was introduced to measure different types of aging processes such as Hot Carrier Injection (HCI), Bias Temperature Instability (BTI) and soft dielectric breakdown [2]. An array based structure for collecting a statistically significant amount of frequency shift data was demonstrated in [3]. An odometer structure to separate characterize both on-state and off-state BTI in both PMOS and NMOS devices using dual power rails was recently proposed in [4]. Here, two sets of power and ground rails are introduced to stress odd and even stages of the ring oscillator, to facilitate aging in both PMOS and NMOS transistors.

The structure discussed in this paper uses the core beat frequency detection concept from [1, 2, 3] but the design has been made to be compatible with industry standard logic synthesis and automatic placement and route tools. Another notable difference is that previous designs had separate power supply voltages and internal power gates which allowed fast voltage switching between stress mode and measurement mode, whereas the new odometer is based on a single power supply voltage which is required for product chips. Additional features that have been added in the new design are (1) a ring oscillator glitch removal circuit, (2) a circuit to escape the frequency measurement dead zone to achieve a calibration free operation.

III. Proposed Synthesizable Odometer Design

Figure 1 shows the top level block diagram of the odometer circuit implemented in RTL. DC or AC stress is applied to the three ring oscillators simultaneously which are configured as open-loop delay chains, and these chains form oscillators in the measurement mode, by closing the loop from output to input.

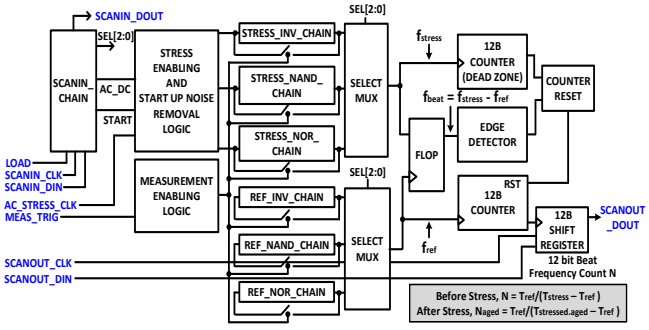


Figure 1. Block diagram of synthesizable and calibration-free odometer circuit with INV, NAND, and NOR ring oscillator pairs.

The main components of the circuits are described below:

A. Beat frequency circuit and calibration-free operation

The main operation of this circuit consists of a single flip-flop device, which operates as a phase comparator sampling the stress oscillator signal to the reference oscillation. The reference oscillator remains fresh (without stress for preventing aging) while the stress oscillator undergoes AC or DC stress in the stress mode of operation. So the stressed oscillator devices suffer from aging, and the frequency of the ring oscillator will reflect the effect. If the rising edges of the fresh and stressed ring oscillator start from the same time, we will see a gradual shift in the rising edges and after N cycles of the fresh ring oscillator, both of their rising edges will coincide again. In the meantime, the stressed oscillator will generate N-1 oscillations, considering the case when the frequency of the reference ring oscillator f_{ref} is higher than the frequency of the stress ring oscillator f_{stress} before applying stress. Let us say before stress,

$$N \times \frac{1}{f_{ref}} = (N-1) \times \frac{1}{f_{stress}} \quad (1)$$

After stress is applied, the count value before the rising/falling edges of the oscillators coincide changes to N'.

$$N' \times \frac{1}{f_{ref}} = (N'-1) \times \frac{1}{f_{stress}'} \quad (2)$$

From these equations, we can calculate the frequency degradation as

$$\frac{f_{stress}'-f_{stress}}{f_{stress}} = \frac{N'-N}{N'(N-1)} \quad (3)$$

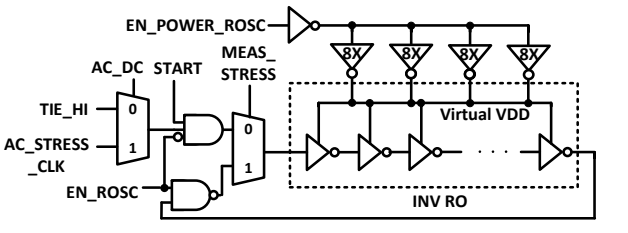
There are two other scenarios. If f_{ref} is lower than f_{stress} in both before and after applying stress, the frequency degradation will be

$$\frac{f_{stress}'-f_{stress}}{f_{stress}} = \frac{N-N'}{N'(N+1)} \quad (4)$$

If f_{stress} is higher than f_{ref} but eventually becomes lower with stress,

$$\frac{f_{stress}'-f_{stress}}{f_{stress}} = \frac{N+N'}{N'(N+1)} \quad (5)$$

Depending on the relative condition of the reference and stress ring oscillator frequencies, we have used equations (3), (4) and (5) for the post processing of our data.




```
INV2  INV(.A(MEAS_STRESS), .X(MEAS_STRESS_INT));                                   RTL code
INV2  INV_POWER(.A(EN_POWER_ROSC), .X(SEL_POWER_OFF));
AND2  AND2_OFF (.A1(SEL_POWER_OFF), .A2(MEAS_STRESS_INT), .X(SEL_POWER_INT));
INV8  INV8_base_1 (.A(SEL_POWER_INT), .X(MOD_VDD)); //default power switch1
        assign EN_VDD = ~( ~MEAS_STRESS | SEL_POWER_OFF );
        assign  IN_INV =(EN_ROSC &  ~(OUT_INV & SEL_INV)) | (~EN_ROSC & ~EN_VDD & START & AC_DC
& AC_STRESS_CLK);
        assign  IN_NAND =(EN_ROSC &  ~(OUT_NAND & SEL_NAND)) | (~EN_ROSC & ~EN_VDD & START &
AC_DC & AC_STRESS_CLK);
        assign  IN_NOR =(EN_ROSC &  ~(OUT_NOR & SEL_NOR)) | (~EN_ROSC & ~EN_VDD & START &
AC_DC & AC_STRESS_CLK);
        assign  OUT = EN_ROSC & ((OUT_INV & SEL_INV) | (OUT_NAND & SEL_NAND & ~SEL_INV) |
(OUT_NOR & SEL_NOR & ~SEL_NAND & ~SEL_INV));
ROSC_STRESS  ROSC_STRESS(.IN(IN_INV), .OUT(OUT_INV), .VDD(MOD_VDD), .VSS(VSS));
```

Figure 2. Four parallel 8X inverters control the virtual supply of each ring oscillator.

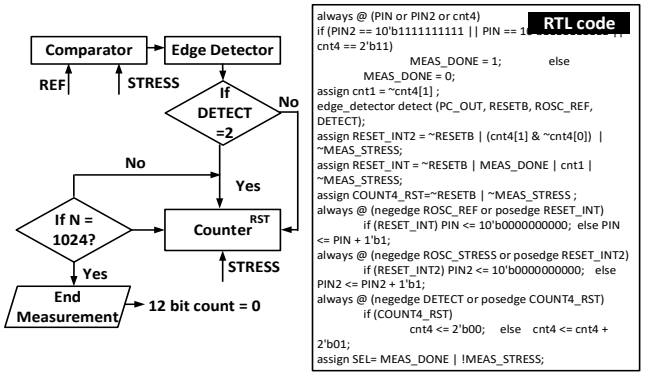


Figure 3. Flow chart of the block to enable the circuit to come out of the frequency dead zone and the RTL implementation of the flow.

Notice that the denominator of the above expression is the product of the count values (typically 100-200) which translates into a two orders of magnitude or higher frequency measurement resolution compared to a non-beat frequency linear counting method [2]. A 10 bit counter counts the beat frequency N, which is equal to the difference between the frequency of the reference fresh ring oscillator (f_{ref}) and the frequency of the stress oscillator ($f_{stress.}$). The counter uses the reference oscillator as the clock signal. The original silicon odometer included frequency trimming circuits that allows tuning of the initial ring oscillator frequencies so that (1) we can get a reasonable beat frequency count (e.g. 100-200) for achieving a high resolution and (2) the beat frequency count decreases monotonically [2]. In the new RTL based design, the frequency trimming circuitry (i.e. programmable custom power gates) has been removed since it's possible to extract the accurate frequency shift as long as the count remains in a reasonable range (e.g. >50) throughout the lifetime of the chip. This makes the overall design attractive for product chips since the whole design can be done in a standard physical design flow. Even without the frequency trimming capability (i.e. relying on the natural frequency difference between two free running oscillators), the frequency shift could be measured with a resolution of 0.01% as shown in our experimental results.

To stress the standard cell gates of the ring oscillators in the stress ring oscillator and to keep the gates of the reference ring oscillators fresh, the power lines of the ROSC need to be kept separate. These power supplies will be turned on during the stress phase (only for the ROSCs that need to be stressed) and the measurement phase (for both the ring oscillators as they will work as free-running ring oscillators). The ROSC power supply control is shown in Figure 2. Four parallel and distributed 8X inverters turn on or turn off the virtual VDD of the individual ROSCs while minimizing the IR drop. The IR drop in the ROSC power was less than 8mV in post-layout SPICE simulations.

B. *AC and DC stress*

AC and DC stress can be applied to all three types of chains, as shown in Figure 2. The START bit, set by the serial input bits from the scan in chain, initiates the stress mode. The AC_DC bit decides whether to stress the chains with an AC (oscillations generated by a separate high frequency voltage controlled oscillator) or DC high voltage signal. The high voltage stress will cause BTI aging in the PMOS devices of the ring oscillator inverters (or NAND and NOR gates operating as inverters), and AC stress will cause both HCI and BTI.

C. *Counter to escape dead zone*

If the frequency of the stress and reference oscillators become too close to each other (e.g. <0.1% for a 10-bit BF counter), the relative phases of the stress oscillators will remain unchanged for a long time (higher amount of oscillation cycles) and the beat frequency counter will keep counting even after it rolls over, which means it will cause overflow in the beat frequency counter. The flow diagram in Figure 3 shows a second 12 bit counter that produces a beat frequency count output of zero and terminates the measurement phase if the circuit cannot detect any phase change before the 12 bit counter overflows.

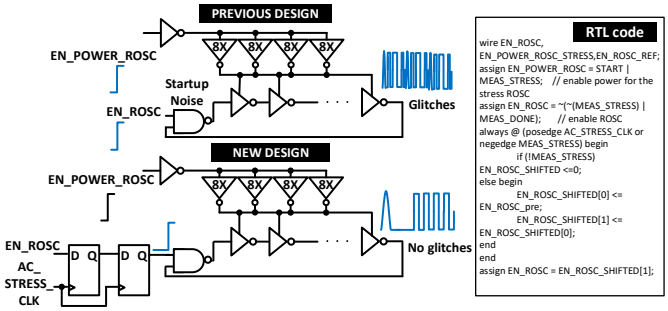


Figure 4. Circuit modification to avoid unstable oscillations in the ROSC during start up. The ROSC starts to oscillate one full AC stress clock period after the virtual power supply is turned on.

D. *Start-up glitch removal circuit*

During the beat frequency measurement, the ROSC power supply is enabled first and then the feedback loop of all the oscillators are closed. Any glitch - either due to the power initialization or due to the transition from an open loop to a closed loop state in the ROSC can cause unstable oscillations that might or might not clear up with time, as shown in Figure 4. These glitches, if their amplitude is higher than the threshold voltage of the devices, will activate the counter and produce garbage beat frequency count values. To avoid this phenomenon, in our proposed design the power of ROSC is enabled and after one full cycle of the external AC stress signal the ring oscillator loop is closed, the stress signal period is sufficient to provide enough time for the inverters in the open loop chain to pass the glitches formed due to power enable to eliminate the glitches.

To demonstrate the ease of transferring the RTL to different technologies, we implemented the same odometer design in 65nm CMOS, 22nm FinFET, and 22nm FD-SOI. The layout structure of the different ROSCs and the top level odometer layouts are shown in Figures 5 and 6, respectively. Each technology design has different numbers of ring oscillator

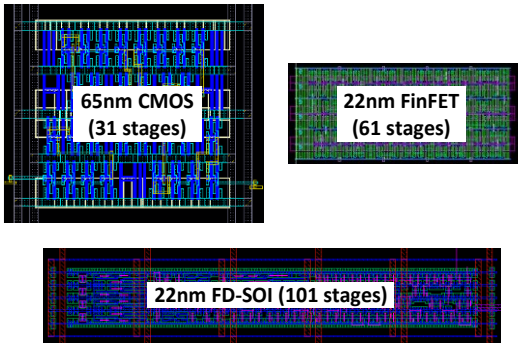


Figure 5. Auto placed-and-routed ring oscillator layout in 65nm, 22nm FinFET, and 22nm FD-SOI.

stages. The number of stages can be easily modified in the RTL, depending on the desired frequency range for the technology. Also in our design only the ring oscillator gates are powered by the 8X inverter bank, while the loop and stress enabling circuits are powered by the main supply. During the measurement mode, when the oscillator loop is closed, the loop control circuitry becomes a part of the ring oscillator and the delay associated with these gates contribute to the frequency of the oscillator. As this frequency directly affects the beat frequency count and the frequency shift, if this circuitry delay contributes more than ~5% of the total oscillator frequency, the degradation values can contain delay portions from the loop control gates and can make the resulting beat frequency measurements unreliable. So, the ring oscillator stages have been chosen to be in the 31-101 stage range so that the loop control gates do not add more than 5% delay to the oscillator period.

In the full chip structure, different layout topologies have been followed for different technology nodes. One main concern while constructing the layout was that the routing should be done in such a way that the signal lines that supply power to the ring oscillators have minimum voltage drop. To achieve that, all four 8X inverters have been placed as near as possible to the ring oscillator pairs, and the routings have been made wider. The ring oscillator structures have been synthesized and laid out separately. The placement of the odometers in the odometer chain has been done manually. 65nm chain consists of 12 odometers, 22nm FINFET design has 60 odometers and 22nm FD-SOI design has 80 odometers with 3 types of threshold voltage flavors (low VT, super low VT and regular VT). Different odometers in the same chain will reflect process variations in the chip.

IV. Experimental Data from 65nm Test Chip with a 12 Odometer Daisy Chain

Test data from the proposed design implemented in 65nm technology, with a daisy chain of 12 odometers, is presented in Figure 7, for INV, NAND, and NOR ROSCs, by varying the operating voltage and temperature. The results show the t^n power law behavior of BTI and HCI aging with time. All the chips have been stressed for 29.1 hours. The results show the clear aging behavior of the ROSC circuits with a resolution of ~0.01% even under nominal 1.2V conditions. Unlike our past

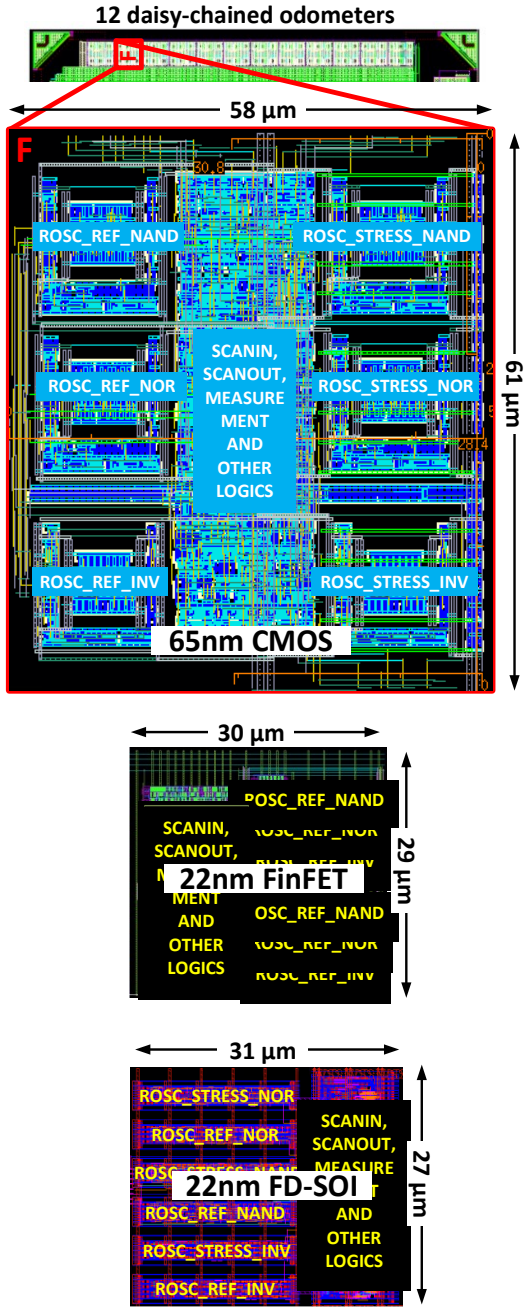


Figure 6. Full odometer top level layout in 65nm and 22nm.

odometer designs, the supply voltage of the stressed ring oscillator remains the same during both stress and measurement modes, which means measurement was done with the same voltage as the stress voltage. The frequency shift data in Figure 7 should be interpreted in light of the fact that the same Vt shift has a stronger impact on the ring oscillator frequency at lower supply voltages. Simply put, the frequency shift would be have been much greater at 1.8V compared to 1.2V if the measurement voltage was uniformly set to 1.2V.

A python based control software running on a 1.8 GHz quad-core ARM board was used to remotely control the entire stress and measurement sequence. Beat frequency count values have been measured from the 12 odometer daisy chain, interrupting the stress for less than a microsecond to prevent unwanted recovery, on an exponentially increasing sampling interval [5]. The first measurement was taken as soon as the control software allowed (~10 millisecond), with subsequent measurements taken at 0.1 second, 0.2 second, 0.4 second, 0.8 second, etc., intervals. Test data shows more frequency degradation in NOR gates (1.25% @ 1.5V, 100°C, 29.1 hours) than NAND (0.90%, same condition) and INV (0.75%, same condition). The reason for this behavior is, high voltage stress in a ring oscillator causes BTI stress in PMOS devices and NOR gate has stacked PMOS devices in its pull-up structure. These stacked devices have higher sensitivity to NBTI induced degradation. NAND gates showed slightly higher degradation than INV gate due to the longer pull-down delay which isn't affected by NBTI. Interestingly, in our experiment due to malfunction in the control software, 1.8V, 100°C, NAND data shows stress interruption at ~10^4 seconds. As expected, the

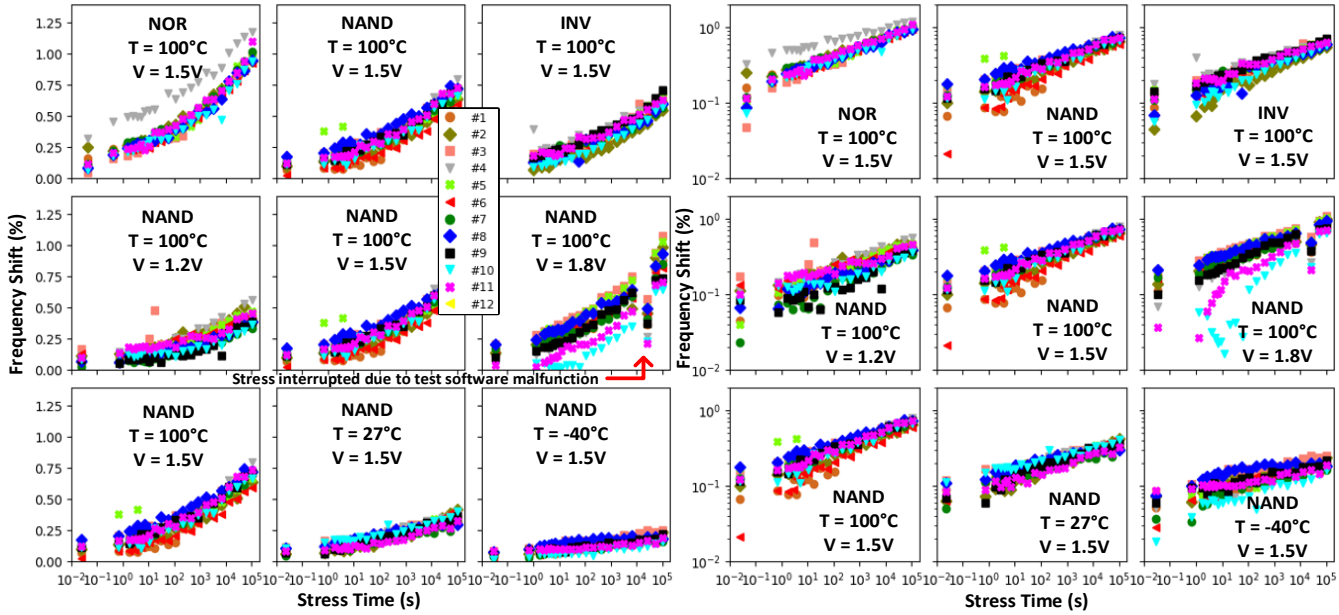


Figure 7. 65nm silicon data from 12 odometers on the same die plotted in (left half) linear-log scale and (right half) log-log scale. (Upper row) NOR vs. NAND vs. INV. (Middle row) 1.2V vs. 1.5V vs. 1.8V. (Bottom row) 100°C vs. 27°C vs. -40°C.

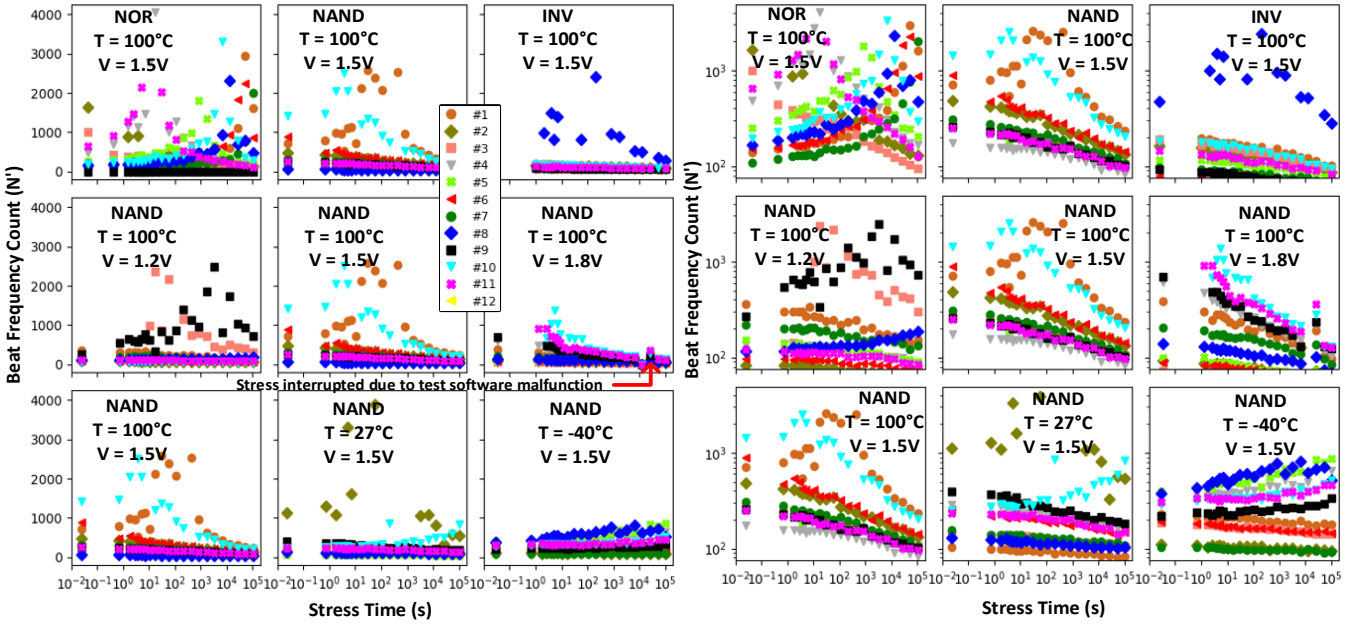


Figure 8. Raw beat frequency values used to generate the linear-log and log-log plots in Figure 7. The beat frequency count either monotonically decreases, or first increases and then decreases, depending on the relative magnitudes between f_{ref} and f_{stress}. Equations (3), (4), and (5) were used to convert the beat frequency count data in Figure 8 to frequency shift data in Figure 7.

degradation quickly goes back to the original trend line after the stress is active again.

Frequency shifts measured at different voltages (1.2V, 1.5V, and 1.8V) and temperatures (-40°C, 27°C, and 100°C) are shown in Figure 7. We can see that the NAND type oscillator frequency degrades up to 1.25% at 1.8V and 100°C, whereas for 1.2V, the degradation in the same type of gates reaches 0.70% after stress, which shows the increase in degradation with stress voltage. It's important to note that (1) the stress voltage and measurement voltage are the same in our design, and that (2) the aging sensitivity is lower at higher voltages due to the higher gate overdrive, which affects the frequency shift results. For 1.5V stress in NAND ring oscillator measurements, we can see the effect of temperature on frequency degradation. Frequency shift under a 100°C/1.5V/29.1 hour stress reaches 0.80%, and for -40°C, the degradation reaches 0.24%. Different color points show the variability in degradation in 12 odometers.

Figure 7 (right half) shows the same degradation values of Figure 7 (left half) but in a log-log scale. The straight line shows the linear relationship between log of degradation and log of time. We can also see that at the beginning of the stress time, the variation among the 12 odometers in the chain is larger due to the lack of a precise initial beat frequency count calibration. With the progress of stress time however, the degradation gradually becomes dominant compared to the initial resolution mismatch resulting in a more consistent frequency shift data. Figure 8 shows the beat frequency count values for the same stress conditions as Figure 7, in absolute values and in log scale. From the count values we can see that the beat frequency count increases with stress time, then in many cases it enters the dead zone and starts decreasing, also in some cases the count decreases for the entire stress period, which gives us an idea whether reference frequency is higher or lower than the stress ROSC frequency, and we can use the correct equation from (3), (4), and (5) for calculating the % frequency shift values.

V. CONCLUSION

This paper presents a significantly improved structure of the previously presented on chip odometer design. The beat frequency detection techniques along with the modification has been written in RTL (verilog) language, which is fully synthesizable and tunable, and can be transferred to any technology. The calibration feature in the previous design has been removed to make the design more attractive from a product implementation perspective. The design has also been updated to remove any potential glitches generated during ring oscillator start-up. The new structure is able to reset the beat frequency counter when it enters the narrow (<0.1%) frequency measurement dead zone. This synthesizable version of the design with new modification does not affect the resolution of the original design. Results from a 65nm test chip shows that the circuit can detect even 0.01% frequency shift due to BTI aging. The open-source RTL codes and test bench are available for download at: https://github.com/reliability-research/odometer.

ACKNOWLEDGMENT

This work was supported in part by Semiconductor Research Corporation Task No. 2810.070 through the Texas Analog Center of Excellence (TxACE).

REFERENCES

[1] T. Kim, R. Persaud and C. H. Kim, "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits", IEEE Symposium on VLSI Circuits, June 2007.

[2] J. Keane, X. Wang, D. Persaud and C. H. Kim, "An All-in-One Silicon Odometer for Separately Monitoring HCI, BTI, and TDDB", IEEE Journal of Solid-State Circuits, vol. 45, issue. 4, April 2010.

[3] J. Keane, W. Zhang, C.H. Kim, "An Array-Based Odometer System for Statistically Significant Circuit Aging Characterization", IEEE Journal of Solid-State Circuits (JSSC), July 2011

[4] G. Park, H. Yu, M. Kim and C. H. Kim, "An All BTI (N-PBTI, N-NBTI, P-PBTI, P-NBTI) Odometer based on a Dual Power Rail Ring Oscillator Array", IEEE International Reliability Physics Symposium, March 2021.

[5] T. Grasser and B. Kaczer, "Evidence that two tightly coupled mechanisms are responsible for negative bias temperature instability in oxynitride MOSFETs", IEEE Trans. Electron Devices, vol. 56, no. 5, pp. 1056-1062, May 2009.