2021 VLSI TECHNOLOGY SYMPOSIUM KYOTO

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Electromigration-Induced Bit-Error-Rate Degradation of Interconnect Signal Paths Characterized from a 16nm Test Chip

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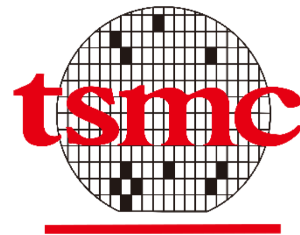
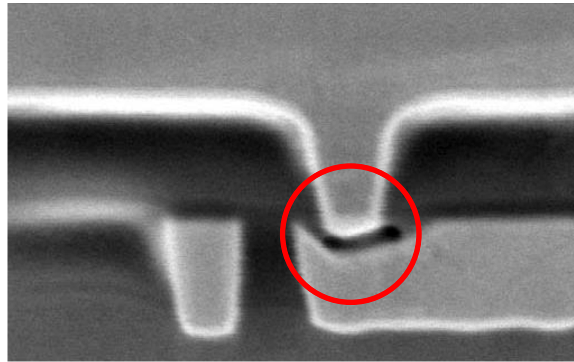


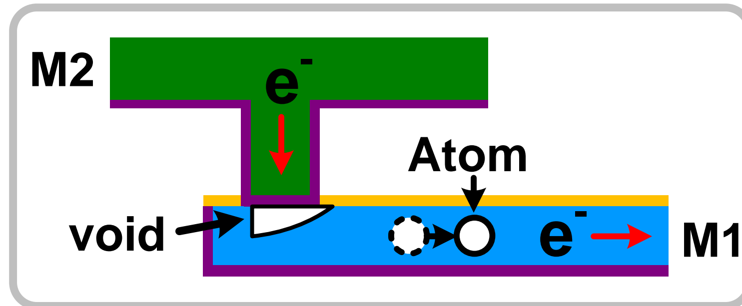
Outline

- Introduction
- Proposed BER-based EM Degradation Monitor
- Automated Testing Methodology
- Measured Results from the 16nm Test-Chip
- Conclusion

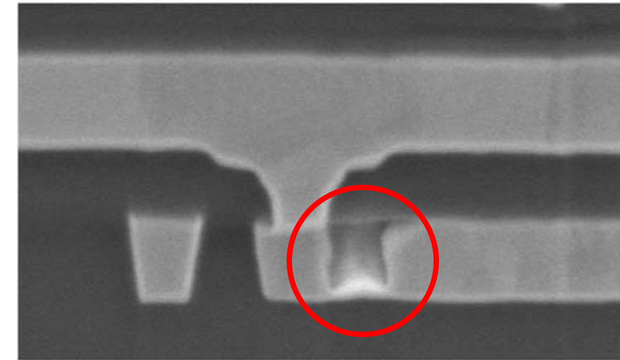
Electromigration In Interconnects

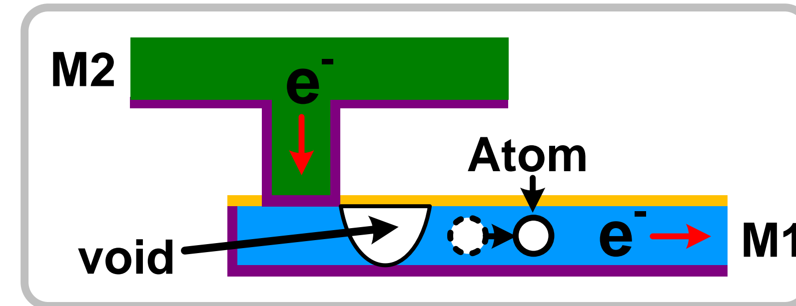
Abrupt failure





Progressive failure

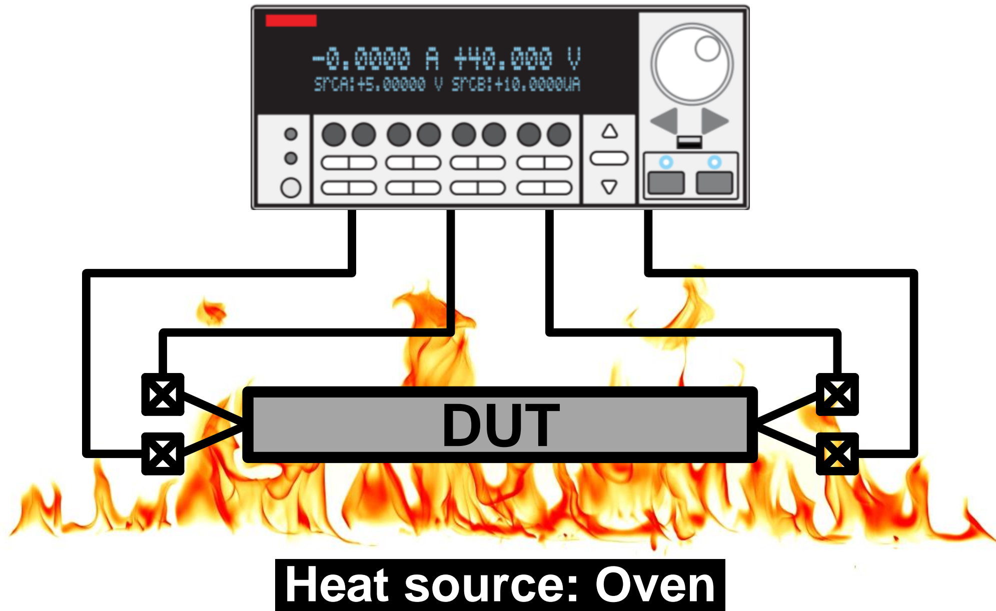




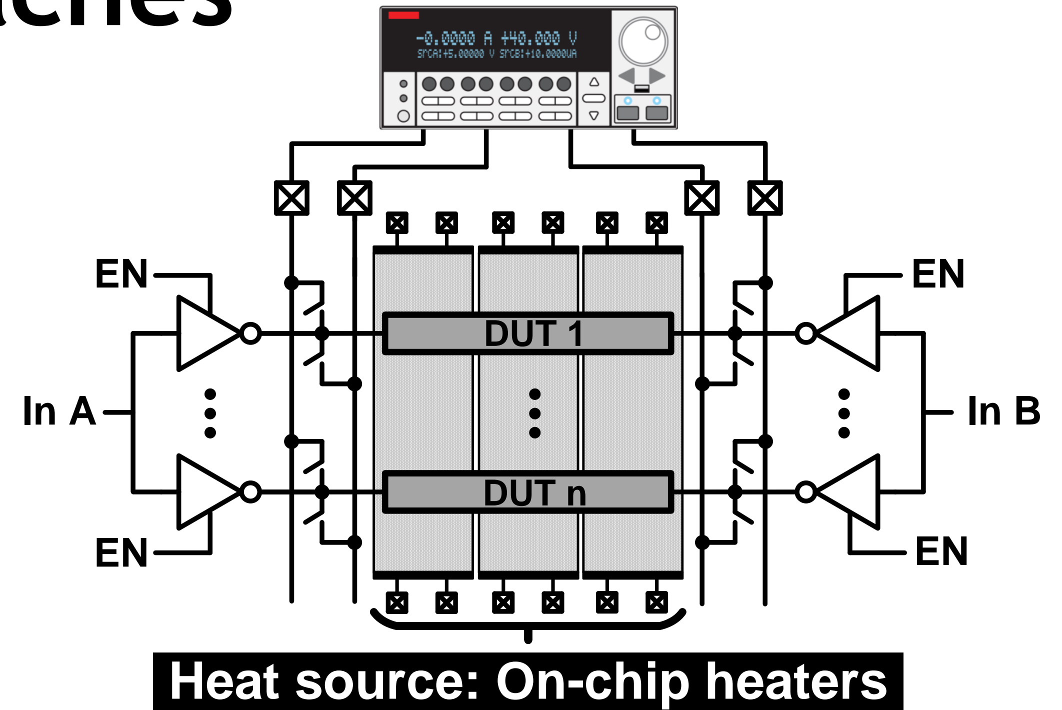
A.S. Oates, et al., TDMR, 2009

- EM is a function of current density, temperature and mechanical stresses
- Impact: Increased delay in signaling interconnects, IR drop in power grids

Prior Art: Resistance-based EM Tracking Approaches



Heat source: Oven



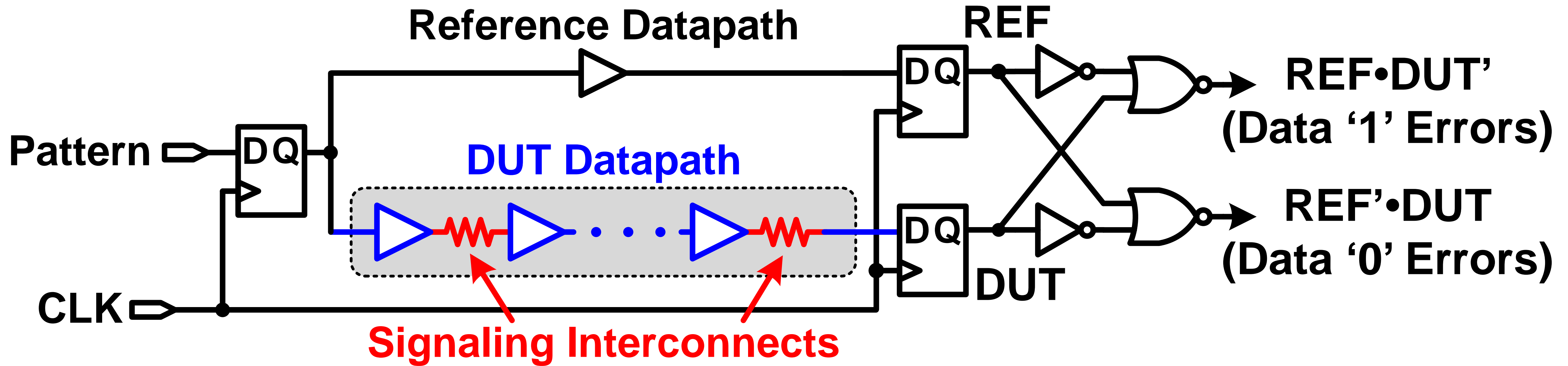
Heat source: On-chip heaters

- Large test area due to IO pads
- Long test time due to serial testing
- Extensive oven-based setup (300°C – 400°C)

- Small test area using array
- Short test time with parallel stress
- Simpler setup using on-chip heaters

N. Pande et. al., IEDM, 2019

Proposed Concept: BER-based EM Degradation Tracking



- Capture EM 'R' shifts directly in terms of degradation in the T-0 BER
- Relevant metric for quantifying the signaling capability of a datapath
- Digital-Intensive on-chip approach, featuring high precision bit-wise tracking

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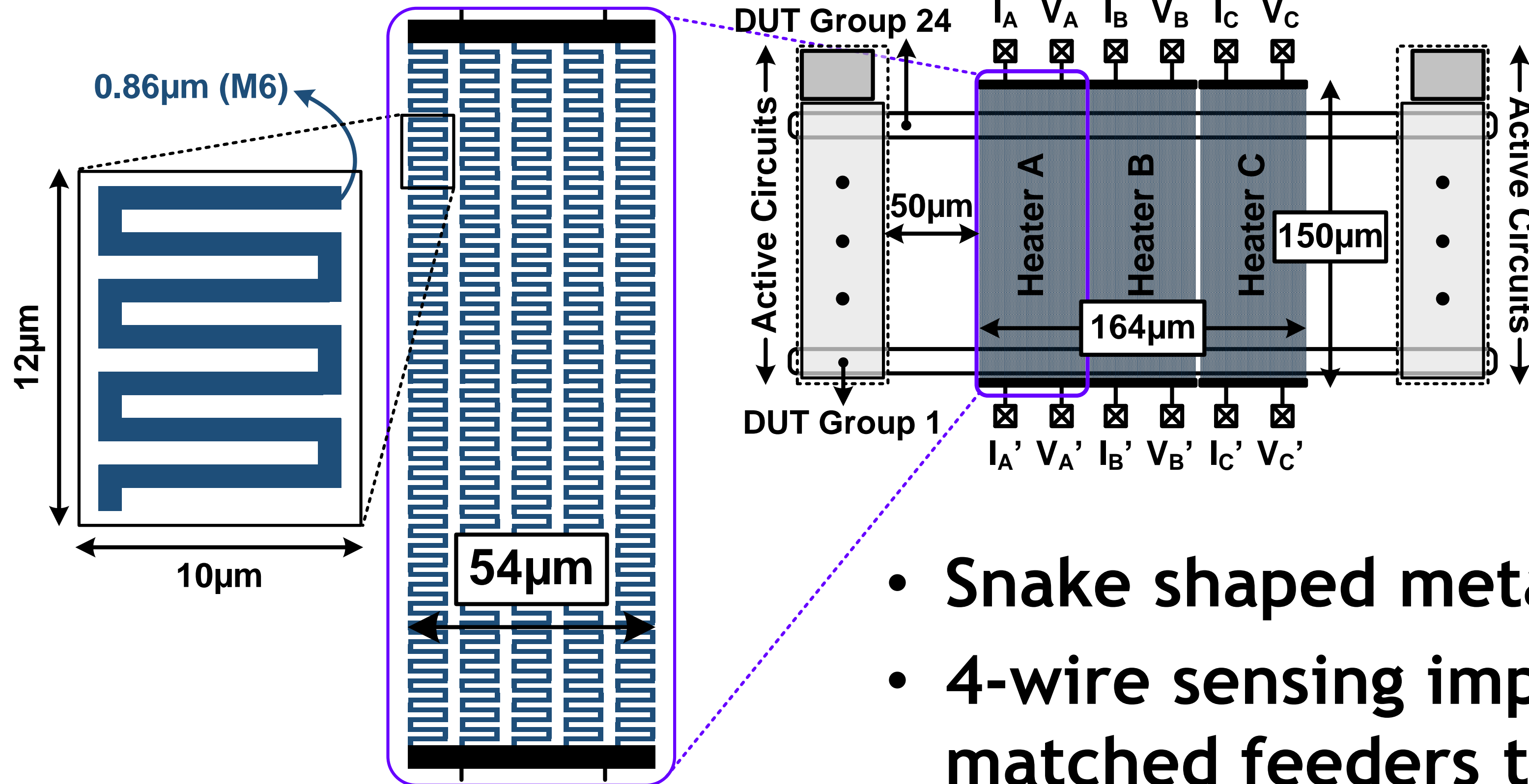
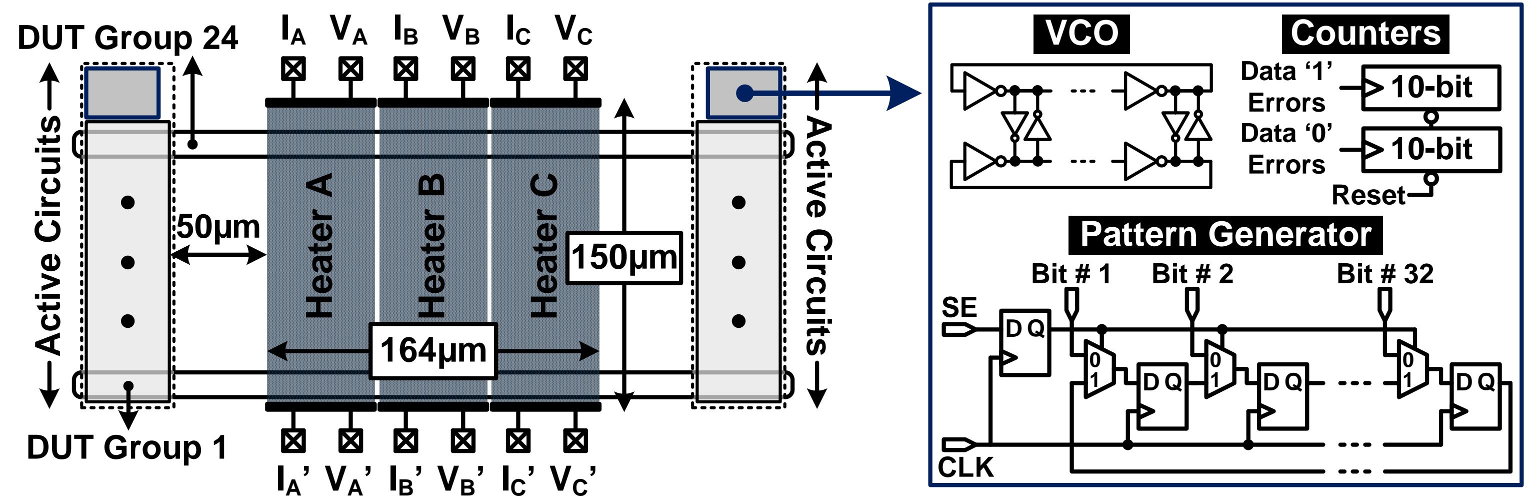
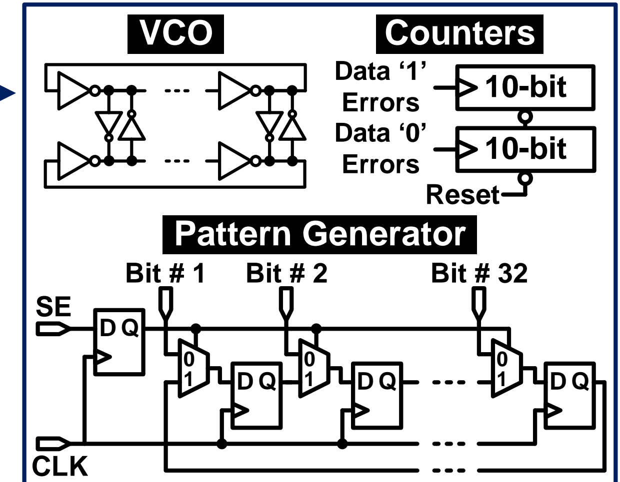
Test-Vehicle Overview



- Snake shaped metal heaters
- 4-wire sensing implemented with matched feeders to accurately track temperature in heating area

Test-Vehicle Overview

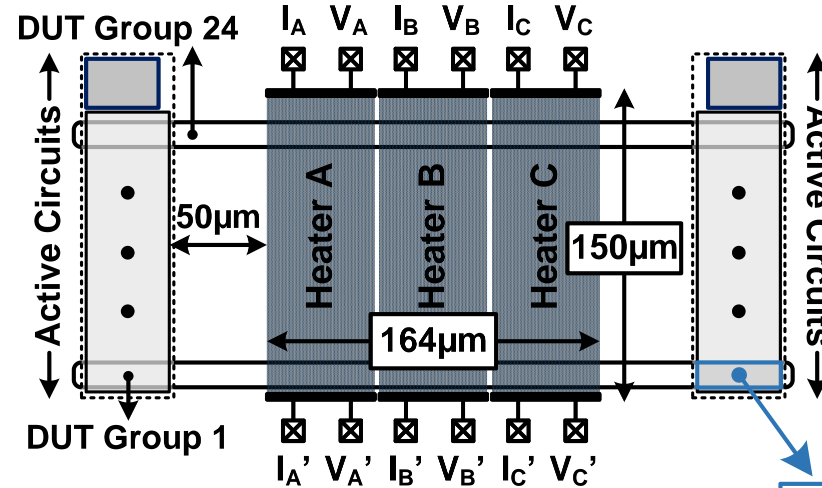


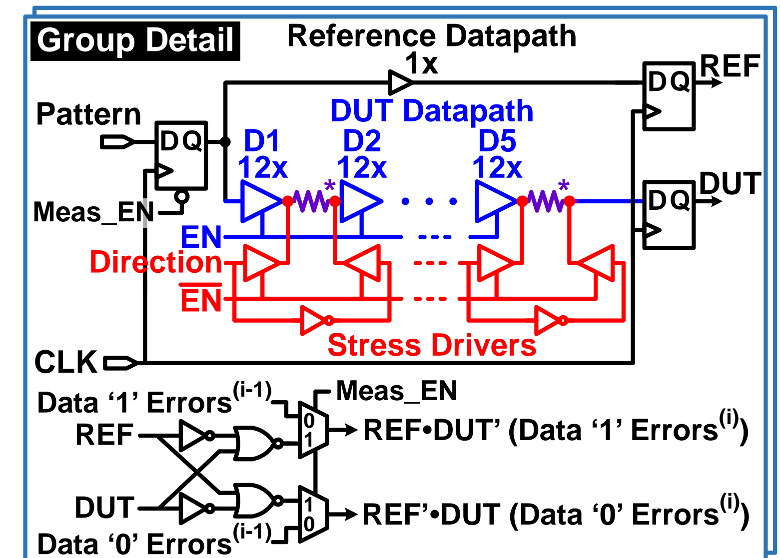


Measurement Top

- VCO: 7-stage, cross-coupled, supply tuned ROSC
- Pattern Generator: 32-bit circular-shift register with scan-based parallel load capability
- 10-bit asynchronous counters to accumulate bit '0' & bit '1' errors separately

Test-Vehicle Overview

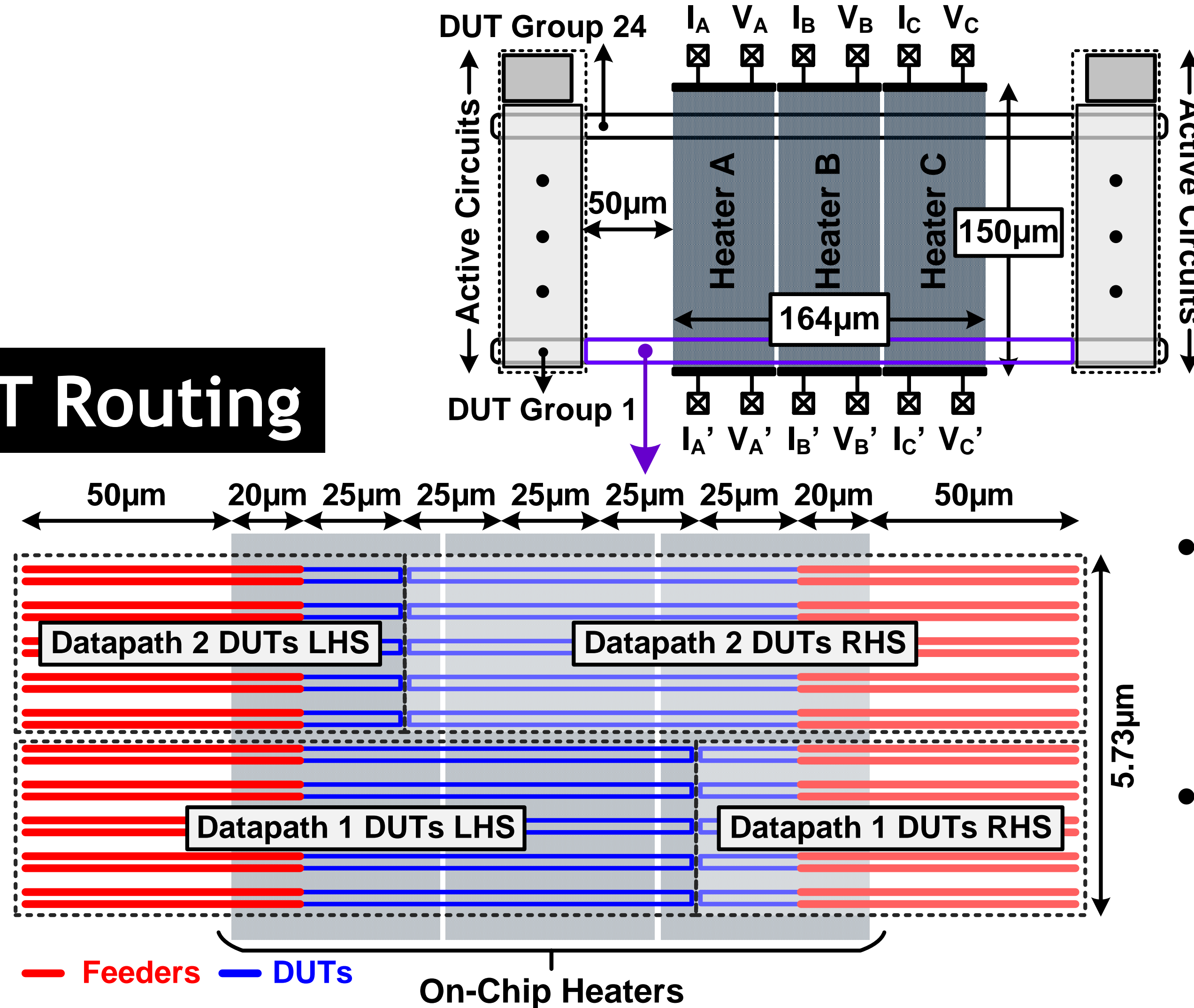




- Local sampling monitors separately track Data '0' & Data '1' bit-errors
- Errors from a selected group are routed to the measurement top

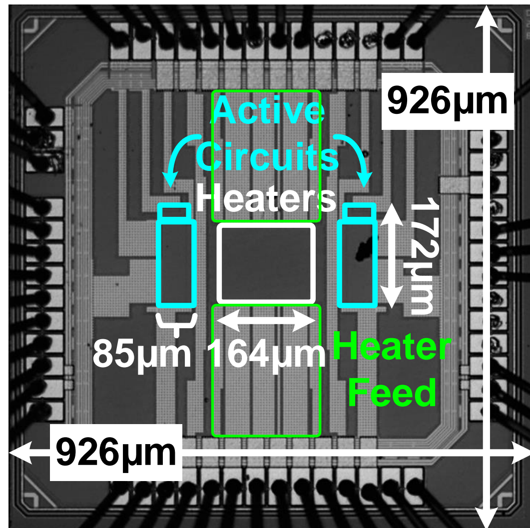
Test-Vehicle Overview

DUT Routing

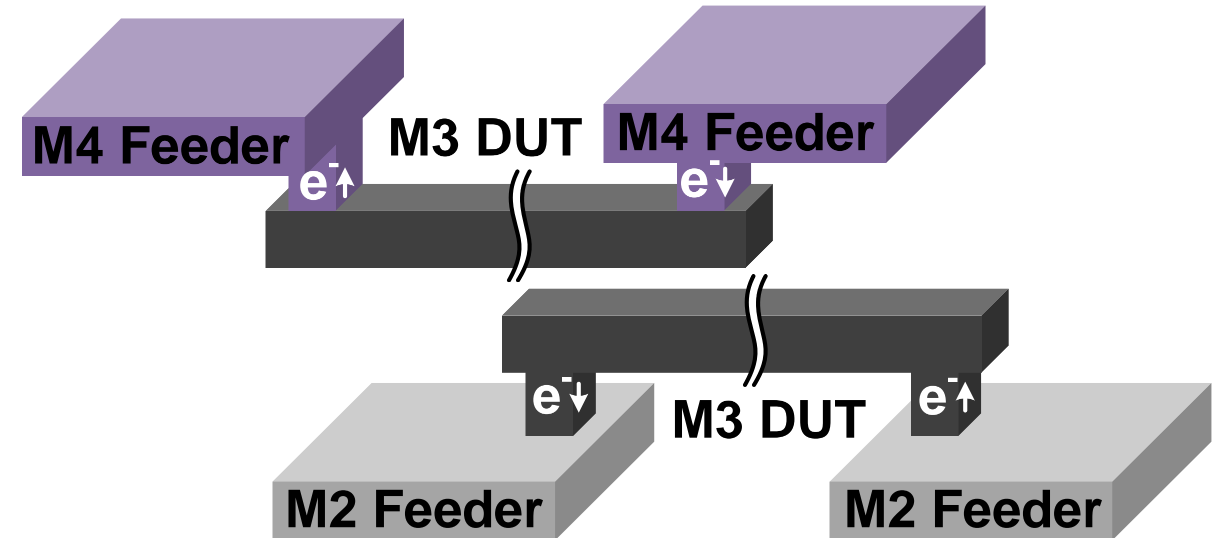


- DUTs folded & mirrored to maximize area utilization
- Routed with wide feeders to minimize IR drop

Implementation Summary



Process	16nm FinFET
Core, I/O VDD	0.8V, 1.8V
Chip Area	926μm x 926μm
Design Area	172μm x 435um
DUT Types	M4-M3, M2-M3
Wire Lengths	50, 100, 200μm
Wire Widths	Minimum
Datapaths / Chip	96 (x5 = 480 total wires)



- Chip Feature Summary
- Implemented EM test-structures

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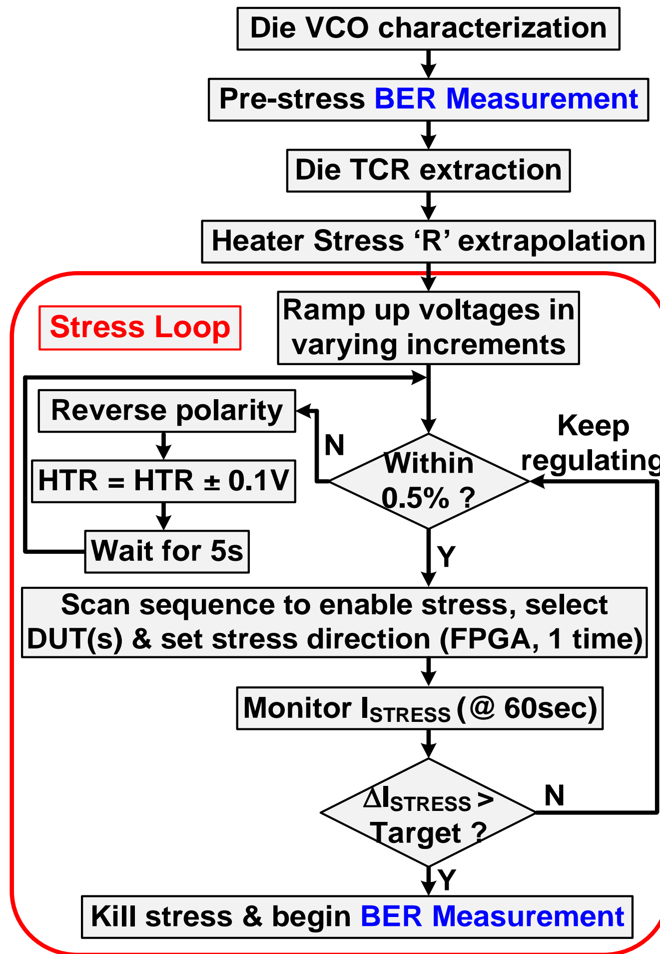
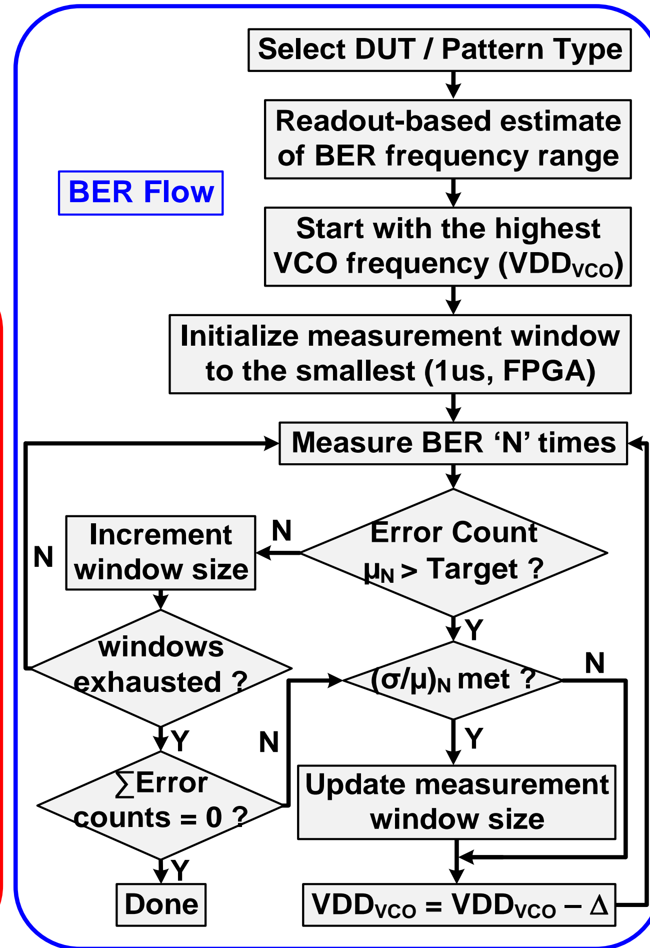
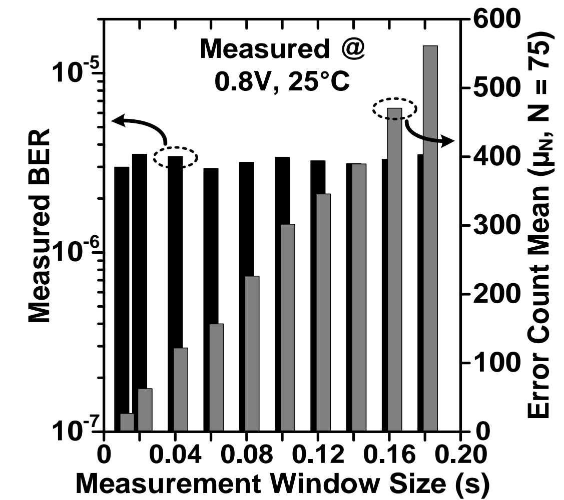
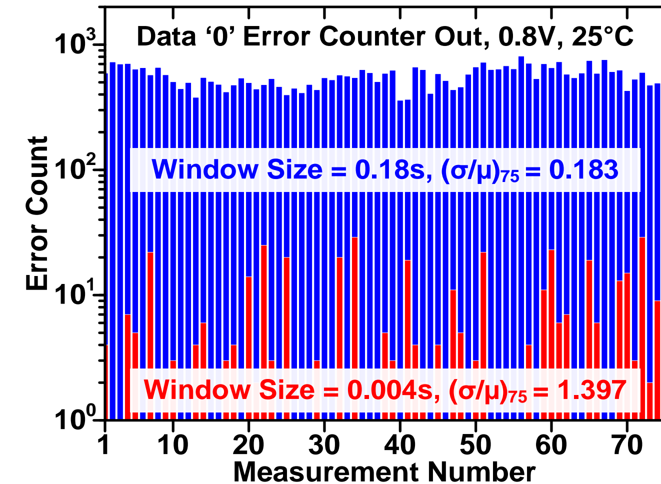
Measurement Methodology



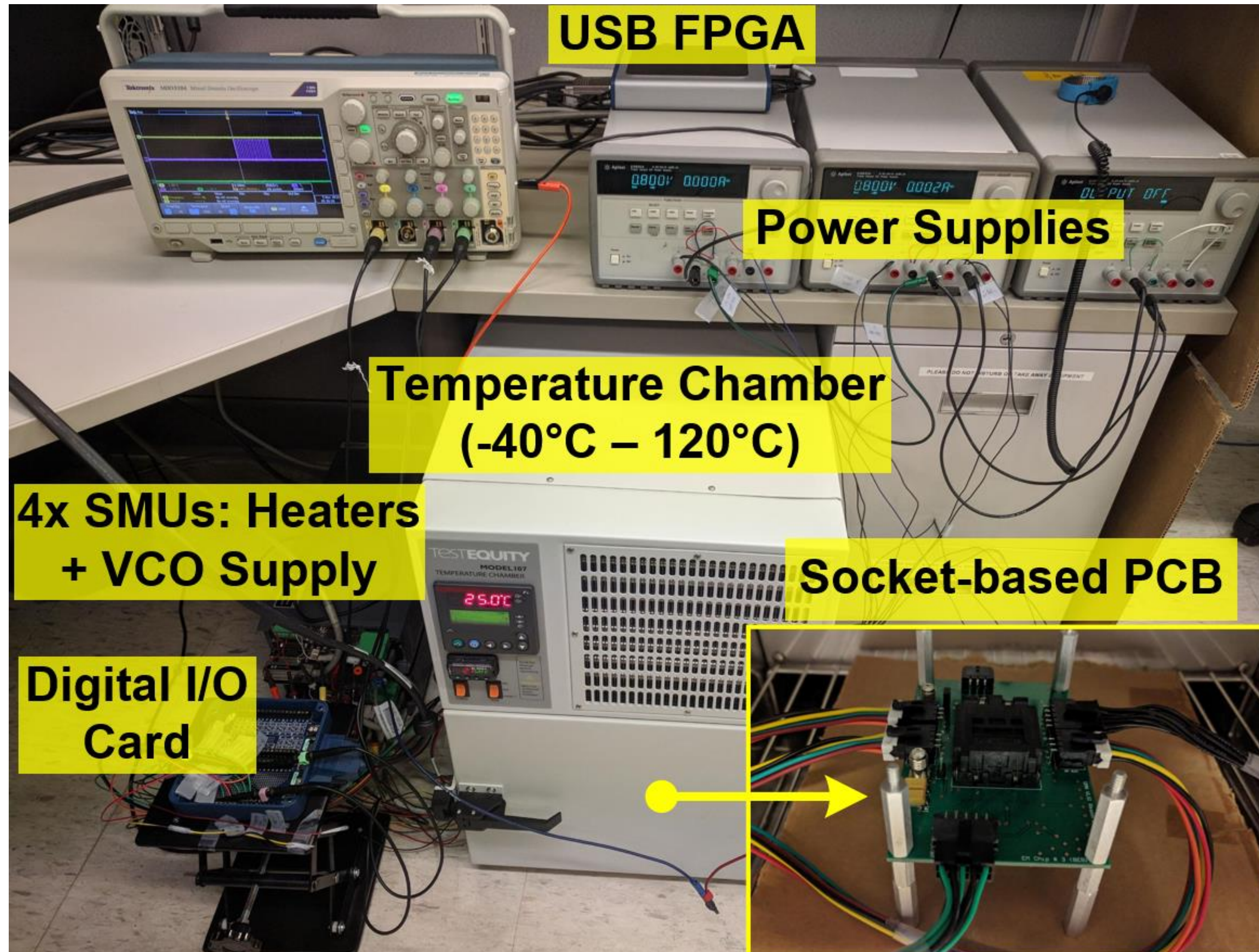






- Measurement Flow
- Measured BER Vs. Window size

Test Setup



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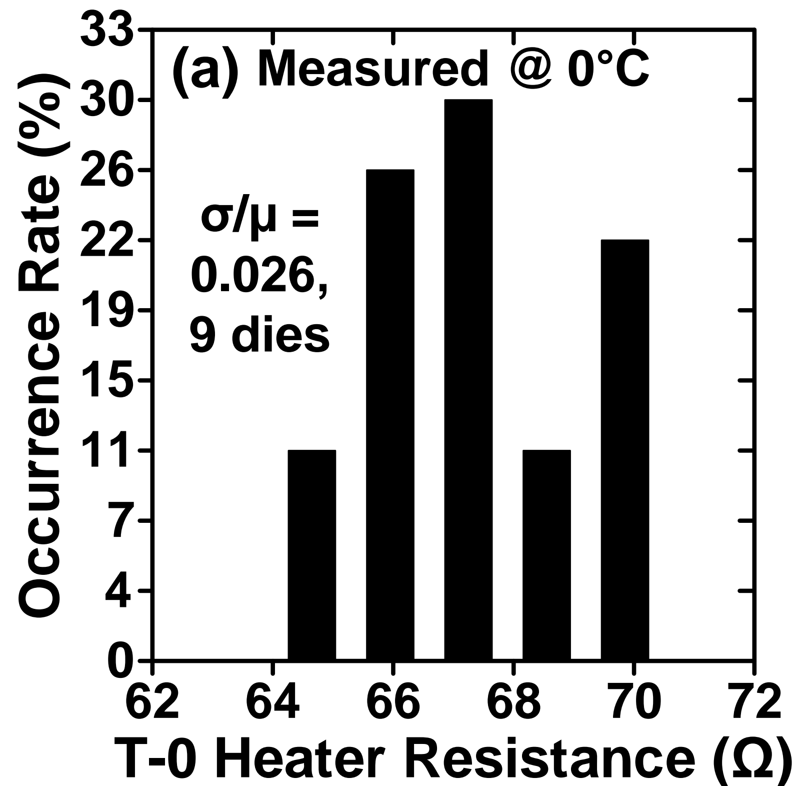
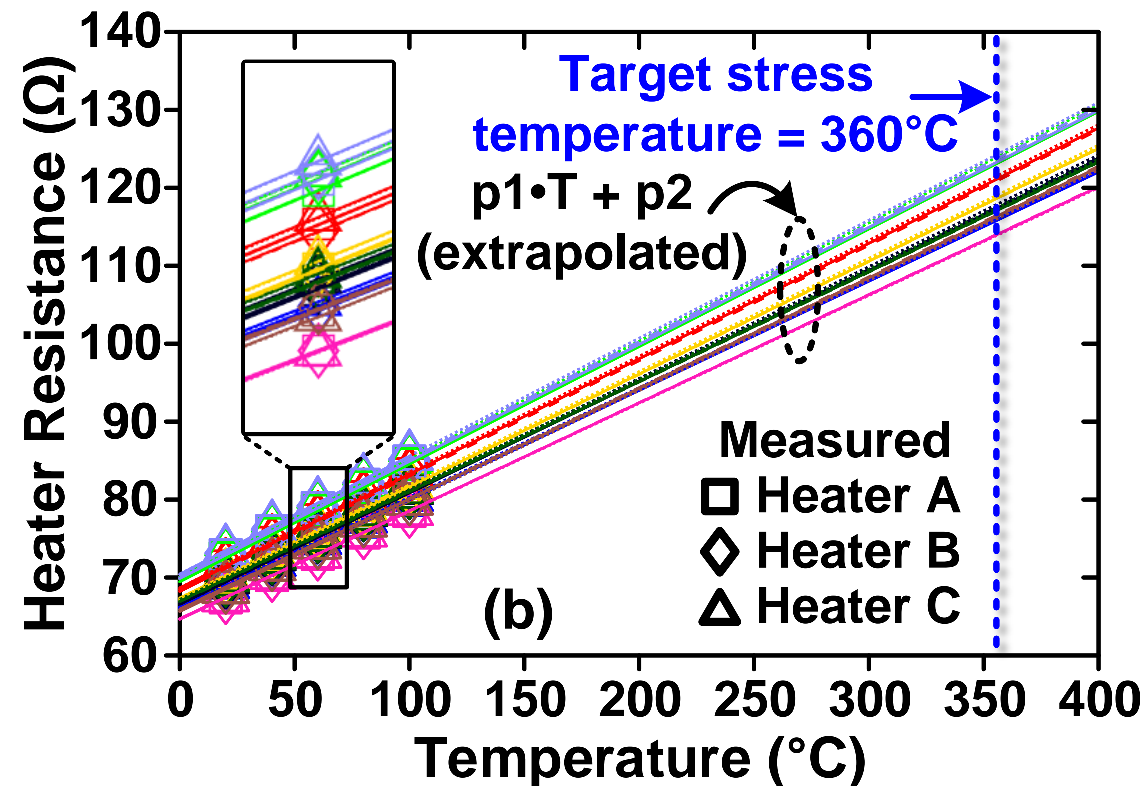
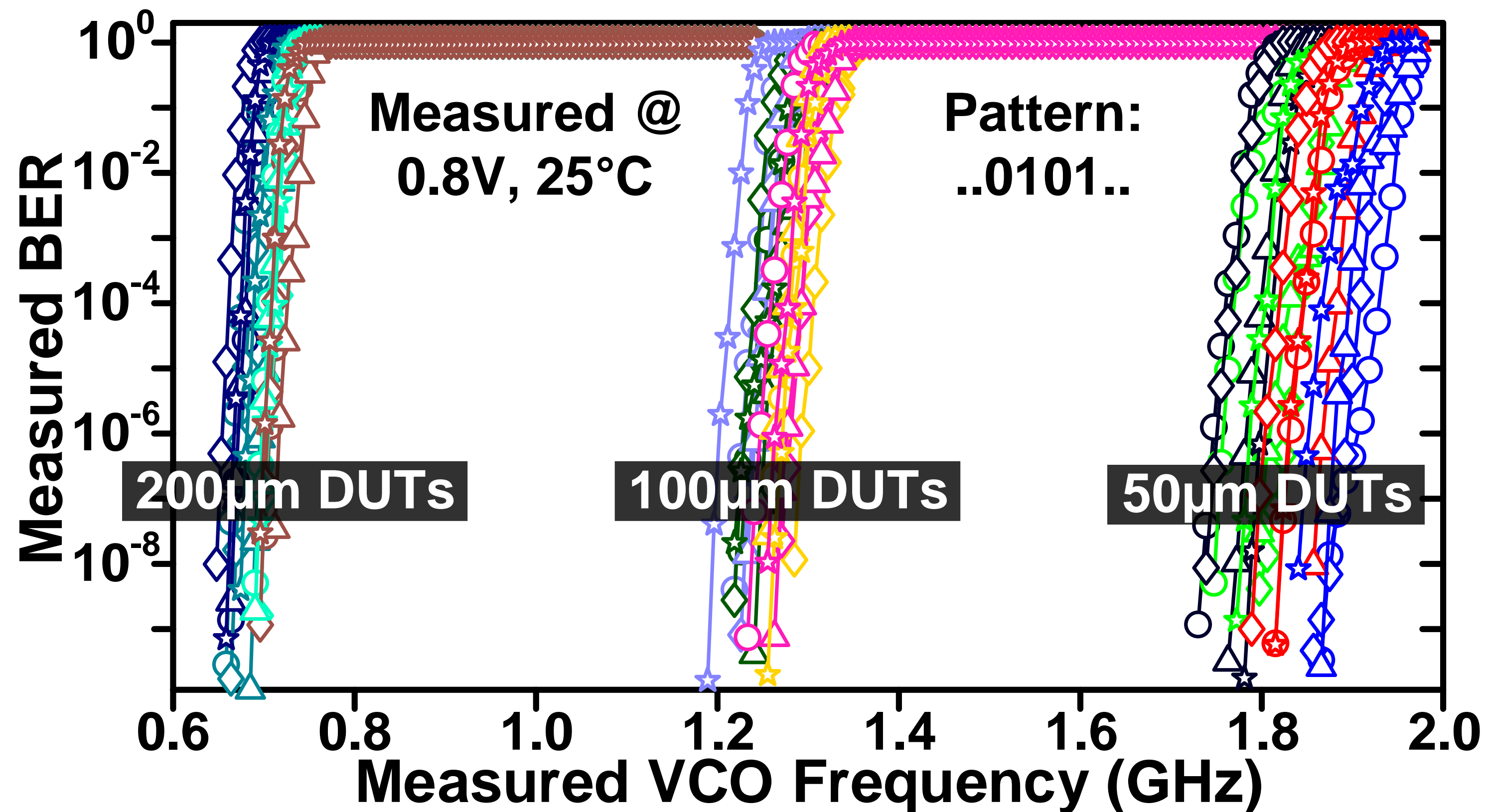
Heater TCR Characterization & Extrapolation





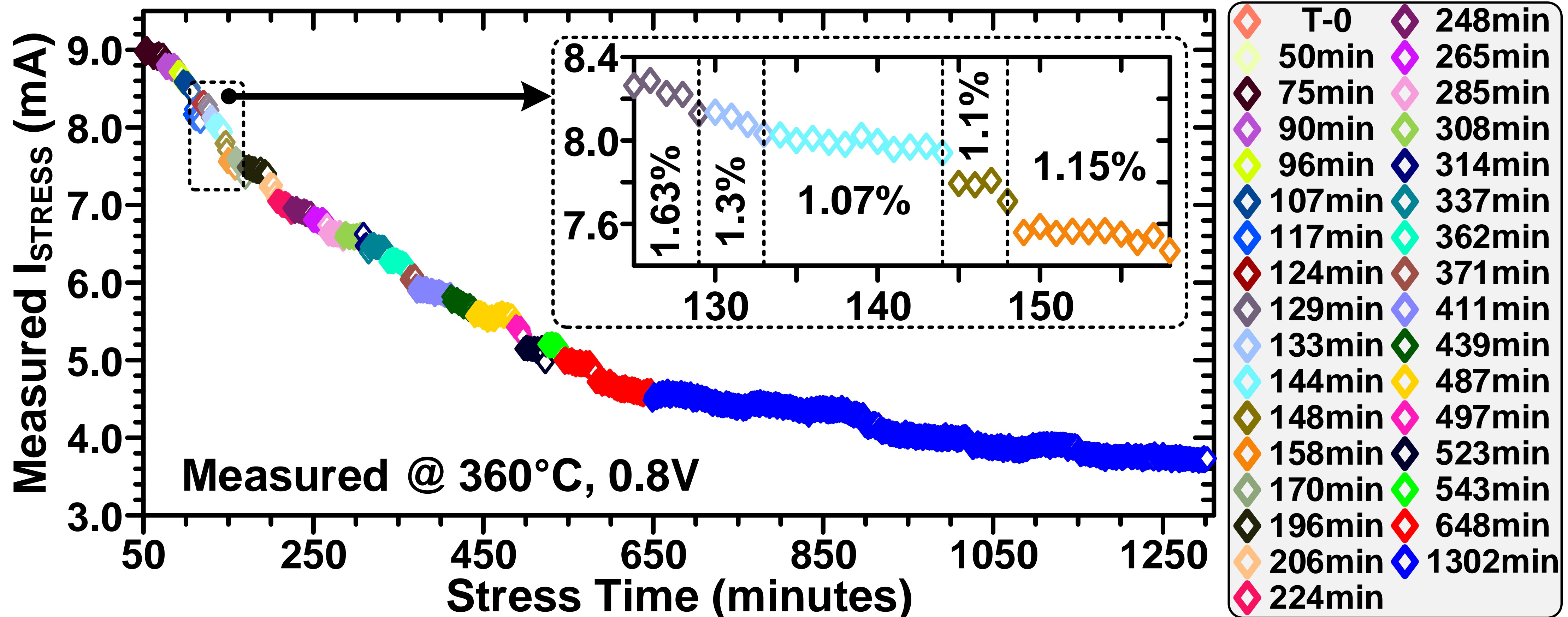
- TCR linearity allows accurate translation to target stress temperature: 360°C, for this work

T-0 BER Characterization Of Fresh Datapaths



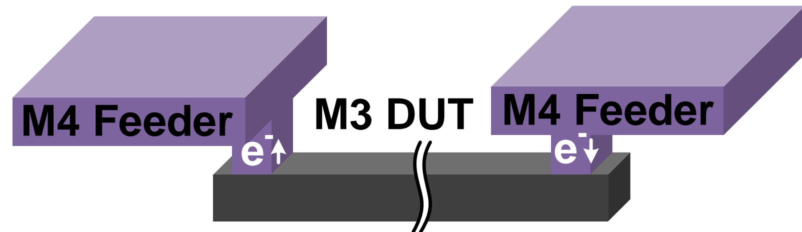
- BER saturates at lower frequencies for interconnect paths with longer lengths

Stress Experiment: Measured I_{STRESS} Degradation



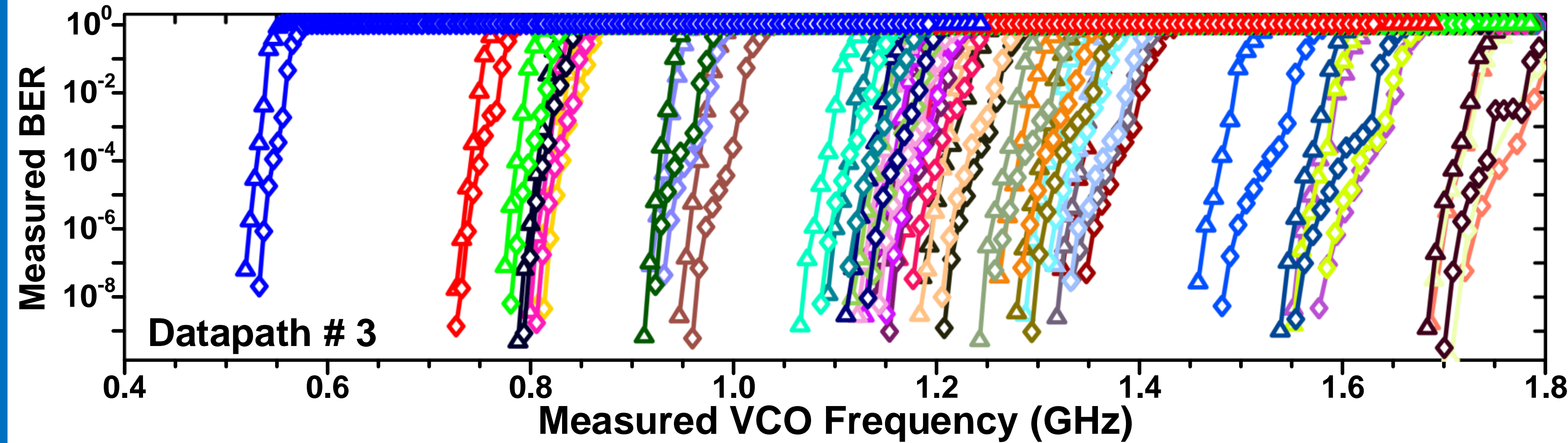
- 1-1.5% shifts are monitored per stress cycle (expect the final two)

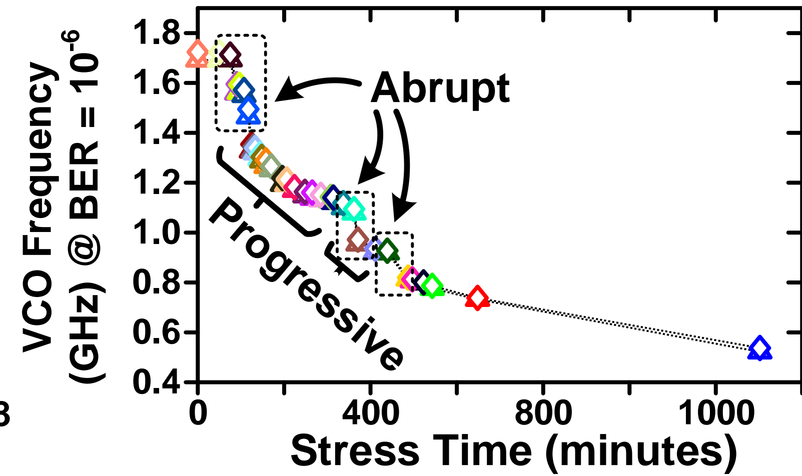
Stress Experiment: Measured Results



△ Data '0' ◇ Data '1'

50µm M4-M3-M4 Datapaths, Stressed @ 360°C, Measured @ 25°C

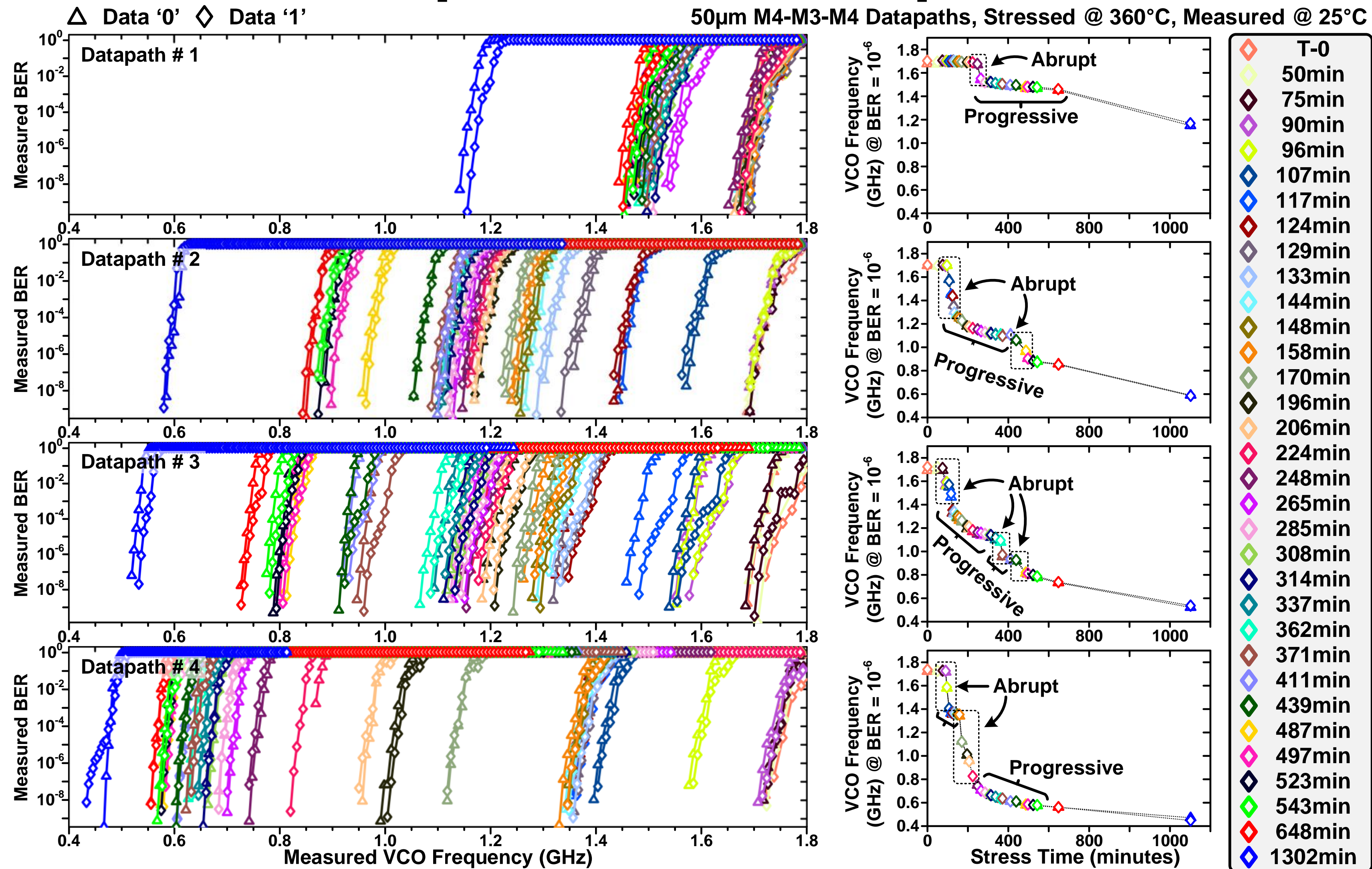




T-0 | 50min | 75min | 90min | 96min | 107min | 117min | 124min | 129min | 133min | 144min | 148min
158min | 170min | 196min | 206min | 224min | 248min | 265min | 285min | 308min | 314min | 337min | 362min
371min | 411min | 439min | 487min | 497min | 523min | 543min | 648min | 1302min

- Test-chip data captures both progressive & abrupt resistance-shift signatures in terms of the measured BER

BER Characterized from four independent datapaths



Conclusions

- The BER of an interconnect-path is proposed as a new metric for capturing EM-induced resistance-shift signatures
- A fully-digital hardware monitor featuring on-chip heaters, stress drivers & local sampling circuits for separately tracking Data ‘0’ & Data ‘1’ errors was implemented in a 16nm FinFET process
- Abrupt & progressive resistance-shift signatures were distinctly captured in terms of the measured BER