

Electromigration-Induced Bit-Error-Rate Degradation of Interconnect Signal Paths Characterized from a 16nm Test Chip

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Abstract

An array-based test-vehicle for tracking bit-error-rate (BER) degradation of signal interconnects subject to DC electromigration (EM) stress was implemented in a 16nm FinFET process. A unit interconnect path comprises five identical interconnect stages where each wire is driven by inverter based buffers. Accelerated EM stress testing is achieved entirely on-chip using metal heaters located directly above the devices-under-test (DUTs) and separate stress circuits driving both ends of the wire. BER measurement results from four individual interconnect paths are presented and analyzed. **Keywords:** Bit-Error-Rate, Circuit reliability, Datapath, Electromigration, Signal-Interconnects.

Introduction

This paper reports for the first time, the impact of EM on the BER of a signal interconnect path using a dedicated array-based test vehicle. Traditionally, single wire based DUTs have been used to characterize EM lifetime where the resistance shift is monitored under elevated temperatures, with either a constant stress current or a constant stress voltage. In contrast, the proposed test structure employs a number of novel on-chip monitoring circuit techniques including on-chip heaters, a bit pattern generator, and an on-chip BER monitor to simplify the overall test setup and allow high precision characterization of EM induced frequency shifts using standard circuits. Measurement data collected from a 16nm test chip reveals unique insights into EM induced signal path degradation.

BER-based EM Degradation Monitor Design

Fig. 1 presents an overview of the proposed test-chip architecture detailing the on-chip metal heater and the interconnects comprising the datapath routed underneath it as in [1], together with the error sampling monitors local to a group and the measurement circuitry specifics. Fig. 1(b) presents the measurement circuitry housing the clock and pattern generator, together with the 10-bit counters for separately accumulating the incoming locally sampled errors, corresponding to data '0' and data '1', for a selected datapath in the array. The clock generator is a voltage-controlled-oscillator (VCO), whereas the pattern generator is implemented as a 32-bit circular shift-register, with a scan-based parallel load capability. The DUT groups consist of two separate datapaths per array, each further consisting of five identical stages comprising a tri-state buffer driving an identical flavor of interconnect per stage. Fig. 1(c) illustrates the layout details for one such DUT group. The BER sampling circuitry local to a datapath (Fig. 1(d)) consists of a reference datapath comprising a signal buffer, along with the actual datapath consisting of the 5 interconnect stages, both driven by the same incoming pattern sequence. Their outputs are then sampled on the next rising edge of the clock to generate the REF and DUT signals. To separately monitor data '1' and data '0' error rates, we perform REF•DUT' and REF'•DUT logic operations which increment the two 10-bit counters, respectively. The interconnects are DC stressed using separate

tri-state stress drivers placed at both ends of the DUTs, with programmable control to allow for a unidirectional current flow in the desired polarity for stressing the DUTs. Fig. 2 shows the M4-M3-M4 and M2-M3-M2 DUTs with lengths of 50 μ m, 100 μ m, and 200 μ m implemented in the chip, along with the chip measurement setup.

Measurement Results from 16nm Test-Chip

Fig. 3 presents the extracted TCR of the on-chip heaters from 9 dies, showcasing the excellent linearity in the measured TCR, as well as the extrapolation to target stress temperature (360°C). Fig. 4 presents the fresh BER measurements corresponding to a total of 24 datapaths, in varying flavors of interconnect lengths and metal stacks, characterized using a pattern sequence with alternating '0's and '1's. As expected, the BER curves saturate at lower VCO frequencies for longer interconnects. Fig. 5 presents the measured BER results corresponding to patterns with differing numbers of consecutive '0's / '1's, performed as a sanity check on the same 50 μ m M4-M3-M4 datapath. The BER saturates at a level that corresponds to the ratio between the number of 0-to-1 or 1-to-0 transitions and the total number of bits transmitted.

For the stress experiments, we have chosen the pattern with alternating '0's and '1's. A total of 8 datapaths, comprising only the 50 μ m M4-M3 interconnects, are stressed in parallel, with stress current flowing from the receiver end to the driver end of the wire. The 40 wire DUTs are stressed while elevating the heater temperature to 360°C. Fig. 7(a) presents the degradation in stress current I_{STRESS} over the experiment duration, as a consequence of the EM induced DUT resistance degradation over time. Fine shifts in I_{STRESS} , with the threshold set between 1-1.5% are monitored per stress cycle except for the final two, after which, the VCO and datapath BER are re-characterized. Fig. 8 shows the BER characterization results from 4 independent datapaths, together with the degradation in path frequency for a BER = 10^{-6} as a function of the stress time. The BER curves remain relatively constant with no appreciable shifts for the first 96 to 248 minutes, depending on the datapath number. This represents the initial phase of EM where vacancies are moving towards receiver end of the wire. As the EM voids nucleate and grow, distinct abrupt and progressive failure signatures are observed over the experiment duration in different datapaths. For instance, datapath 1 exhibits a slow EM failure rate, with little to no degradation for the first 4 hours, followed by an abrupt shift and a slow progressive deterioration thereafter. In contrast, datapaths 2-4 exhibit a fast degradation over time, exhibiting distinctly evident fast abrupt shifts over the same stress time, followed finally by slow progressive degradation. It's also interesting to see that none of the datapaths completely failed even after extensive stress suggesting that low frequency functionality testing may not be effective in diagnosing EM-induced parametric shifts.

Acknowledgement: The data collection and analysis work was supported in part by Semiconductor Research Corporation (SRC).

Reference [1] N. Pande, IEDM, pp. 5.3.1-5.3.4, 2019.

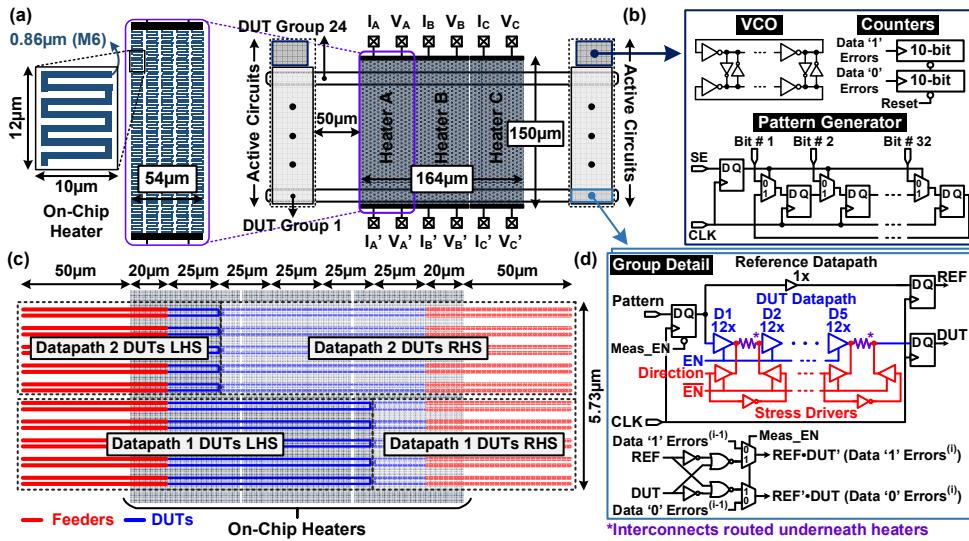


Fig. 1. (a) Overview of the 16nm EM induced BER shift characterization monitor and on-chip heater specifics; (b) Measurement circuit consisting of VCO, error counters, and 32-bit data pattern generator; (c) Datapath routing details comprising one DUT group underneath the heating area; (d) Unit tileable DUT group details: Reference and DUT datapaths, with separate error counters for data '0' and data '1'

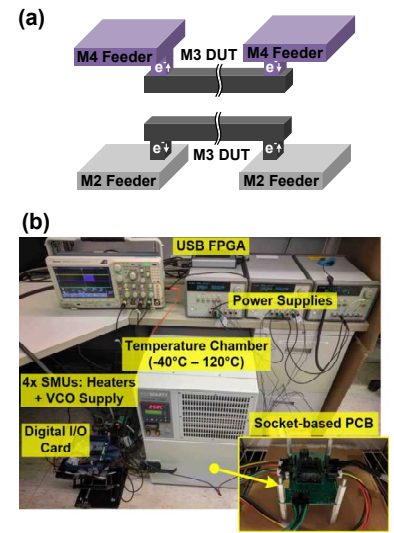


Fig. 2. (a) Implemented metal test structure specifics; (b) measurement setup.

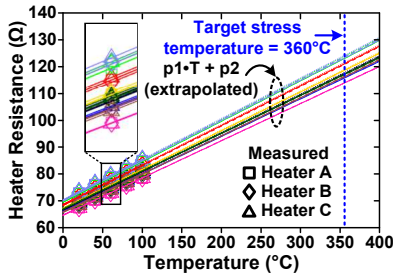


Fig. 3. Heater TCR characterization.

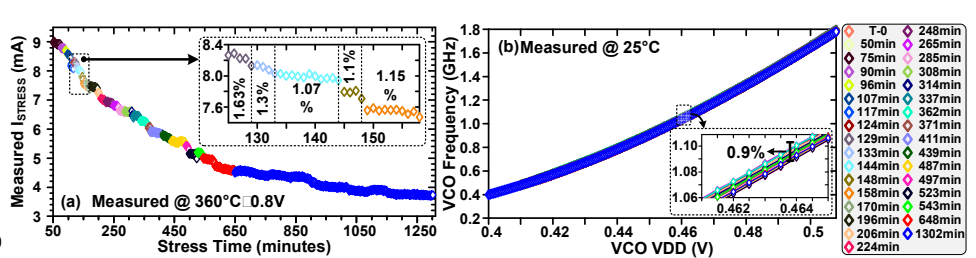


Fig. 7. (a) Measured stress current (I_{STRESS}) degradation; (b) Measured VCO performance.

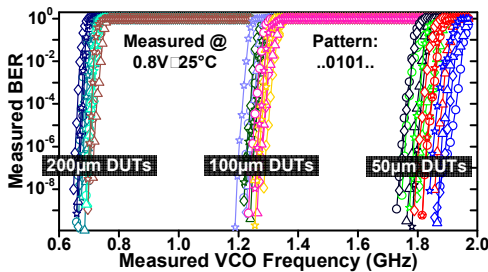


Fig. 4. Fresh BER characterization.

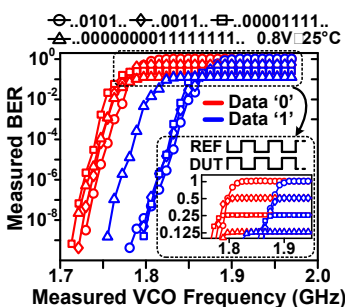


Fig. 5. BER sanity check.

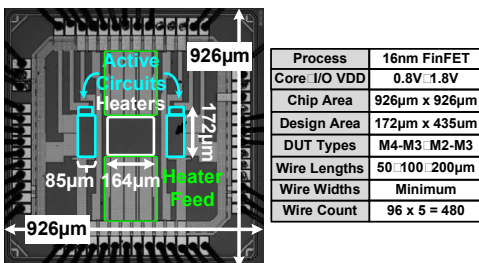


Fig. 6. Die photo and chip feature summary.

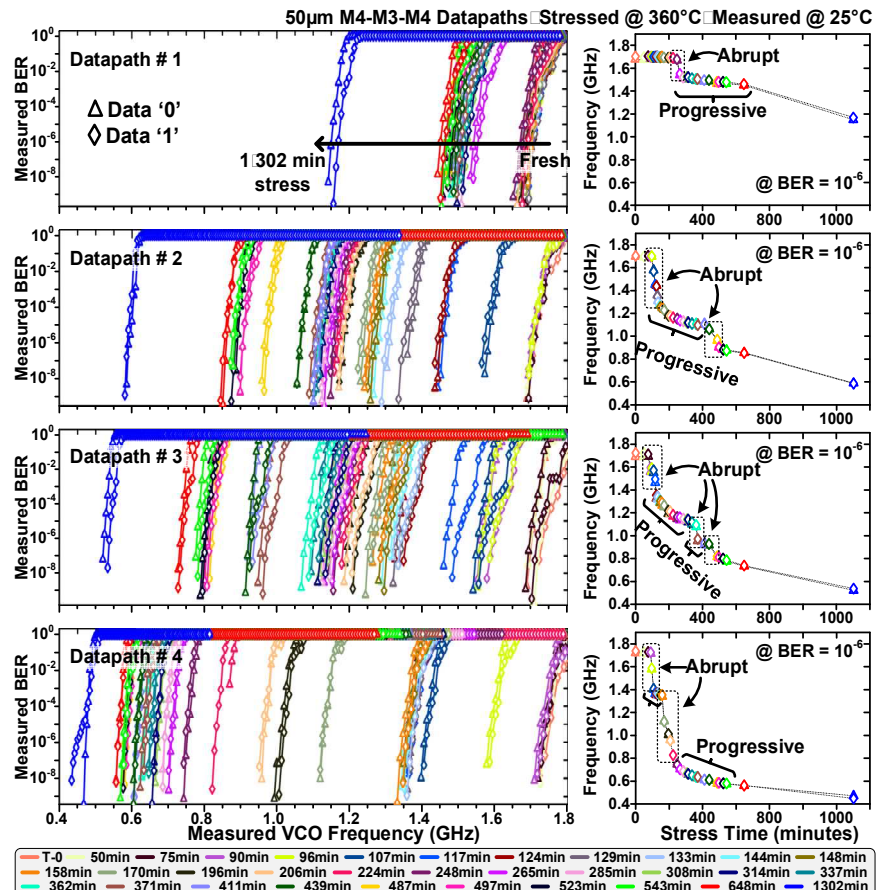


Fig. 8. (Left) Measured shift in BER captured over a 1,302 minute stress period. (Right) Degradation in path frequency vs. stress time for a BER of 10^{-6} .