A Back-Sampling Chain Technique for Accelerated Detection, Characterization, and Reconstruction of Radiation-Induced Transient Pulses

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***Abstract*— Accurate characterization of radiation-induced soft errors is a critical step toward understanding the impact of these glitches on circuit and system reliability. With process scaling, there has been exponential increase in number of transistors that can be packed on a die which, in turn, results in higher sensitive node count and persistent soft error susceptibilities. In this work, a novel circuit technique employing higher sensitivity toward soft errors is proposed. The circuit makes use of current-starved gates with bias knobs to fine-tune both measurement resolution and strike sensitivity enabling accelerated and efficient induction of errors in a limited-time irradiation test environment. The back-sampling chain (BSC) circuit can measure individual radiation-induced transient pulse with as low amplitude as 0.3 × VDD while maintaining a high measurement resolution for pulsewidth characterization. The bias knobs allowing tuning of sensitivity and resolution enable, for the first time, a strike pulse waveform reconstruction methodology that can be used to calibrate current pulse models for assessing soft error rate (SER) sensitivity of standard logic gates.**

***Index Terms*— Back-sampling, FinFET, multi-bit upset (MBU), neutron irradiation, radiation strike, single event transient (SET), single event upset (SEU), soft error rate (SER).**

I. Introduction

With process scaling, integrated circuits have shown tremendous resiliency against radiation-induced events [1]–[5]. Scaling down of device feature size has resulted in lower charge collected by each junction, leading to a lower per transistor soft error rate (SER) with new technology nodes. Introduction of FinFET technology has changed the device architecture with elevated 3-D junction structures (Fig. 1). This has led to further reduction of SER due to a more constrained path for the charge to get collected [6], [7]. Even within FinFET technology, with further scaling, the fins have become narrower and taller, as shown in Fig. 1, which leads to even more constrained path for the charge to travel and get collected at the junction to induce an error.

Despite the steady decrease in per-transistor SER, the exponential increase in the number of transistors per chip may cause the chip-level SER to increase with scaling. Moreover, the lower operating voltage coupled with dynamic voltage scaling capabilities can make the system more susceptible to radiation-induced strikes depending on the operating conditions. Radiation-induced SER, especially in logic circuits, flip-flops, and memory arrays in advanced CMOS process, can pose significant reliability challenges for mission critical applications such as finance, transportation, military, space, biomedical, Internet of Things, and so on. Hence, SER remains a critical reliability issue that needs to be addressed in any new technology.

Previous works [8]–[12] have shown standard logic chains implemented, wherein a time-to-digital converter (TDC) circuit at the end of the chain is used for pulsewidth measurements (Fig. 2). In this case, using a long propagation path may induce pulsewidth modulation effects resulting in distorted results [13]. Moreover, standard gates are not sensitive enough for statistical data collection during the limited beam time. While using lower VDD values can increase the sensitivity, both the restore current and capacitance change so the circuit behavior at the nominal VDD may be hard to predict. In another work [14], a pulse shrinking chain with local sampling was used to capture and measure single event transient (SET) pulsewidth (Fig. 2). This is an elegant approach; however, the skewed gates used for pulse shrinking lower the SER sensitivity which adversely impacts the amount of data collected during the limited beam time.

Hence, an ideal SER characterization circuit must satisfy several requirements, including high sensitivity to radiation strikes, tunable sensitivity, a scalable architecture, and a uniform layout. In addition, it needs to support an SER characterization methodology that can use an analytical model

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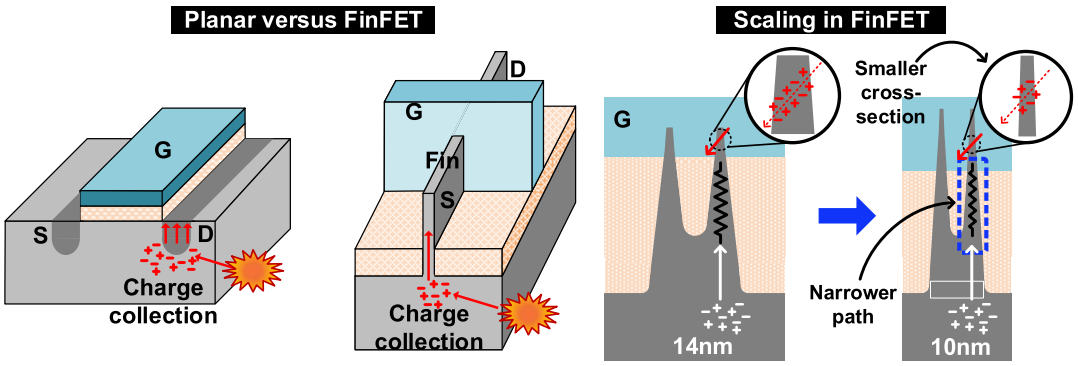


Fig. 1. Illustration showing radiation strike in planar and FinFET devices [13] (left). Reduced junction area and constricted fin structure in FinFET devices result in lower SER. Fin scaling impact on SER (right). Taller and narrower fins make the charge collection more difficult and, hence, lower the SER.

to predict SER susceptibility for any given circuit topology in the same process technology. While prior works [16]–[18] have, in parts, addressed few of these issues by proposing new detection circuits and a basis for a simulation framework, a comprehensive SER analysis framework is required based on measured data collected from circuit-based SER detection.

In this article, we propose a novel back-sampling chain (BSC) circuit technique that can meet the above listed requirements. The BSC circuit can detect SET, single event upset (SEU), and multi-bit upset (MBU), simultaneously. Although the proposed circuit is not an exact representation of standard logic gates, it allows the strike current pulse to be reconstructed with the help of a suitable SER model and, hence, the data can be mapped on to any given generic circuit topology with high confidence.

The test chip was implemented in a 14-nm trigate technology with a nominal VDD of 0.7 and irradiated under a neutron beam at the Los Alamos National Laboratory (LANL), Los Alamos, NM, USA. SET pulsewidth measurements and flip-flop SER cross section results are presented that highlight various circuit parameters impacting SER. The BSC circuit applies tunable analog bias voltage knobs that control the sensitivity and resolution of the circuit toward strikes. This allows fine control over both pulsewidth resolution as well as sampling cutoffs or detection thresholds. The detection threshold and pulsewidth measurement resolution parameters are swept to enable a unique voltage pulse reconstruction of the originally induced SET pulse based on measured data. To the best of our knowledge, this is the first-time demonstration of individual SET voltage pulse reconstructed based on irradiation data. The conference version of this work was published in [15].

II. Current-Starved Inverter Chain

Fig. 2 shows the various circuit parameters that affect the critical charge (Q_{crit}) associated with a given circuit node. Q_{crit}, for SETs, is defined as the minimum amount of charge injected at device junction to induce a transient pulse propagation along the combinational chain. Restore current I_{restore}, node capacitance C_{node}, junction area J_{area}, and trip point of the next stage V_{SW} are the key circuit parameters that affect SER sensitivity. To enhance the sensitivity of the circuit to a

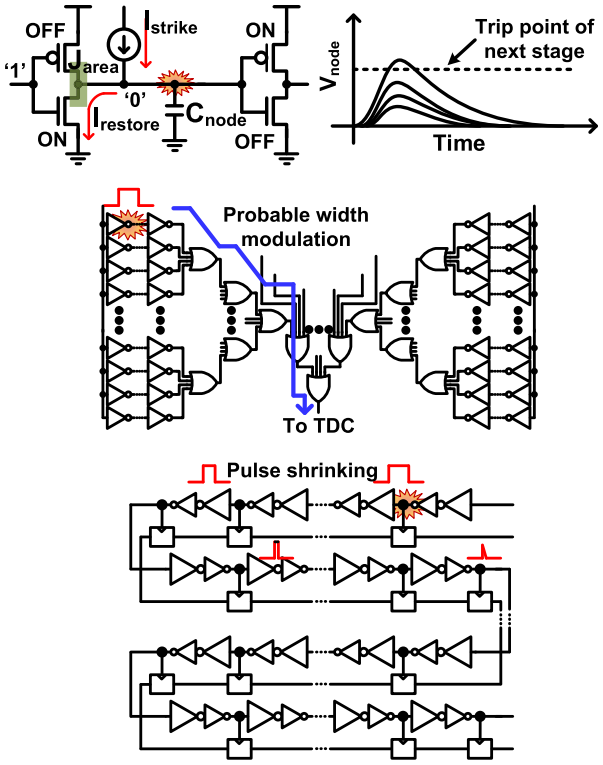


Fig. 2. Circuit parameters affecting SER in logic path (top). Previous radiation detection circuits [8], [14] are novel and elegant, but suffer from pulsewidth modulation effects and/or lower sensitivity to radiation strikes (middle and bottom).

radiation strike, we must reduce I_{restore} by making the drive current weaker, reduce C_{node}, increase J_{area}, and reduce V_{SW}.

In order to cater to these requirements, a chain of current-starved buffers is used in our design as the detection circuit. As illustrated in Fig. 3 (top), each buffer consists of a pair of current-starved inverters with additional NMOS and PMOS devices per stage that are used for biasing purpose. Gate terminals of the bias transistors are tied alternatively to separate analog voltages and can be used to fine-tune the amount of starving that needs to be applied to each individual inverter stage, thereby controlling the SER sensitivity. Applying alternate bias lowers both the restore current and the switching threshold of the next stage, thereby increasing the sensitivity of the sensor chain. As the PMOS bias voltage (V_{PE})

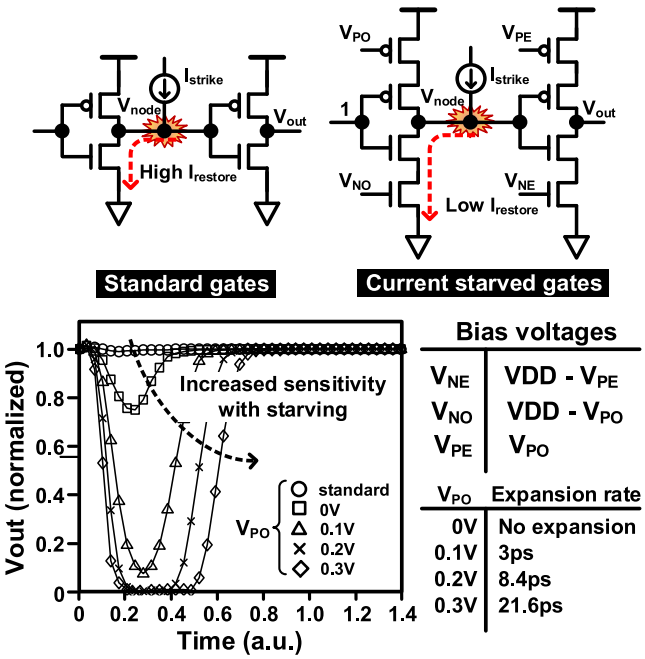


Fig. 3. Current-starved inverters exhibit higher SER sensitivity due to lower restore current ($I_{restore}$) and lower switching threshold voltage (V_{SW}).

is increased and corresponding NMOS bias voltage in alternate stage (V_{NO}) is reduced, the drive strength of the inverter pair reduces and skew increases resulting in increased sensitivity and pulse expansion.

To analyze the circuit sensitivity in the event of a radiation strike, an independent current source modeling the radiation current I_{strike} is used to inject charge at a given node (Fig. 3). The double exponential current transient model [19]–[21] was used with empirically chosen time constants and critical charge (Q_{crit}) values. More accurate FinFET current transient models are being developed, which could be adopted for future studies. Simulation results show that standard inverters are least sensitive toward the strike with no pulse propagation at the next stage node, while starved inverters exhibit higher sensitivity by detecting a strike pulse height as low as 28% of the supply voltage at 0.3 V. Also, as the starving is increased, sensitivity increases with the next stage pulses achieving an increased swing and a larger width. Fig. 4 shows simulation results for sensitivity comparison of current-starved chain and the standard buffer chain. The proposed circuit is able to achieve around 9× higher Q_{crit} sensitivity across multiple VDD points which will result in orders of magnitude higher number of SET strikes.

III. BSC Circuit

A previous pulsewidth measurement technique employed local sampling of the SET pulses, while the pulse shrinks along its propagation line [12]. Each output node of the buffer is connected to a flip-flop that samples the output node of each stage. Local sampling of the transient pulse eliminates any pulsewidth modulation that may occur when routing signals to a shared TDC [11], [14].

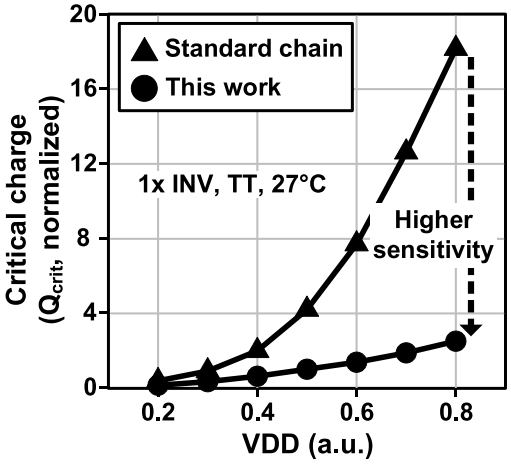


Fig. 4. Simulation plot showing critical charge (Q_{crit}) comparison of current-starved buffers chain with standard inverter chain with respect to supply voltage.

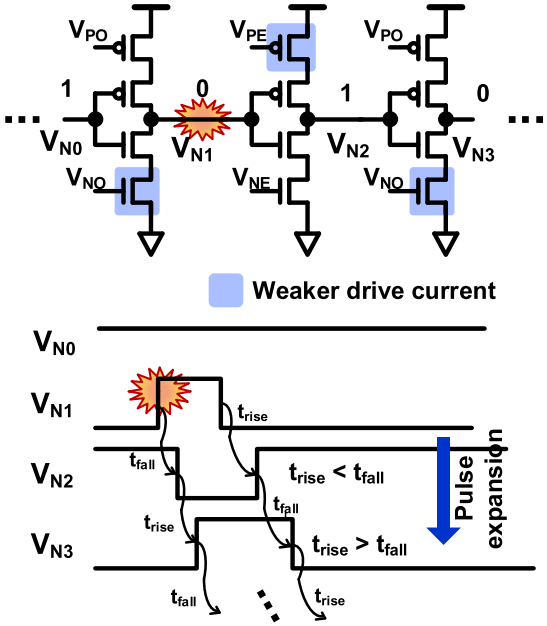


Fig. 5. Skewed current-starved inverters in the direction of increasing sensitivity result in pulsewidth expansion along the propagation path.

In order to increase the strike probability in the detection chain, in this work, the starving direction of current-starved buffers is maintained in favor of higher sensitivity by keeping $V_{PO} > V_{PE}$ and $V_{NO} > V_{NE}$. However, the direction of skew applied to raise sensitivity results in pulsewidth expansion as the transient propagates along the buffer chain, as illustrated in Fig. 5.

The associated pulse expansion prohibits use of the direct local sampling method for pulsewidth measurements proposed in [12]. Hence, we propose a novel BSC circuit technique which addresses this issue by measuring the strike pulsewidth by means of back-sampling previous stage falling edge using later stage rising edge. The strength of current starving determines the per stage pulse expansion rate (also refers to the pulsewidth measurement resolution). Alternate starving results

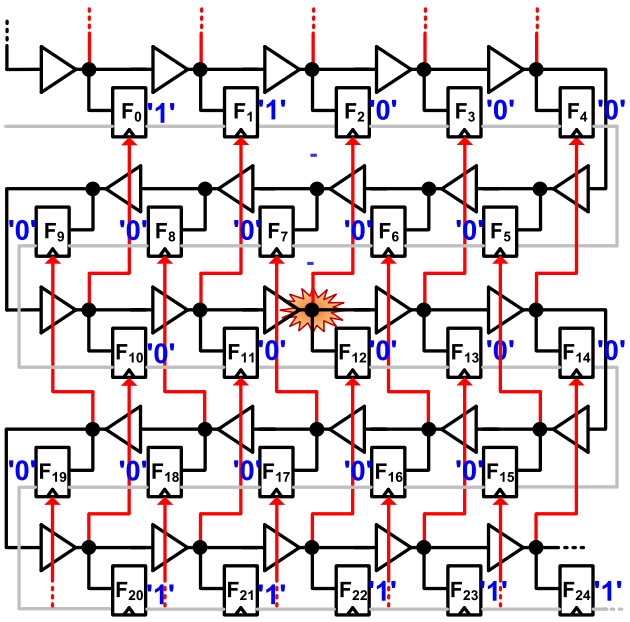


Fig. 6. BSC circuit with current-starved buffers and embedded local sampling flops. For the sake of simplicity, we omitted the input MUX in front of each flip-flop which can be seen in Fig. 10. During irradiation mode, the flip-flop inputs are connected to the buffer outputs, whereas in read out mode, the flip-flops are configured as a scan chain (grayed out path).

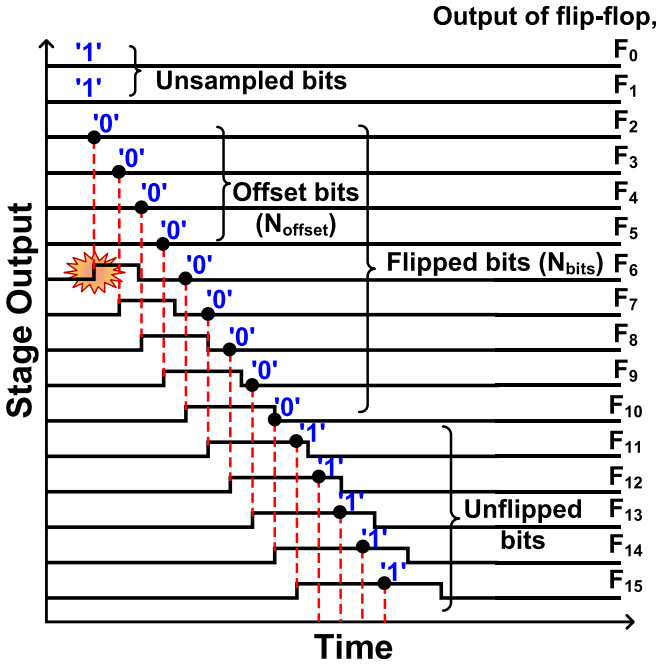


Fig. 7. Timing waveform illustrating pulse expansion and back-sampling technique for measuring the originally induced SET pulsewidth.

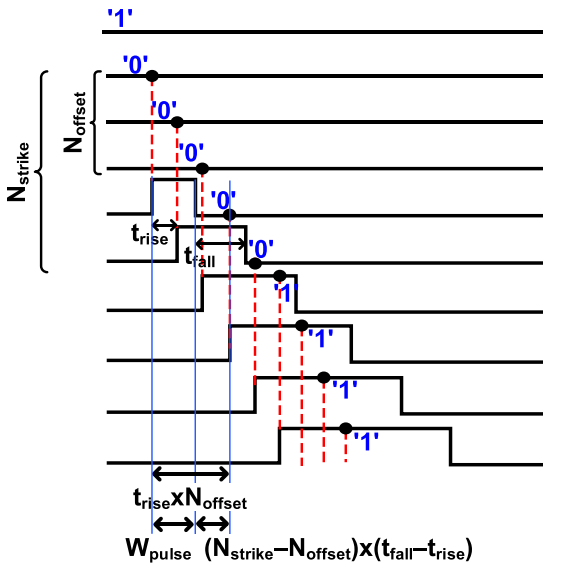
in unbalanced rise and fall time delays ($t_{fall} > t_{rise}$) leading to pulse expansion as it propagates along the chain. Transient pulse width measurement is enabled by back-sampling the fast propagating falling edge of the pulse using its later stage slow moving rising edge. Fig. 6 shows the back-sampling circuit with current-starved buffers and embedded flip-flop scan chain. Pulse expansion enables back-sampling of the falling edge of early stage transient pulse by the rising edge of a later stage transient pulse, as shown in Fig. 7. The detailed working principle of the BSC technique is discussed here. All flip-flop outputs are initialized to all 1's and then the circuit is irradiated under the radiation beam.

Once a strike induces the SET pulse at the inverter junction, it begins to propagate along the buffer chain, expanding while propagating. Since the falling edge of the pulse travels slower as compared with the rising edge, the rising edge eventually catches up with the falling edge and hence the pulsewidth information is captured in the form of the consecutive bit flips that are registered in the flops, as shown in Fig. 6. In the use case shown here, the strike is detected at the output node of third buffer in row number 3 (i.e., input of flip-flop F_{12} or clock of flip-flop F_2).

The induced transient begins back-sampling the nodes that are two rows behind in the chain. In this case, the first back-sampled node is third buffer output node in first row (i.e., input of flip-flop F_2). Hence, all nodes before this node are unsampled and their associated flops store the same initialized "1." Furthermore, as the pulse propagates, it keeps sampling "0" till the falling edge of the strike finally catches up with the rising edge of the later stages sampling pulse. In this case, it happens at the output node of first buffer in last row (i.e., input of flip-flop F_{19}). After this stage, all flops sample a "1" since sampling rising edge cannot catch up with it. We define N_{strike} as the number of bits flipped in the array that is recorded in the scan-out data. In the flipped bits (N_{strike}), we also need to factor in the offset bits (N_{offset}) which are the sampled 0's due to the first two rows of flip-flops. This offset is equal to the number of stages between the sampling node and the flip-flop being back-sampled, which is 2 rows in the array. This is fixed to 500 stages (250 $\times$ 2 rows) in the test chip by design. Based on the rise and fall delay of the chain, N_{strike}, and N_{offset}, the original pulsewidth can be computed. According to our simulations, the minimum pulsewidth that can be measured reliably is $\sim$25 ps which is limited by the setup time and hold time constraints of the flip-flop circuit.

Fig. 8 illustrates the SET pulsewidth computation in detail. N_{offset} is fixed to 500 by design. N_{strike} equals the number of total bits that flipped. The measured N_{strike} varies from strike to strike and contains the SET pulsewidth information. The rise delay and fall delay are measured for the entire chain at different VDD and gate bias voltages before each irradiation cycle. Dividing these delays by the number of stages in the BSC chain gives us the average per-stage pulse expansion rate $t_{fall} - t_{rise}$. The delay in time between rising edge of originally induced pulse and the rising edge of the sampling pulse is given by ($t_{rise} \times N_{offset}$). The original pulsewidth can then be computed by arithmetic subtraction of the added pulsewidth value due to expansion [($N_{strike} - N_{offset}$) $\times$ ($t_{fall} - t_{rise}$)] from the ($t_{rise} \times N_{offset}$) value.

The SER test chip can be configured in three modes, which are calibration, radiation, and scan modes, as shown in Fig. 9. In calibration mode, the BSC arrays are bypassed by means of MUX/De-MUX pairs as shown to estimate delays without the BSC array and then with the array. Difference in delay values gives a precise average propagation delay (t_{rise} and t_{fall})



Pulse width calculation example:

t_{rise}(ps)	t_{fall}(ps)	N_{offset}	N_{strike}	W_{pulse}(ps)
4.2	6.9	500 (fixed)	781 (varies)	168

Fig. 8. Timing waveform illustrating pulse expansion and back-sampling technique for measuring the original SET pulsewidth. t_{rise} and t_{fall} are prechar-acterized, while N_{offset} is set by design (two rows in BSC array). Table shows an example of SET pulsewidth calculation based on measurements parameters.

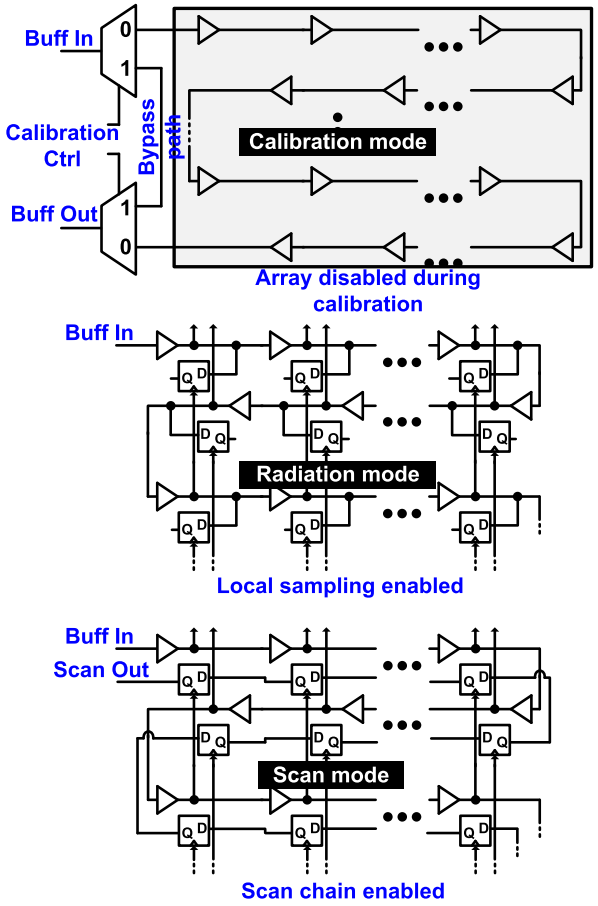


Fig. 9. BSC array can be configured in three modes, viz., calibration, radiation, and scan modes.

value for each buffer stage. Once the delays are measured, the chip is put in radiation mode with all flip-flops initialized to 1. When an SET pulse is generated, the local flip-flops back sample the signal value. This results in consecutive bit flips. After a fixed exposure time, the chip is switched to scan mode where the flip-flops are configured as a scan chain and sampled bits are scanned out for postprocessing. This cycle is repeated every 5–15 min depending on the test VDD. For relatively higher VDD values, irradiation duration is extended since higher supply reduces the probability of strike induction due to increased critical charge and vice versa. Detailed irradiation test routine will be provided in Section IV. A calibration routine just before each irradiation test cycle minimizes measurement error. The test routine details can be found in Section IV.

Fig. 10 shows the generic architecture of BSC array scalable in both row and column dimensions. In this work, a 250 row × 500 column BSC array was implemented in the 14-nm test chip. The array is implemented using tile-able unit cell layout structure that allows for large-scale implementation in both x- and y-directions as shown. A unit cell-based layout is used to enable a uniform implementation that helps in decoupling location-based dependencies on SER due to geometric differences in the array.

Fig. 11 shows the 14-nm SER test-chip layout and specifications. Twelve identical BSC arrays were implemented in the chip. For control and data transfer, an eight-port JTAG control unit (JCU) was implemented with each port integrated to a BSC array pair. The chip configurator block is responsible for controlling the mode of operation in the test chip.

IV. Neutron Irradiation Test Setup

Fig. 12 shows the SER test setup at LANL facility for neutron beam irradiation tests. Ten test boards, each containing nine chips, were vertically stacked in a custom-built aluminum enclosure. The openings at both sides of the enclosure allow the neutron beam to penetrate through all the chips. Nine test chips were mounted on each board. The nine chips on each board were placed in proximity so that all the chips were covered within the 3-in beam diameter. An on-board field-programmable gate array (FPGA) chip handles data and control signal communication via USB to a PC. Programmable low dropout (LDO) regulators and power sequencing (required for FPGA power bring up) schemes implemented on each board allow remote supply and gate bias voltage control via FPGA. To deliver highly stable analog gate bias voltages, a closed control loop-based LDO scheme was implemented on-board with a hierarchy of decoupling capacitors added on die as well as at the package and PCB levels.

The neutron beam energy versus flux plot is shown in Fig. 13 where the beam energy profile roughly follows the terrestrial neutron spectrum profile. The acceleration factor between the two profiles was 5×10^9. The irradiation test

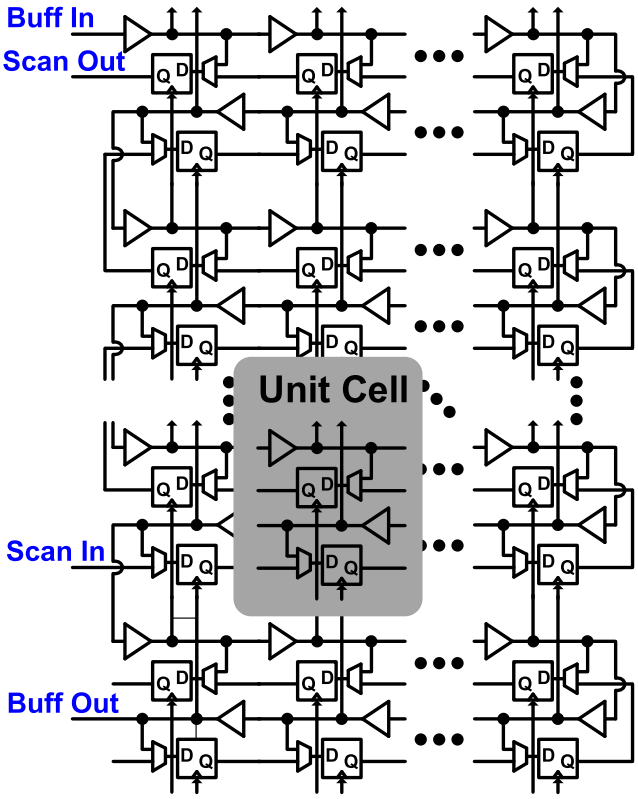
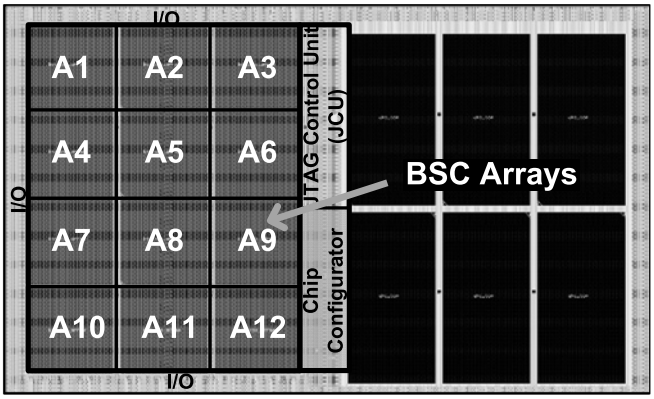


Fig. 10. BSC array implemented using a tile-able unit cell structure.



Technology	14nm 9-metal layer tri-gate HKMG CMOS
Die area	3.7mm x 2.2mm
Nominal VDD	0.7V
Scan chain VDD	1.1V
Array dimension per chip	250x500x12 = 1.5 million BSC stages

Fig. 11. 14-nm trigate SER test-chip layout details showing 12 identical BSC arrays implemented with a total of around 1.7M BSC stages.

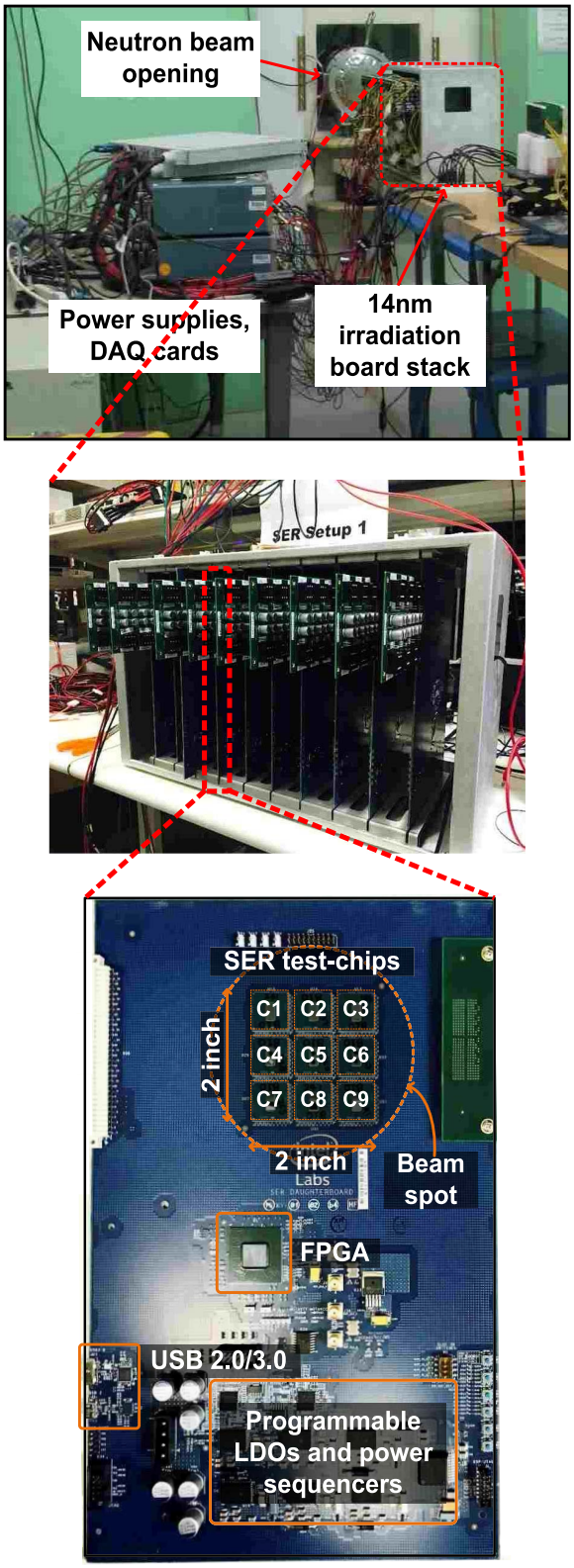


Fig. 12. LANL neutron irradiation test setup with 90 chips on ten boards irradiated in parallel. Custom-built aluminum enclosure designed to accommodate ten SER test boards, each with nine SER test chips. Each SER test board equipped with an FPGA and USB/UART interface for automated remote control.

was conducted for five effective days and extensive SER data were collected under different supply voltage and gate bias conditions. Caution was exercised to avoid any permanent damage due to total ionization dose (TID) by controlling the beam flux and using large pool of test chips/boards to collect massive amount of statistical data.

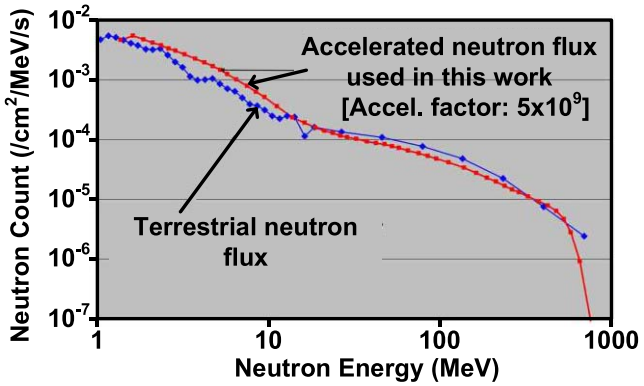


Fig. 13. LANL neutron beam energy versus particle flux profile showing similar trends as compared with the terrestrial neutron profile with an acceleration factor of 5×10^9.

Irradiation test routine (Fig. 14) consists of three phases beginning with the one-time calibration phase where the intrinsic delay values of the buffer chain are characterized for a given VDD and bias voltages and the scan chain is initialized to all "1." First step is a one-time calibration step where the intrinsic delays of the array are measured to establish per stage propagation delay and pulse expansion rate. These two measurements are then used to eventually compute the originally induced SET pulsewidth, as shown in Fig. 8. t_{rise} corresponds to average per-stage propagation delay of rising edge, while t_{fall} refers to the sum of t_{rise} and per-stage pulsewidth expansion. Measured input to output pulse rising edge delay from BSC array gives t_{rise}, while per-stage width expansion can be measured by taking difference of input and output pulsewidth and dividing it by number of BSC stages in the array. Calibration steps are needed each time the voltages are changed (analog bias as well as supply voltage).

Calibration is followed by irradiation phase in which the neutron strikes are detected and captured by the BSC circuit over a period of few minutes. After irradiation, scan-out is performed by raising the VDD to 1.0 V and scanning out all bits from the chain. Higher VDD during scan-out lowers the probability of data corruption under neutron beam. SET, SEU, and MBU errors can be seen in the sample spatial map given in Fig. 14. If a neutron particle strikes a node in the current-starved inverter chain and enough charge is collected, an SET can propagate across the buffer chain. This can be identified by a long trail of consecutive 0's sampled by adjoining flip-flops as shown in the two SET incidents. Isolated bit flips scattered across the map denote SEUs and MBUs that are induced when the strike happens at the storage nodes in the flip-flops. Multiple bit-flips within a reasonable range can be attributed to MBUs, while an SET pulse induction results in consecutive bit-flips with at least 500 stages of propagation. Any SET pulse spanning partially or completely, the last 500 stages (two rows) are discarded from analysis as the back-sampling operation ends at (array length—500)th stage.

V. Neutron Test Results

Neutron irradiation tests were performed for multiple supply voltages as well as different current starving levels. The VDD

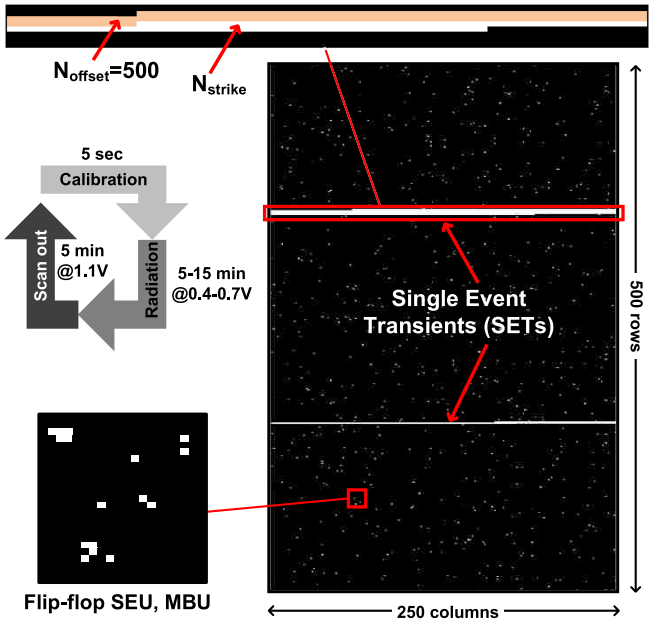


Fig. 14. Irradiation test routine and raw data showing SET/SEU/MBU errors occurring in the BSC array during a single irradiation period. Orange colored bits show N_{offset} (=500, fixed by design), while white colored bits show N_{strike} (varies for each SET strike) in zoomed in SET pulse scan map. All orange/white bits are flipped bits to 0 from 1 during irradiation.

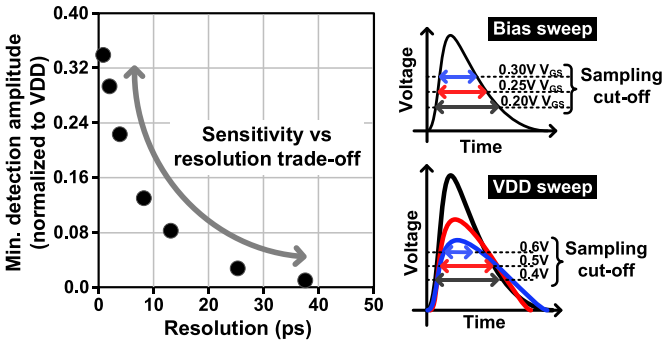


Fig. 15. Simulation plot showing resolution versus sensitivity tradeoff in BSC circuit. The circuit can detect very low amplitude pulses (0.08× of VDD) with relatively good precision (12 ps); VDD and gate bias voltage knobs can be used in conjunction with each other to precisely control sensitivity.

sweep enabled analysis of SER trends as a function of supply voltage, while gate bias voltage sweep enabled analysis of SER dependence on the sensitivity. The pulsewidth measurement resolution could be tuned in 1.3–35-ps range which allowed detailed pulsewidth distribution analysis.

Fig. 15 shows the simulation plot depicting resolution versus sensitivity tradeoff. Bias voltage knobs in conjunction with VDD can be used to fine-tune resolution and sensitivity. This provides the ability to collect accurate data for different radiation/beam parameters and operating conditions. Furthermore, it enables sensitivity and resolution tuning during the experiments. Fig. 15 (right) illustrates both VDD and gate bias sweeps that vary the sampling cutoff.

Pulsewidth measurement was carried out for both VDD and gate bias sweeps. Fig. 16 shows the measured SET voltage pulsewidth distributions. During VDD sweep, gate bias

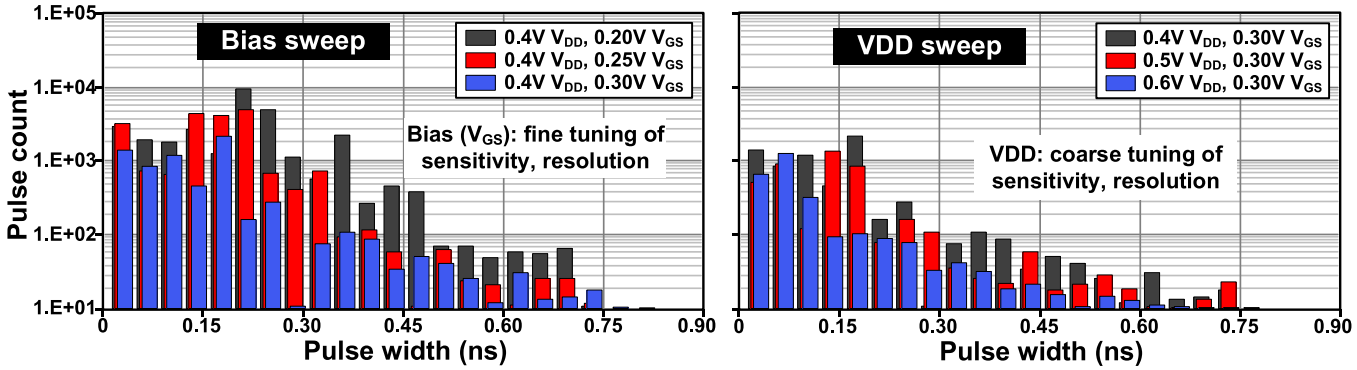


Fig. 16. Measured SET voltage pulsewidth distribution for bias sweep and voltage sweep. Bias/VDD control knobs allow precise tuning of both resolution and sensitivity in accordance with the requirements.

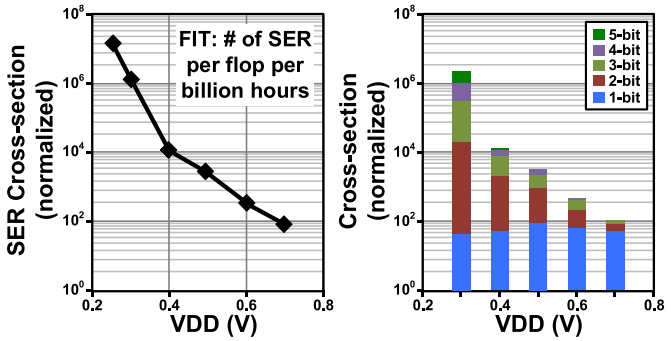


Fig. 17. Measured SER cross section plot of flip-flop SEUs as a function of VDD (left); measured normalized SER cross section of flip-flop SEUs and MBUs across various VDD points (right). Further details of the SEU and MBU pattern analysis method can be found in [22].

voltages were fixed which affect the sensitivity as well as pulse amplitude. At lower VDD, sampling cutoff drops which results in wider pulses being sampled. This is evident from the distribution plot where lower VDD contributes to generally wider SET pulses, while higher VDD has narrower pulses sampled. Moreover, critical charge goes down which leads to higher SER activity. Hence, at 0.4 V, SER is highest, also reflected in the absolute SET pulse count as compared with that at 0.6 V.

During gate bias sweep, VDD was kept constant while changing the current starving biases of the buffers. With more starving, sampling cutoff drops which results in wider voltage pulses. This is clearly seen in the distribution plot where the highest starving voltage of 0.2 V shows more sampled pulses in the wider range as compared with the lowest starving point of 0.3 V where majority of the sampled pulses are of narrow width.

Although not the main focus of this work, SEU and MBU errors captured by the flip-flop scan chain embedded within the BSC array are shown in Fig. 17 for the reader's information. Fig. 17 (left) shows measured SEU cross section as a function of supply voltage. Cross section is the measure of rate of soft errors per unit area. The plot shows an exponential rise in SER as VDD scales down. There are around four orders of magnitude rise in SER at 0.3 V as compared with 0.7 V which is the nominal VDD of this technology. This can be attributed to the lowering of Q_{crit} with VDD which, in turn, results in a steep increase in cross section.

Fig. 17 (right) shows the number of SEU and MBU at different VDDs. The method we used to distinguish and classify different SEU and MBU patterns along with the detailed error rate statistics can be found in [22]. Overall SER cross section rate increases as VDD scales down resulting in lower critical charge required for an upset. In addition, at higher VDDs, due to relatively higher critical charge, probability of an MBU reduces since not enough charge is collected to induce an upset in multiple storage nodes in flops. This trend shifts toward MBU dominant cross section for lower VDD values. This can be attributed to the lower critical charge at lower VDDs that allows multiple upsets in closer proximity when ample amount of charge gets collected during the strike enough to induce multiple storage node upsets in adjacently located flops through charge diffusion and sharing. Another point to note is that the SEU contribution slowly reduces as the VDD scales down. The probable reason may be that some of the SEUs are counted as 2 bit or higher MBUs resulting in higher MBU and lower SEU cross section.

SEU probability across all arrays and multiple scan cycles was analyzed to check for any spatial variation. Fig. 18 shows the SEU probability map for close to 12 960 scan cycles at 0.5 V. The SEU probability is shown to be random without any strong correlation between SEU induction rate and the strike location. This may be attributed to the uniform layout implementation of the BSC array which facilitated decoupling of location-based dependence from SER results. Uniform exposure to neutron beam might have also contributed to this random behavior.

VI. SET Pulse Reconstruction

SET voltage pulsewidth data measured from the BSC core for different sampling cutoff points can be used to reconstruct the voltage transient pulses using a combination of SPIC-based circuit simulations and an analytical model. The pulse reconstruction method is illustrated in Fig. 19 where the measured width data along with the sampling cutoff information obtained through simulations can be used to reconstruct the

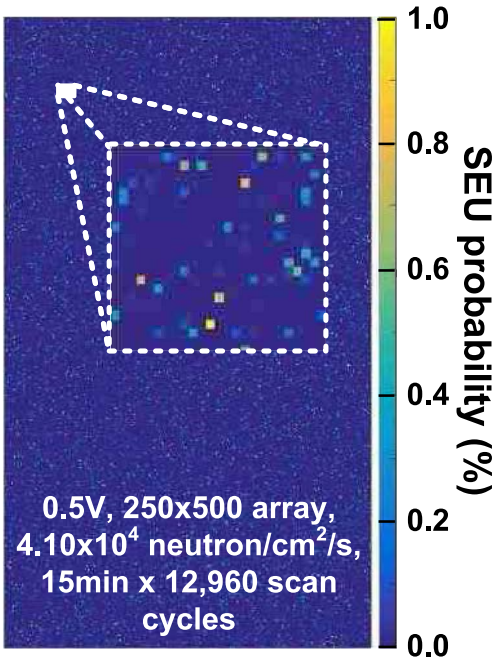


Fig. 18. SEU probability distribution map showing uniform average SEU probability across multiple scan cycle data. This confirms that there is negligible correlation between SEU and strike location within the arrays.

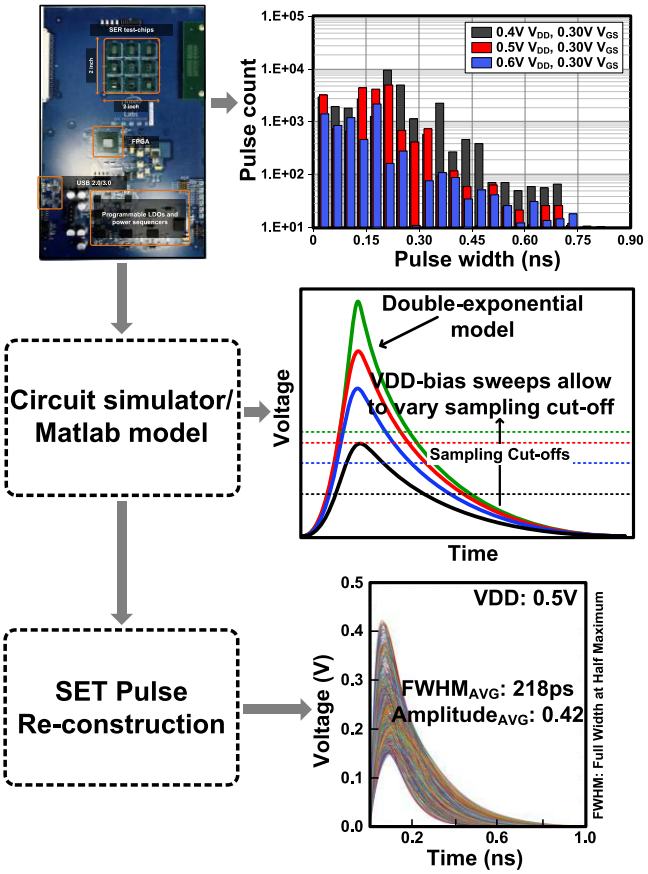


Fig. 19. SET pulse reconstruction framework using a combination of measured data and circuit simulations.

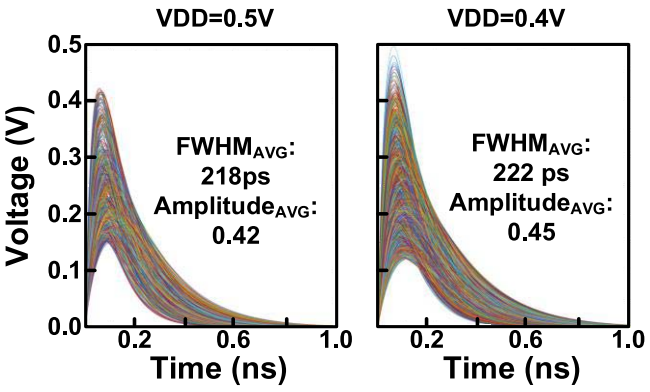


Fig. 20. Reconstructed SET voltage pulses at 0.4- and 0.5-V VDD.

transients as shown. To the best of our knowledge, this is the first report showing individual SET pulses reconstructed from irradiation data. This is an important step forward in enabling a framework that can accurately estimate the current transient induced by a radiation strike. With the use of a compact model, reconstructed current transients can then be mapped on to any given circuit topology to get an estimate of SER susceptibility.

Individual SET voltage pulses were reconstructed for different VDDs. Fig. 20 shows a side by side comparison of reconstructed pulses for 0.4- and 0.5-V VDD. At lower VDD, both the pulse amplitude and pulsewidth are higher as compared with 0.5 V [as seen from the average full width at half maximum (FWHM) and amplitude values].

One important point to note here is that proposed reconstruction methodology is agnostic to the underlying current transient charge injection/collection model (e.g., double exponential model). A more accurate or suitable model specific to FinFET devices can be calibrated using collected SET pulse data and used for running SER simulations on any type of logic gate. We would also like to make it clear that our test results are from current-starved inverters and, hence, there can be some discrepancy with the results from standard logic gates. However, our tunable test structure can provide deeper insight into the dependence of logic SER on various circuit parameters that would otherwise be difficult to observe in standard logic gates. This unique capability in conjunction with the SER data of standard logic gates [6], [23] can help obtain an accurate and detailed picture of logic SER in extremely scaled technologies.

The joint distribution plot of amplitude and FWHM for the reconstructed SET voltage pulses is shown in Fig. 21. In the plot, we can see a general trend that for higher amplitude pulses, the widths tend to be narrower and vice versa. This can be attributed to the fact that for a nearly constant charge collected under the junction area, higher amplitude SET pulses tend to be narrow, while low amplitude pulses are mostly wide so as to keep the area under the voltage–time curve constant (i.e., charge is constant).

Finally, Fig. 22 shows the comparison summary of the proposed circuit and prior arts. The proposed circuit is regular, tunable, and scalable in terms of layout implementation and exhibits a 1.3–35-ps width measurement resolution. The circuit

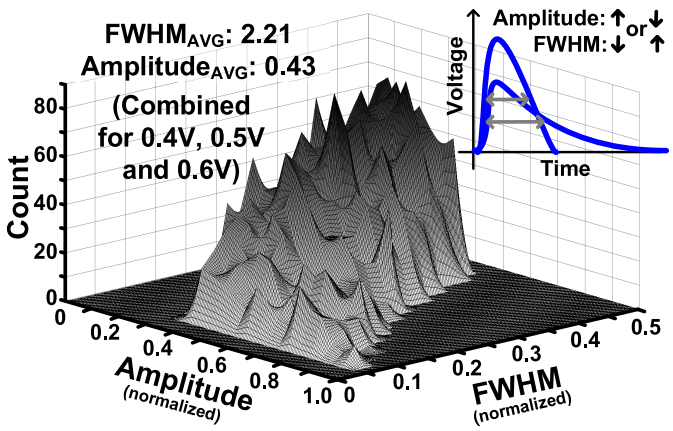


Fig. 21. Joint distribution plot of amplitude and FWHM of reconstructed SET voltage pulses.

	TDC based circuit [5]	Pulse shrinking [7]	This work
Unit cell layout	Irregular, not easily scalable	Regular, scalable	Regular, scalable
Sensitivity tuning	Fixed by design	Fixed by design	Variable using bias knobs
Resolution*	> 30ps	> 1ps	> 1.3ps
Q_{crit} sensitivity*	1x	0.6x	9x

* Results reproduced in 14nm process

Fig. 22. Summary table showing comparison between proposed circuit and previous works.

is extremely sensitive in terms of critical charge across multiple VDD points, making it an ideal candidate for radiation-induced strike detection and SER characterization.

VII. Conclusion

A highly sensitive BSC technique is proposed for efficient and accurate characterization of radiation-induced soft errors. The proposed circuit makes use of current-starved buffer chain with analog bias voltage knobs that enable fine-tuning of sensitivity and resolution. Local sampling flops eliminate any possible width modulation due to longer and irregular propagation paths. The BSC circuit can capture SETs, SEUs, and MBUs simultaneously, making it a suitable candidate for SER characterization. With highly sensitive detection chain circuit and a scalable architecture, it enables large volume data collection within a limited beam time. The VDD and bias knobs enable a 2-D resolution and sensitivity sweep that allows reconstruction of individual strike pulses based on the collected strike data.

Acknowledgment

The views and conclusions contained in this article are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the U.S. Government.

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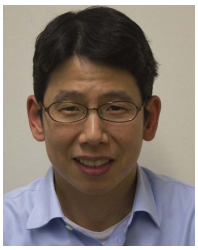

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