Neutron-Induced Pulse Width Distribution of Logic Gates Characterized Using a Pulse Shrinking Chain Based Test Structure

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***Abstract*—This work presents measured data showcasing neutron-radiation induced Single Event Transient (SET) pulse widths in distinct standard logic gate types, together with a detailed analysis on the choice of design parameters impacting the corresponding sampled pulse width distributions. The SET pulse width distributions are obtained from a high density, array-based characterization-vehicle, implemented in 65nm planar CMOS and 16nm FinFET processes, featuring a tunable, high resolution pulse-shrinking chain together with a closely embedded sampling circuit to avoid width distortion effects. The proposed macro employs standard logic gate-chains in varying lengths, threshold voltages (V_{TH}) and transistor width flavors as the Devices-Under-Test (DUTs). Measured irradiation data for a range of operating voltages from nominal down to near-threshold reveals the relative impact of the chosen design parameters such as VDD, V_{TH}, device width and the logic chain length as well as their interplay, impacting the overall soft-error susceptibility and the sampled pulse width distributions among the different standard gate types.**

***Index Terms*— Circuit reliability, combinational logic, neutron irradiation, single event effects, single event transient, single bit upset, soft error rate, radiation effects.**

I. Introduction

THE scaling of feature sizes over the years in accordance with the Moore's Law has witnessed the general trend of gradual reduction in supply voltages, improvement in circuit delays and an increase in the on-chip device densities, all in the quest of simultaneously improving the Power, Performance and Area (PPA) metrics of the system. Unfortunately, this has also led to renewed reliability concerns, with soft-error being one among the many. Soft error susceptibility goes up exponentially with the reduction in chip operating voltages [1-3]. Moreover, with the reduction in circuit delays, the gate response time improves, with the consequence that the probability of a narrower Single Event Transient (SET) surviving through combinational logic and getting captured in a sequential element increases manifold [4, 5]. Finally, although innovations in the transistor design itself have led to a reduced per-device Soft Error Rate (SER) [6-10], soft error susceptibility still increases proportionally with increased transistor count on-die, as a consequence of scaling [1]. Designing complex logic blocks intended for high radiation environments in today's technology nodes therefore necessitates developing an insight into the design parameters affecting the soft error vulnerability of actual standard logic gate cells, as opposed to indirect translations from inaccurate representations, for instance [11, 12].

To this end, in our recent paper [13], we introduced a highly scalable, logic SER and SET pulse width characterization macro employing a tunable pulse shrinking chain architecture and featuring standard combinational logic gate variants as the Devices-Under-Test (DUTs). We further presented the measured cross-section statistics obtained from neutron irradiation experiments conducted at the Los Alamos National Science Center (LANSCE), showcasing the interplay between a host of factors such as the node capacitance, restore current ($I_{RESTORE}$), transistor stacking, logic chain length and supply voltage (VDD), jointly determining the SER for a gate type and flavor.

Our previous discussion was limited to the gate failure rate statistics. In this follow-up paper, we present in detail, the corresponding sampled pulse width distribution data, highlighting the principal utility of the proposed test-vehicle. Several studies have reported pulse width distributions for transistor variants and VDDs at multiple process nodes, for instance [14, 15]. This work provides further insight on the impact of key logic design parameters on the SET pulse width distributions in context to the different logic gate types.

The rest of the paper is organized as follows. In section 2, we review the proposed standard logic characterization-vehicle and the silicon prototypes together with the calibration / irradiation routine at LANSCE, further expanded from [13] to facilitate a better understanding of the proposed concept in correlation to the measured results presented later. Section 3 briefly recapitulates the simulated $I_{RESTORE}$ and critical charge (Q_{CRIT}) trends, discussed here for the reader's convenience. Section 4 showcases the sampled SET pulse width distributions for the distinct standard logic gate variants implemented in this work, arranged subsection-wise to highlight the impact of a specific design parameter together with the related analysis. Finally, section 5 presents the conclusions drawn.

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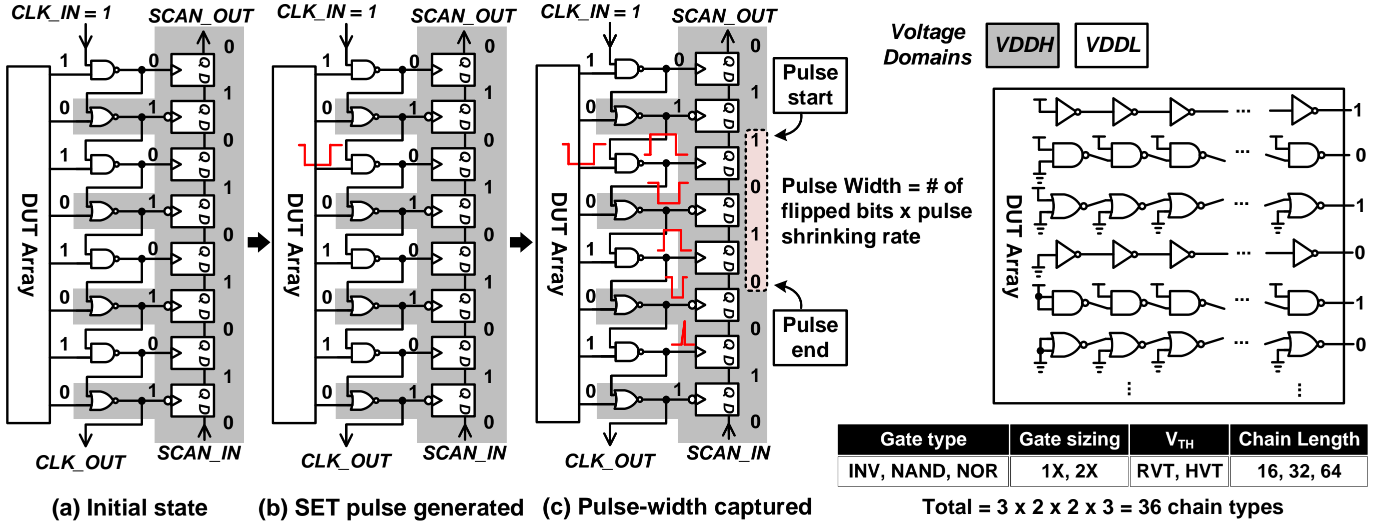
II. Proposed Macro Concept, Silicon Implementation and Irradiation At LANSCE

A. *The Pulse-shrinking Chain-based Soft-Error Monitor*

Fig. 1 graphically details the proposed test-vehicle concept. The DUT array consists of distinct chain lengths comprising the standard combinational gate types ubiquitous in digital-design viz. INV, NAND, NOR, implemented in varying flavors of V_{TH} and device widths. The array can also be readily modified to study other gate topologies in a standard cell library, thus serving as a characterization-vehicle for gates designed in a particular technology node. The transient detection and pulse width measurement circuitry comprises of a NAND-NOR chain serving as the clock to a chain of serially connected D Flip-Flops (DFFs), routed in an opposite direction to avoid the possibility of hold-time violations. The supply voltage of the DFFs and the NOR gates in the clock-chain is kept at a slightly higher value (VDDH) compared to the DUTs and the NAND gates in the clock chain (biased at VDDL). Prior to irradiation, the DFFs in the array are programmed using a scan sequence comprising alternate '0's and '1's as shown in Fig. 1(a). A transient error in the standard logic gate chains in Fig. 1(b), enters the NAND-NOR clock chain, where it experiences a picosecond-order, bias-controlled, uniform shrink rate (set by the relative difference in magnitudes of VDDH and VDDL, increasing the drive strengths of the stacks in the clock-chain) as it propagates downwards along the chain, while also clocking the serially connected DFFs in succession (Fig. 1(c)). This causes the initially programmed checkerboard sequence in the array bit map to shift up by one bit until the SET pulse width falls below the capture resolution of the DFF (details in Fig. 3), clearly demarcating the start and end points in the flip-flop chain as successive 0's or 1's. Although the DFF resolution can be improved to beyond the limit imposed by the technology node, for instance, by skewing the clock pulse to expand within the DFF, it would not be representative of a real test case and construe unnecessary overdesign. Hence, the proposed test vehicle takes the corresponding sequential element resolution into account, with the DFF acting as a high pass filter, rejecting any SETs below its capture resolution, as in a realistic scenario. The point of entry into the flip-flop chain reveals the DUT failure location whereas the number of flipped stages translate to the transient pulse width. Fig. 2 presents an experimentally obtained array bit-map for an irradiation duration of 5 minutes, with VDDL and VDDH set to 0.6V and 0.681V respectively, showcasing an SET with the DUT failure location highlighted, together with a Single-Bit-Upset (SBU) in one of the DFFs.



Gate type	Gate sizing	V_{TH}	Chain Length
INV, NAND, NOR	1X, 2X	RVT, HVT	16, 32, 64

Fig. 1: Graphical illustration detailing the proposed concept: (a) the pulse width measurement circuit programmed in its initial state using a sequence of alternating 0's and 1's, (b) the depiction of a transient generated in one of the logic gate chains or the DUTs as a consequence of a radiation strike, and (c) the subsequent SET pulse width capture in the form of a digital code. The shifted portion of flip-flop bits in the scanned out data reveals the SET injection point in the chain as well as the pulse width information. 36 DUT types comprising the different standard logic gate types in distinct flavors of V_{TH}, device width and chain lengths were implemented for comprehensive SET pulse width characterization.

The proposed test-vehicle has the following features which makes it effective for characterizing logic soft-errors. First, the test-vehicle can characterize both SER and SET pulse widths for standard logic gates, obviating the need of indirect

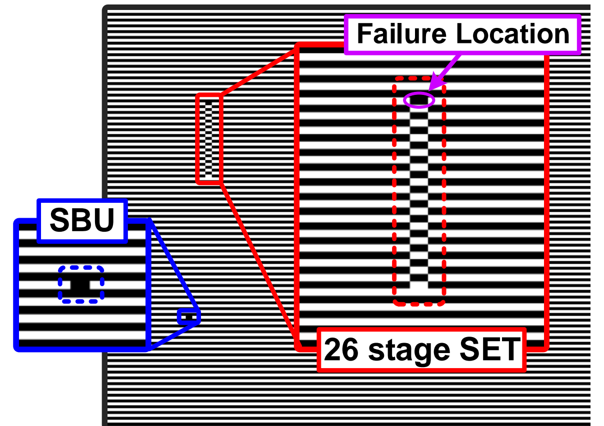


Fig. 2: Experimentally obtained array bit-map highlighting an SET spanning 26 stages together with a Single-Bit-Upset (SBU) in one of the DFFs.

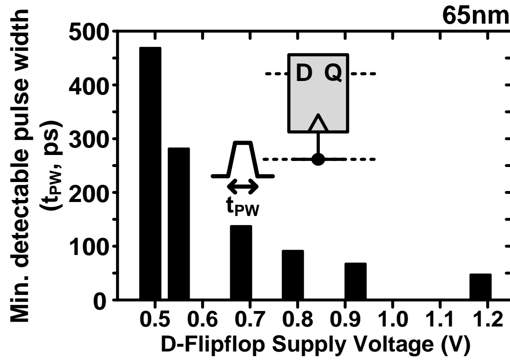


Fig. 3: Post-layout simulations showcasing the D flip-flop resolution for multiple values of VDDH used in the irradiation experiment.

translations from potentially inaccurate representations. Second, the overall architecture comprises entirely of standard library cells and is unit tile-able (Fig. 4), which results in a highly regular and compact layout, making the test-structure both readily scalable and process portable. The measurement circuit also occupies a small footprint, further increasing the overall area efficiency. Third, local sampling of the transient by the closely embedded measurement circuitry avoids any possibility of pulse width distortion [16]. Fourth, the pulse-shrinking resolution is set by the relative difference in magnitude of the two supply voltages VDDH and VDDL, which provides a simple sensitivity control knob, independent of the technology of design, along with the flexibility of fine post-silicon resolution trimming. Finally, the DFF accounts for the sequential element capture resolution in a given technology node, making the measured results closer to actual errors occurring in an actual logic block.

B. Test-Chip Implementation

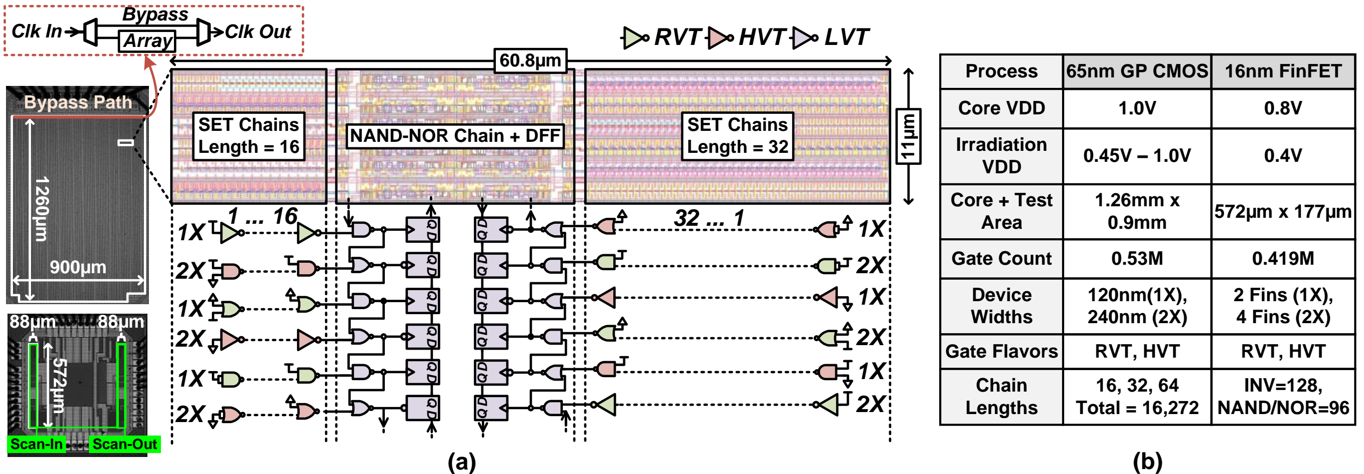
Fig. 4 presents the die-micrographs corresponding to the 65nm and 16nm versions of the design, together with the silicon implementation summaries. The standard logic gates were designed with all transistors identically sized, either at 1X or 2X, and were implemented in two V_{TH} flavors: Regular Vth (RVT) and High Vth (HVT), and three different chain lengths 16, 32 and 64 for the 65nm version. Fig. 4 (a) also illustrates the layout for a unit-cell variant comprising chain lengths of 16 and 32, with the sampling circuit embedded in-cell. To avoid any systematic effects, chain lengths of 16, 32 and 64 were distributed uniformly throughout the available die space and an identical version of each unit-cell was designed, wherein the logic gate chains feeding the NAND and NOR gates in clock-chain respectively were swapped. Furthermore, the embedded measurement circuit comprising the clock-chain and the DFFs was designed using non-minimum sized Low-V_{TH} (LVT) devices to minimize any occurrences of soft-error events. To verify this assumption, a dummy chain consisting of only the measurement circuit was implemented as part of the design. Discussed previously in [13], measured SER cross-section results confirmed our hypothesis of negligible errors in the readout circuit.

The 16nm version of the design was implemented as a test-structure on a shuttle utilizing the limited die-area available on the sides (Fig. 4 (a), bottom left). Fixed chain lengths of logic gates, 128 for INV and 96 for NAND / NOR were implemented from the point of view of both efficient utilization of the available die-space and maximizing the chances of a radiation-induced strike event. As in the 65nm version, the standard logic-gate chains were implemented in two V_{TH} flavors and two device sizes viz. 1X (2 fins per device) and 2X (4 fins per device).

C. Irradiation Experiment at LANSCE

As discussed in [13], nine 65nm boards, comprising five test chips each together with five 16nm boards, consisting of one test-chip each, were stacked vertically and exposed to a spallation neutron beam for a total of five effective days at LANSCE. The total irradiated gate count was 26M gates (24M gates for the 65nm prototype, 2M for the 16nm version). The beam energy ranged between 1.38 - 750MeV while the average beam flux was $2.03\text{x}10^6$ neutrons/cm2/sec. Fig. 5 presents the neutron fluence details for each of the DUT irradiation voltages (VDDL) over the experiment duration at LANSCE.

The scan and clock inputs corresponding to the five 65nm test chips were daisy-chained to result in combined scan and clock inputs per board. (For the single test-chip corresponding



Process	65nm GP CMOS	16nm FinFET
Core VDD	1.0V	0.8V
Irradiation VDD	0.45V – 1.0V	0.4V
Core + Test Area	1.26mm x 0.9mm	572µm x 177µm
Gate Count	0.53M	0.419M
Device Widths	120nm(1X), 240nm (2X)	2 Fins (1X), 4 Fins (2X)
Gate Flavors	RVT, HVT	RVT, HVT
Chain Lengths	16, 32, 64 Total = 16,272	INV=128, NAND/NOR=96

Fig. 4: (a) Die-micrographs for the 65nm and 16nm versions reproduced from [13], showcasing the layout details of a unit-cell variant together with the bypass path used for delay calibration, and (b) Test-chip implementation summaries.

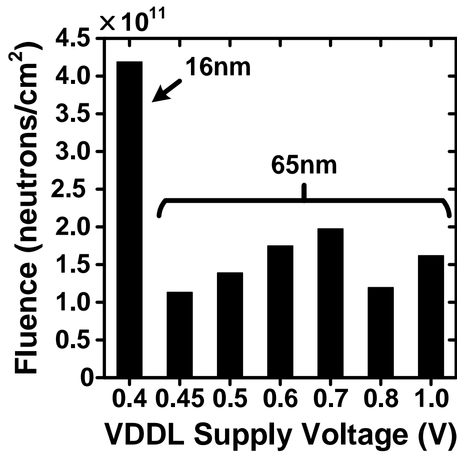


Fig. 5: Neutron fluence numbers for the DUT irradiation voltages (VDDL) used in the experiment.

to the 16nm version per board, the scan and clock inputs were tiled internally by design (Fig. 4)). Prior to irradiation, a one-time calibration routine was performed to measure the per-stage contraction rate for multiple values of VDDL and VDDH. A matched bypass path consisting of a MUX-DeMUX unit, illustrated in Fig. 4 for the 65nm prototype, was used during the calibration routine to cancel out any unwanted routing or parasitic delays existing on-chip, on-board or introduced due to equipment I/O differences. At this step, the standard deviation in the per stage delay between the boards was evaluated and the VDDH values were readjusted to result in appreciably higher values for the per stage contraction rate. This was done to ensure random variation induced differences were negligible for the transient pulse width distribution studies, especially at low supply voltage levels (Fig. 6).

An automated FPGA based test-flow was adopted for the experiment, wherein a checkerboard sequence (752Kbits) was written to all 50 test chips while also reading out the stored flip-flop values. This sequence was repeated every five minutes of irradiation exposure. Also mentioned previously, we did not observe any systematic trends indicating a non-uniformity in the neutron beam flux, potentially on account of stacking multiple boards vertically in the beam path, confirmed from the measured results between different boards.

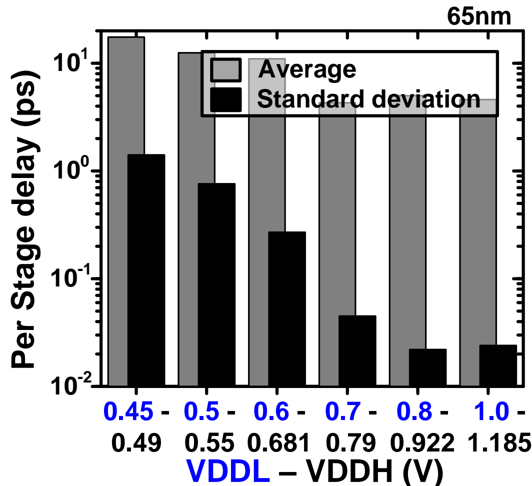


Fig. 6: Average and standard deviation for the stage delay numbers corresponding to the nine 65nm boards used in the experiment, measured during the calibration routine at LANSCE.

III. Recap: Simulation-Based Analysis

This section briefly recapitulates the simulated restore current ($I_{RESTORE}$) and critical charge (Q_{CRIT}) trends for the 65nm technology node, illustrated in [13] and re-summarized here to facilitate an easy correlation between the DUT design and the measured pulse width distributions presented in Section IV. For a detailed overview of the simulated trends, the simulation methodology, together with the associated analysis, the interested reader is referred to [13].

A. *Simulated $I_{RESTORE}$ Trends*

Fig. 7 presents the transistor-level detail for the standard logic gates implemented in this work. As discussed previously, the devices in the Pull-Up-Network (PUN) and the Pull-Down-Network (PDN) were all identically sized, either at 1X or at 2X (Fig. 4). This results in low values of simulated $I_{RESTORE}$ (~0.5X) for the stacked PUNs / PDNs, the exact magnitude of which also varies slightly with the supply voltage levels. The low mobility of holes in the 65nm process further results in reduced $I_{RESTORE}$ for the p-channel devices comprising the PUNs, in comparison to their PDN counterparts. As a consequence, the PUN for the NOR gate exhibits the lowest $I_{RESTORE}$ level among the three gate types, in stark contrast to its PDN, which exhibits the highest $I_{RESTORE}$ for a given sizing, at a given supply level. Furthermore, simulations reveal the HVT variants to be especially weak at low supply voltages such as 0.45V and 0.5V, as a consequence of the reduced gate overdrive, with even the 2X device width variants exhibiting lower drive currents compared to the 1X RVT flavors. These preliminary simulation-based observations will be helpful in analyzing the measured data presented in Section IV.

B. *Simulated Q_{CRIT} Trends*

To conceptually study the soft-error susceptibility of a gate type relative to others, Q_{CRIT} simulations were performed on the post-layout netlists of the tile-able unit-cell, so as to accurately account for the layout-introduced parasitics, which play an important role in determining the vulnerability of a gate node to a soft-error event. A double-exponential current source, modeled in Verilog-A, was used to mimic the radiation-induced strike event for the low-going (1→0) and the high-going (0→1) transitions, for the purpose of individually examining the

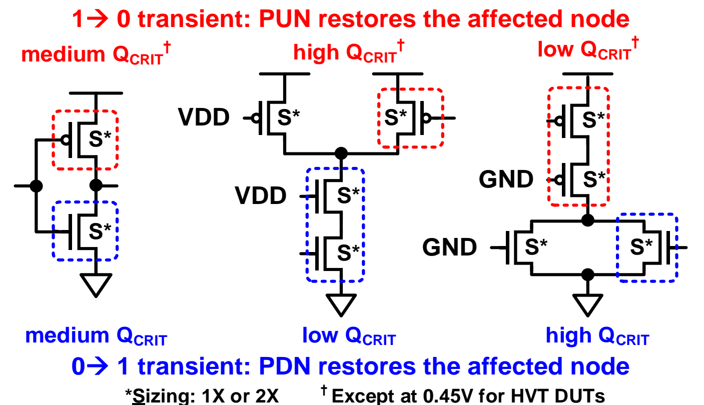


Fig. 7: Implemented logic gates with the relative expected Pull-Up-Network (PUN) and Pull-Down-Network (PDN) sensitivity highlighted.

relative PUN and PDN sensitivity (Q_{CRIT}, 1→0 and Q_{CRIT}, 0→1). Furthermore, we introduced the mean of the two, the Averaged Q_{CRIT}, as a metric to determine the cumulative susceptibility of a logic gate. These simulations account for both the drive current / $I_{RESTORE}$, as well as the device capacitances and the parasitics at the gate output node, which prove insightful in understanding the comprehensive soft-error susceptibility for a given logic gate.

Fig. 7 highlights the Q_{CRIT} simulation trends for the PUN and PDN corresponding to the three logic gate types. As expected, networks featuring stacks (NAND / NOR) exhibit the lowest Q_{CRIT}, primarily due to the reduced $I_{RESTORE}$ as a consequence of the extra channel resistance introduced in series. Contrary to this, networks featuring an off-device in parallel, such as the NAND PUN or the NOR PDN, demonstrate the highest Q_{CRIT} values, on account of the extra node capacitance introduced by the off-transistor at the gate output node, despite the network configuration being logically equivalent to that of the INV. In [13], we discussed about the node capacitance and process variations being the dominant factors determining the SER susceptibility at Near-Threshold Voltages (NTV) viz. 0.45V and 0.5V) in comparison to the $I_{RESTORE}$, which becomes the dominant factor at nominal voltages (1.0V), offsetting the former two. Simulations reveal a substantially higher Q_{CRIT} (0→1) for NOR gates at NTV compared to the other gate types, supplementing this observation. Furthermore, despite the stacked PUN, the weaker 1X HVT NOR gates exhibit higher Q_{CRIT} (1→0) at 0.45V compared to the INV, primarily due to the extra node capacitance introduced by the off-transistor at the output node, in conjunction with the very weak $I_{RESTORE}$. In general, the simulated Q_{CRIT} trends are a strong function of the irradiation voltage, which determines the interplay between the node capacitance and the drive current, modulating the soft-error susceptibility of a logic gate type and sometimes resulting in deviations from the expected norm.

It should be noted, however, that these post-layout Q_{CRIT} simulations do not account for secondary effects such as process variations, electrical masking, exposed junction areas and the like, and therefore, may fail to account for these effects happening in an actual irradiation setup. Nevertheless, the insight provided by these first-order simple layout-based simulations still proves useful in developing an understanding of the measured results, as we shall see in the subsequent section.

IV. Measured Transient Pulse width Distributions

This section presents the pulse width measurement results corresponding to the standard logic gate variants, arranged section-wise to highlight the impact of a specific design parameter on the sampled SET pulse width distributions. The sampled pulse widths in the following section are obtained by multiplying the calibrated stage delay corresponding to a specific VDDL-VDDH setting at LANSCE (Fig. 6) with the number of flipped DFF stages in the chain.

A. DUT Supply Voltage (VDDL) and Gate type Impact

Fig. 8 showcases the sampled pulse width distributions from our proposed test-vehicle comparing the three standard logic gate variants at multiple values of supply voltages, ranging from NTV (0.45V, 0.5V) all the way upto nominal (1.0V), with the x-axis limits kept the same at a given irradiation level (VDDL). The increase in supply voltage (moving from the topmost row to bottom in Fig. 8) increases the $I_{RESTORE}$ of the gate, making it more immune to soft-errors as well as improving its response time, thus allowing rapid restoration of the affected node state, and thereby resulting in narrower pulse width distributions with fewer sampled pulse-counts. Evinced from measured data, sampled pulse width distributions span a range of approximately 40ns at a supply voltage of 0.45V to less than 150ps at the nominal voltage of 1.0V, exhibiting a nearly 240X increase in the widest sampled pulse (Fig. 9).

The pulse width distributions illustrated in Fig. 8 capture two distinct signatures differentiating the three gate types. First, the gates featuring stacks viz. NAND and NOR, exhibit broader distributions with distinctly higher pulse counts at wider pulse widths, primarily a consequence of the lower $I_{RESTORE}$ in a stacked PUN / PDN, resulting in poorer immunity and a slower response time to a soft-error event. This is especially true for the NOR gates in the 65nm process due to the lower hole mobility in the p-channel transistors, leading to a further lowered $I_{RESTORE}$, which results in broader sampled distributions for this gate type. Although the distinction between stacked and unstacked gate types is not clearly apparent at NTV levels (i.e., 0.45V, 0.5V) owing to a similarly weak $I_{RESTORE}$ in all gate types, it becomes apparent as the supply voltage is increased to levels of 0.6V and 0.7V, with higher counts for wider pulse widths primarily sampled from the stacked gate types and the effect particularly evident for the weaker 1X HVT variants. Finally, with the increase in $I_{RESTORE}$ at nominal voltages, the pulse width distributions all span a similar range, with only marginally higher sampled pulse-counts for the stacked gate types.

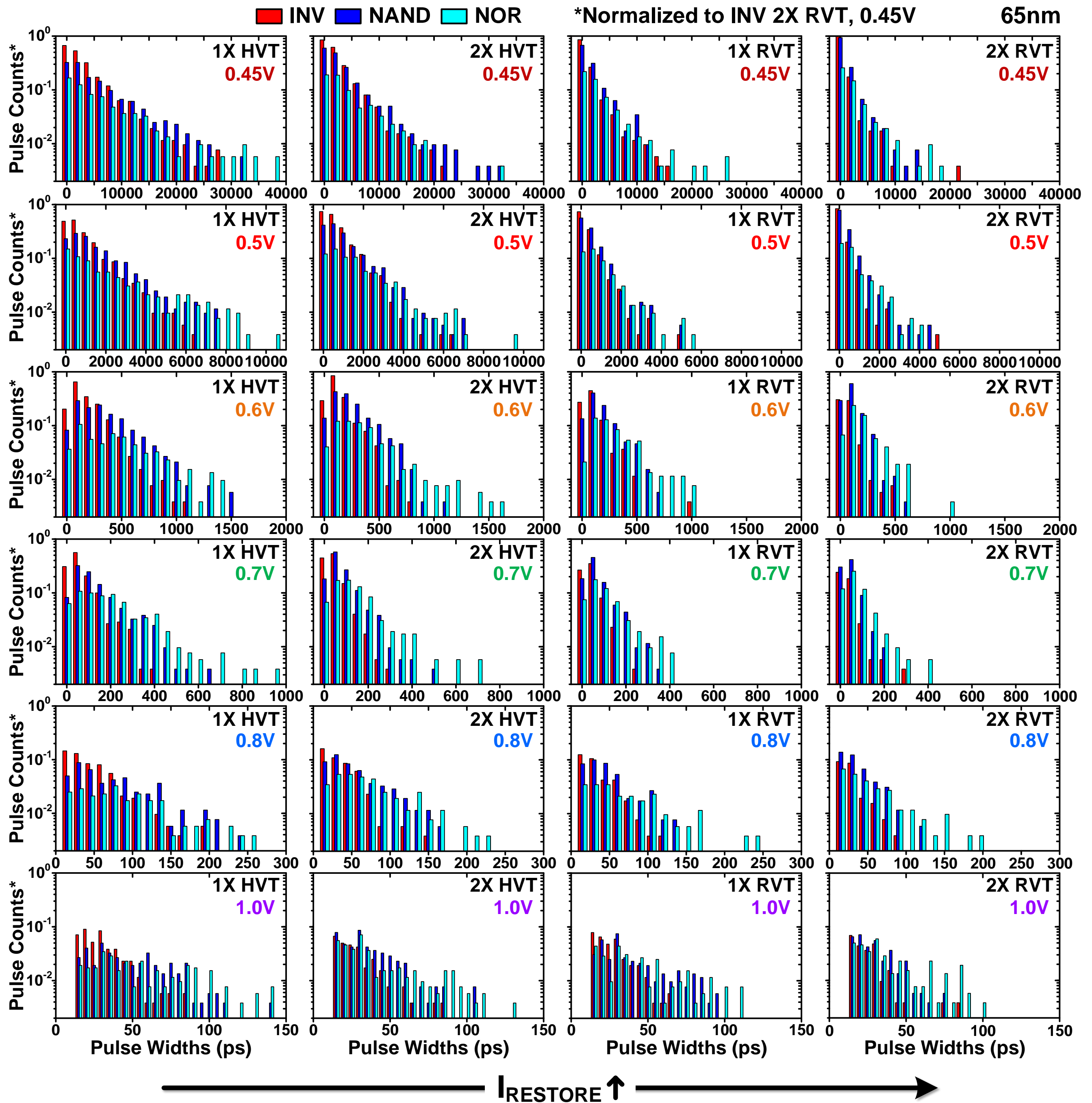


Fig. 8: Sampled pulse width distributions corresponding to the standard logic gate variants presented at multiple irradiation voltages (VDDL) and for the distinct transistor drive current variants, showcasing the impact of supply voltage, the $I_{RESTORE}$ variant and the logic gate type.

The second signature differentiating the three logic gates is a consequence of electrical masking or pulse quenching effects [17-21], causing several narrower SET transients to shrink within the logic gate chains, the severity of which is a strong function of the supply voltage, process variations, the drive current or $I_{RESTORE}$ and the gate type, with the stacked gates particularly susceptible to this effect, as discussed previously [13]. At lower supply voltages, the reduction in $I_{RESTORE}$ results in an increased gate response time to an SET event. Moreover, process variations result in further mismatched propagation delays, the severity of which increases especially at lower supply levels and for the lower $I_{RESTORE}$ variants. The combined effect of the two causes several narrower transients to attenuate and shrink in-chain, prior to reaching the measurement circuitry. To understand this better, consider the case of a gate operating at the slow process corner in a logic gate chain. When a transient propagating along the chain encounters such a gate, it degrades the slope of either the rising or the falling edge of the transient, resulting in a narrower pulse at the output of the subsequent stage. Furthermore, due to the increased response time, this gate acts as a filter for pulses below a minimum pulse width, which is wider as compared to what a gate operating in the regular or the faster process corner would allow to propagate, resulting in some of the narrower transients to disappear in-chain. The impact of these effects compound at

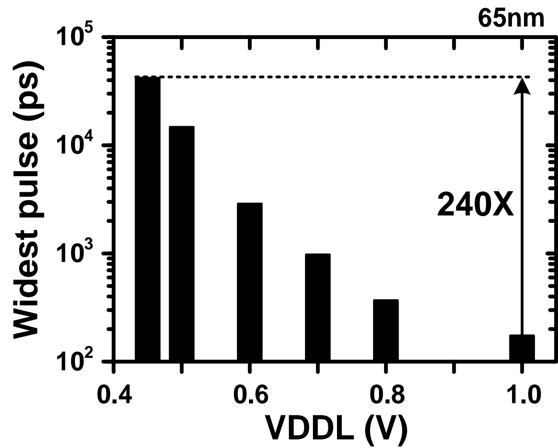


Fig. 9: Widest sampled pulse width as a function of the DUT irradiation voltage used over the experiment duration at LANSCE, showcasing a 240X increase in the pulse width at a NTV level of 0.45V as compared to the nominal supply level (1.0V).

lower supply voltages, for slower drive current variants, total capacitance loading the gate-output, longer chain lengths and the number of active devices directly involved in the transition. The severity of this effect can be especially observed at NTV levels (0.45V, 0.5V) for the 1X HVT flavors (Fig. 8), showcasing distinctly lower pulse-counts at narrower pulse widths for the stacked gates, particularly evident for the weaker NOR gates in comparison to the INVs. The increase in $I_{RESTORE}$ in going from 1X HVT to 2X RVT flavors somewhat offsets this effect, with the NAND gates progressively exhibiting higher pulse-counts in the narrower pulse width regime approaching the INVs, in moving from left to right. However, the NOR gates still show this effect at these low voltages on account of the weaker PMOS stack. Following the same reasoning, INVs exhibit the highest pulse-count for the narrower transients owing to comparatively higher $I_{RESTORE}$, lower overall capacitance loading the gate-output and a single transistor involved in the transition, minimizing the probability of process-variations . Finally, at 1.0V, the impact of this effect is negligible, especially for the stronger 2X HVT and RVT variants (refer to simulated $I_{RESTORE}$ trends [13], showcasing a near-identical $I_{RESTORE}$ for the 2X HVT and RVT variants at 1.0V) as a consequence of the increased $I_{RESTORE}$ improving the gate response time and offsetting both capacitive loading and process-induced variations, resulting in similar sampled pulse-counts for the narrower transients corresponding to the three gate types.

Lastly, Fig. 8 also highlights the impact of increasing the transistor drive strength or the $I_{RESTORE}$. Arranged in the order of increasing drive current strengths at NTV, an increase in the gate drive current results in the distributions to shift leftward to lower pulse widths, with more narrower pulses being sampled for the stronger variant of the same gate type, also attributed in part to the reduction in electrical masking effects (discussed in further detail in the subsequent sections). Fig. 10 further illustrates the sampled pulse widths corresponding to each of the gate types at distinct irradiation voltages in the form of notched box charts, with the aim of providing the reader greater insight into the distribution statistics.

B. V_{TH} Impact

Although prior art [14, 15] has studied the impact of V_{TH} variants on the sampled pulse width distributions, further investigation is required to understand this effect with respect to the different standard logic gate types. Fig. 11 showcases the

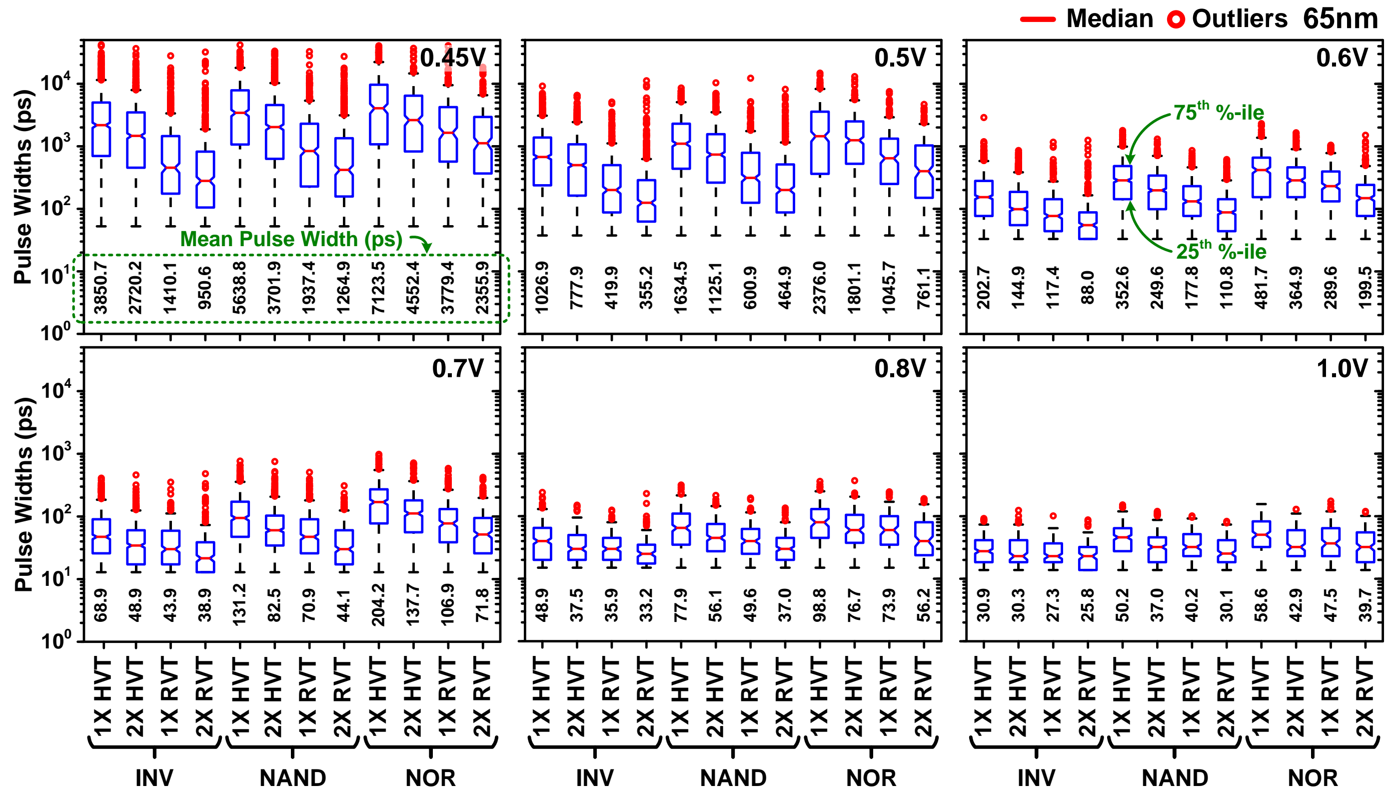


Fig. 10: Notched box charts corresponding to the sampled pulse width distributions illustrated in Fig. 8, detailing the mean pulse widths together with the median, the 25th and the 75th percentile as well as the distribution outliers, presented to provide the reader with a detailed statistical insight.

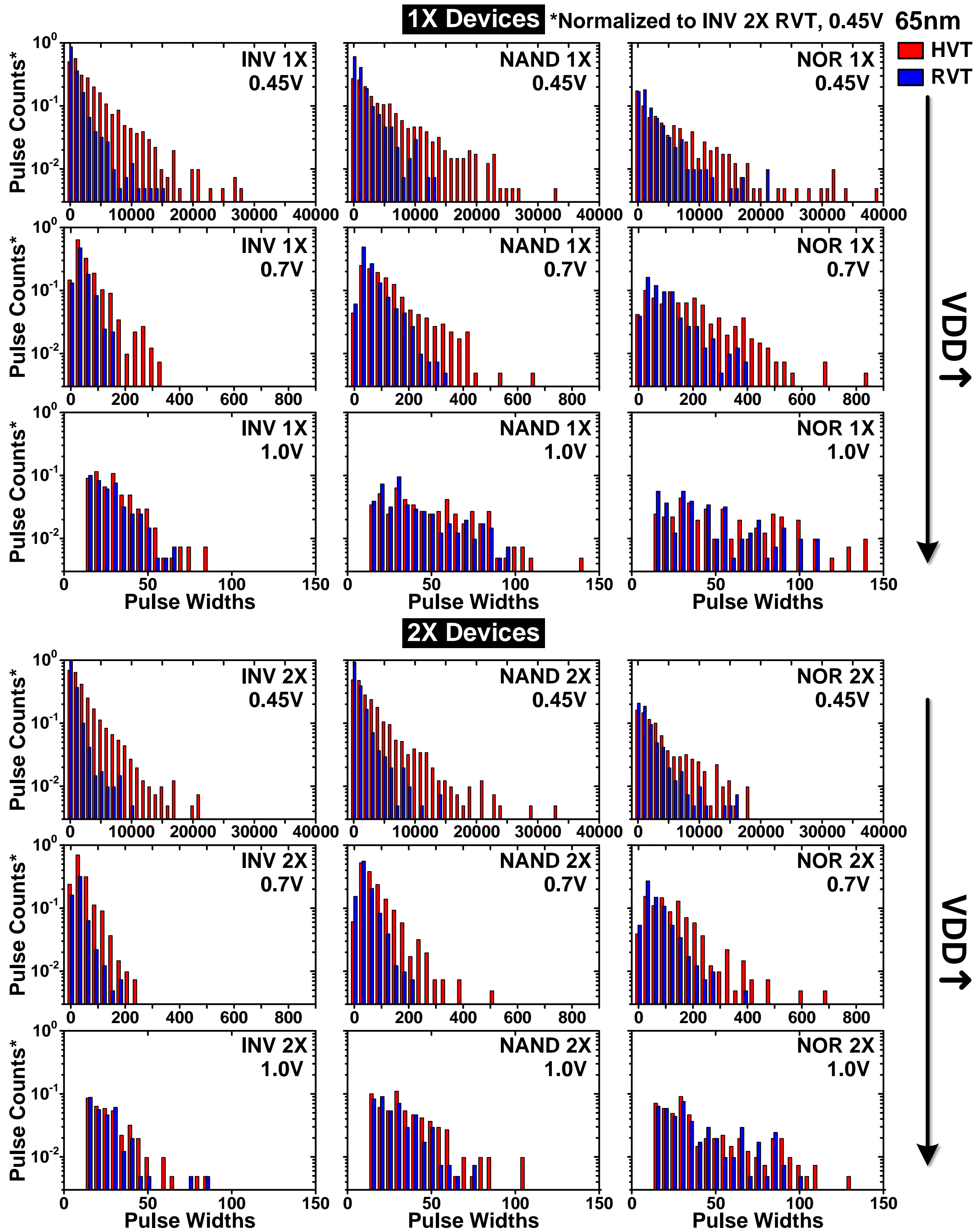


Fig. 11: Sampled pulse width distributions comparing the HVT and the RVT flavors corresponding to the three standard logic gate types at low (0.45V), mid (0.7V) and nominal (1.0V) supply voltages, for the two distinct device width variants.

sampled pulse width distributions for the V_{TH} variants corresponding to three logic gate types at low (0.45V), mid (0.7V), and nominal (1V) supply voltages respectively, presented separately for the distinct device width flavors. Evinced from measured distributions at 0.45V, a change in the V_{TH} variant from HVT to RVT impacts both the SER sensitivity, measured in terms of the sampled pulse-counts, as well as the pulse width distributions, primarily due to the increased $I_{RESTORE}$, with the stronger RVT drive-current variants exhibiting tighter lognormal shaped distributions featuring distinctly lower pulse-counts for wider pulse widths. The increase in VDD, however, offsets this effect, as the relative difference in the overdrive voltage V_{OV} (=$V_{GS} - V_{TH}$) between the two variants starts to level up, as can be observed from measured results at 0.7V, wherein the pulse width distributions for the two variants begin to approach each other.

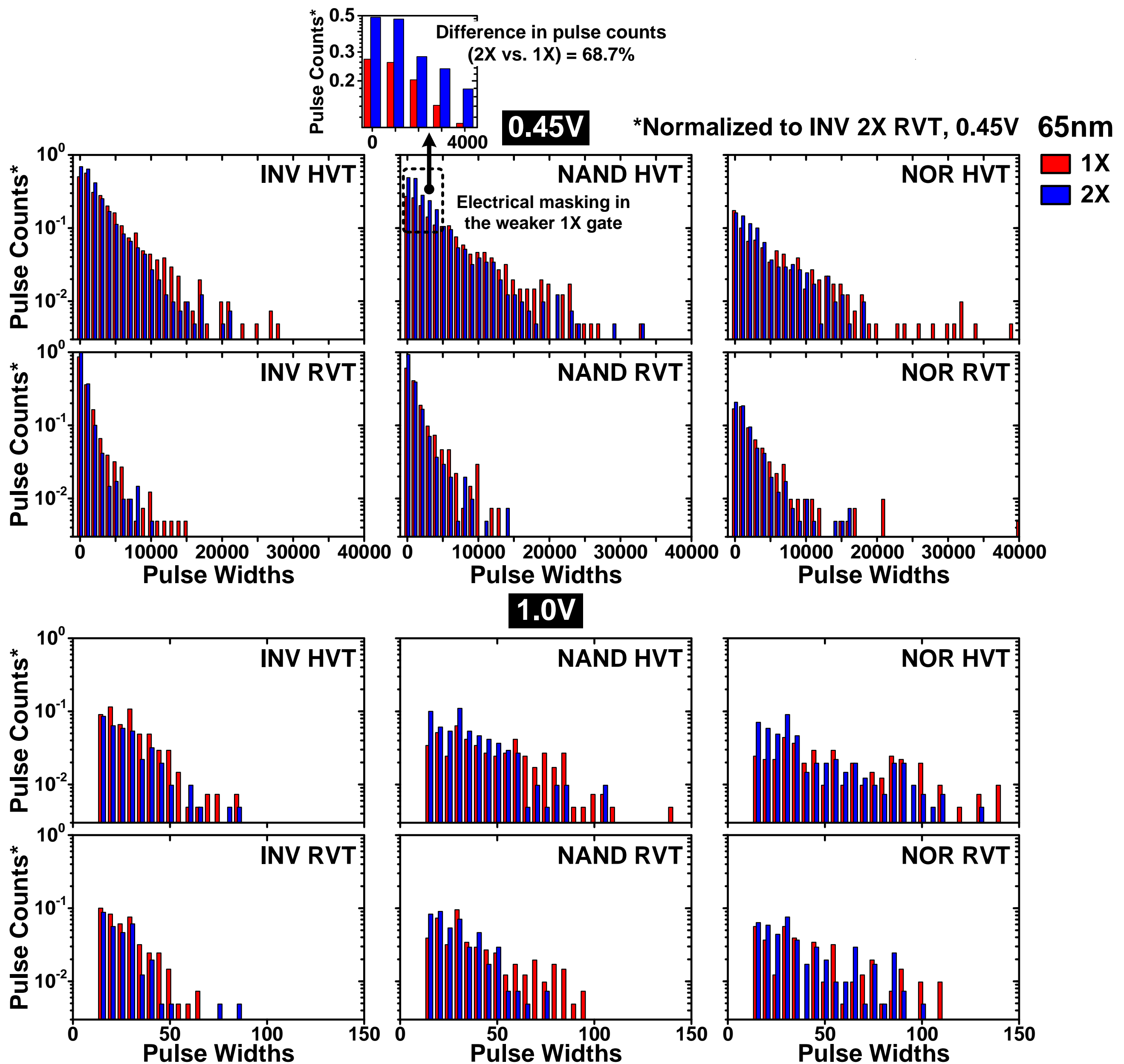


Fig. 12: Sampled pulse width distributions comparing the 1X and the 2X device width flavors corresponding to the three standard logic gate types at low (0.45V) and nominal (1.0V) supply voltages, for the distinct V_{TH} variants.

Finally, at 1.0V, near identical pulse width distributions with similar sampled pulse-counts are observed for all gate types. The aforementioned trends are consistent between the 1X and 2X device width variants (Fig. 11).

Between the three gate types, NANDs and NORs exhibit comparatively wider pulse width distributions in comparison to the INVs, with the effect most noticeable at mid-supply levels of 0.7V, particularly for the weaker 1X NOR gates. This can be attributed to the similarly weak drive current in the three gate types at 0.45V, together with the increase in $I_{RESTORE}$ being dominant at nominal, which results in an almost similar pulse width distribution range between the three gate types at these extremes. Furthermore, it should be noted that at 0.45V, where the difference in the two V_{TH} variants is pronounced, the NOR gates (both the 1X and the 2X variants) exhibit the least difference for a V_{TH} change among the three gate types. This is primarily on account of the weak PMOS stack, which benefits only marginally for a change in the V_{TH}, resulting in similar susceptibility to soft-errors, as well as electrical masking effects in logic-gate chains.

C. *Device width (W) Impact*

Fig. 12 showcases the measured pulse width distributions comparing the transistor-width variants for the three standard logic gate types, presented separately at 0.45V and 1.0V, for the distinct V_{TH} flavors. Compared to a change in V_{TH} (Fig. 11), the increase in device width by a factor of two does not impact the pulse width distributions noticeably at 0.45V (Fig. 12), with the two width variants exhibiting similar lognormal shaped distributions, indicating the $I_{RESTORE}$ to be a weaker function of the device width in the low-voltage regime. In [13], we discussed the impact of device width on the measured SER cross-section results, where it was observed that electrical masking effects progressively dominate as chain length

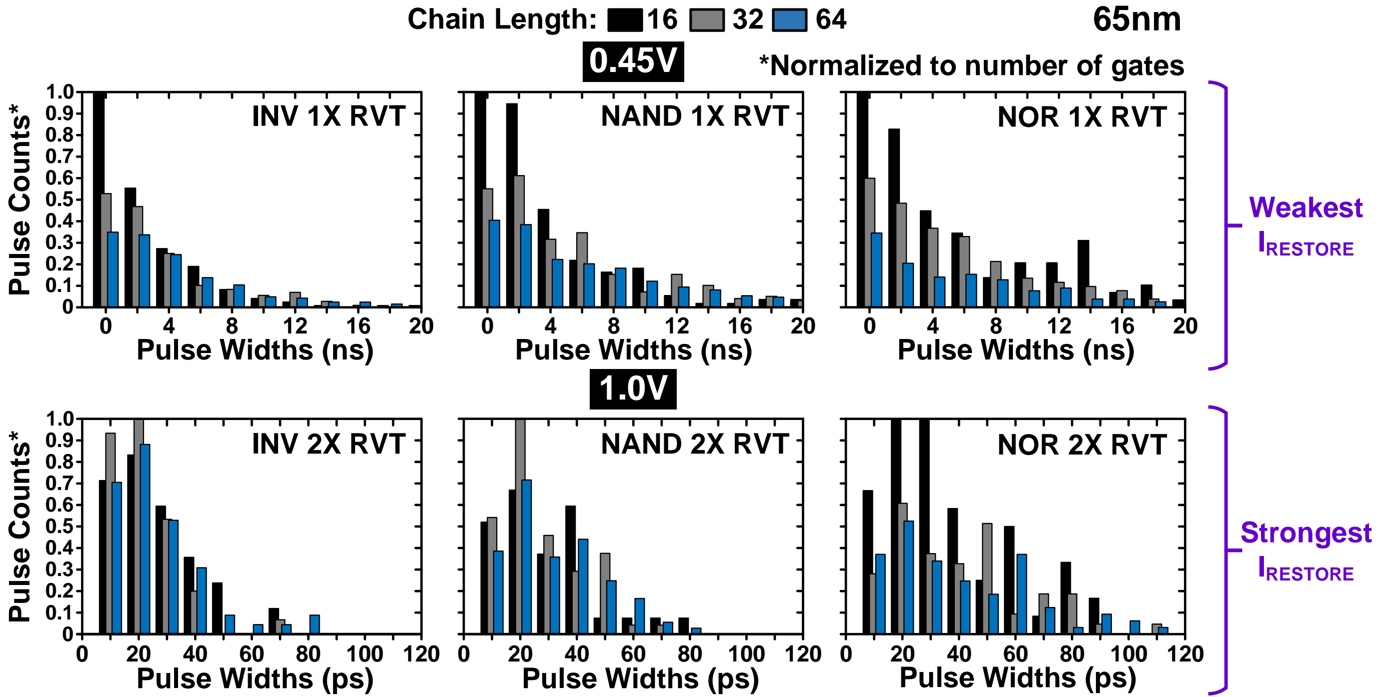


Fig. 13: Sampled pulse width distributions capturing the severity of electrical masking effects in longer gate chains, illustrated for two corner cases: 1X HVT gates at 0.45V and 2X RVT gates at 1.0V, and for chain lengths of 16, 32 and 64 implemented in the 65nm version.

increases from 16 to 64, resulting in a collective higher SER for the 2X versions, especially for the weaker HVT flavors, stacked gate types and at lower supply voltages. Highlighted in Fig. 12, the increase in SER reported in [13] for the 2X flavors, comes about from the loss of several narrower transients in the weaker 1X gates, which attenuate significantly before reaching the detection circuitry, particularly in longer chains (this effect will be isolated further in section D). The severity of this effect reduces in going from the HVT to the RVT variants on account of the increased $I_{RESTORE}$, with a measured 39.5%, 48% and 33.5% reduction in the excess narrower transients at 0.45V for the INV, NAND and NOR, respectively. Among the different gate types at 0.45V, the NOR gates exhibit this effect weakly on account of the comparable $I_{RESTORE}$ in the PMOS stack for the two width variants, whereas the NAND gates exhibit this effect more strongly as compared to the INVs on account of the stacked PDN. Finally, the increase in VDD offsets this effect due to the increased $I_{RESTORE}$, particularly evident for the case of INV DUTs beyond 0.7V (Fig. 11, 12).

D. Logic Chain length Impact

Fig. 13 showcases the impact of logic chain length with the sampled pulse width distributions normalized to the gate count per chain in each of the subfigures. To illustrate the severity of electrical masking and/or pulse quenching effects in longer logic chains, we present results from two corner cases: (1) weakest $I_{RESTORE}$: 1X HVT gates at 0.45V and (2) strongest $I_{RESTORE}$: 2X RVT gates at 1.0V. At 0.45V, the joint impact of weak $I_{RESTORE}$ and process variations (causing delay uncertainty and mismatch between stages), has a pronounced effect on the gate response time, the probability of which compounds with the logic distance travelled, as discussed previously [13], causing several narrower SETs to disappear in-chain. The impact is seen at 0.45V in terms of distinctly higher pulse counts sampled for the narrower transients corresponding to a shorter chain length of the same gate variant. At 1.0V, the increase in $I_{RESTORE}$ results in a shorter gate response time, largely offsetting process variations and loading effects, thus enabling many more narrower pulses to reach the detection circuitry, evinced from similar sampled pulse counts for the three chain lengths corresponding to the 2X RVT variants. It should be noted, however, that NOR gates are still susceptible to these effects even at voltages as high as 1.0V owing to the weak PMOS stack, with the smallest chain length still exhibiting a comparatively higher pulse count as seen from the measured results in Fig. 13.

Finally, Fig. 14(a) presents the averaged pulse widths for the distinct gate variants corresponding to a chain length of 16 at multiple VDDs, with the shorter chain length chosen primarily for a better correlation between the simulated $I_{RESTORE}$ trends and the measured average, minimizing any secondary effects due to process variations, electrical masking and exposed diffusion areas etc., creeping in at longer chain lengths of 32 and 64. The results agree well with the $I_{RESTORE}$ simulations we presented in [13], especially for INV DUTs, due to a reduced susceptibility to masking effects as compared to stacked gates. Fig. 14(b) presents the measured averaged pulse width results for logic gates variants considered collectively, indicating the movement of the distribution towards a higher average value with increase in chain length, again a consequence of electrical masking effects.

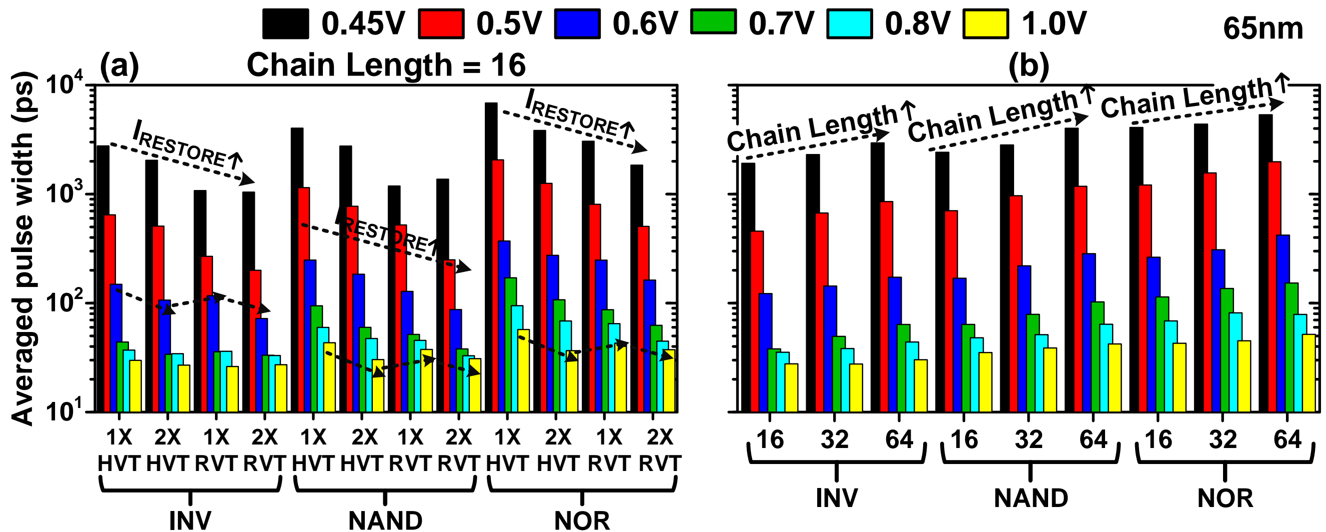


Fig. 14: Averaged pulse widths: (a) indicating the $I_{RESTORE}$ dependence which agrees well with the simulation results presented previously [13], and (b) impact of increasing chain length on the measured averaged pulse width.

E. 65nm Planar CMOS Vs. 16nm FinFET

Finally, Fig. 15 presents the sampled pulse width distributions comparing the 65nm planar CMOS and the 16nm FinFET implementations of the proposed concept, with the standard logic gate variants biased at half the nominal VDDs (technologically identical bias points), and with the pulse-counts normalized to the total number of gates. The FinFETs demonstrate better immunity to soft-errors compared to their planar CMOS equivalents, in agreement with the previously reported data [1-3, 6-10]. Furthermore, even though the two implementations differ in terms of the logic chain lengths (16, 32, 64 for the 65nm version and 128 for INV, 96 for NAND/NOR for the 16nm implementation) and input connections (for NAND/NOR gates), making a one to one comparison difficult, measured SER trends [13] as well as the pulse width distributions at half the nominal VDD still exhibit strikingly similar trends between the three gate types outlined in previous subsections.

V. Conclusion

In this work, we presented detailed neutron-irradiation data, for the three standard logic gate types ubiquitous in digital designs, highlighting the principle utility of our proposed test-vehicle, first introduced in [13]. The corresponding sampled pulse width distributions were compared among the different gate types and analyzed closely in relation to the logic design parameters impacting them, such as the VDD, V_{TH}, device width and the logic chain length. The aim of the discussion was to develop an insight of the design choices impacting the sampled pulse width distributions in relation to the standard gates. The discussion is particularly relevant for digital designs where multiple domains operate at distinct VDDs, owing to dynamic voltage and frequency scaling and all standard logic gate types are distributed throughout the logic.

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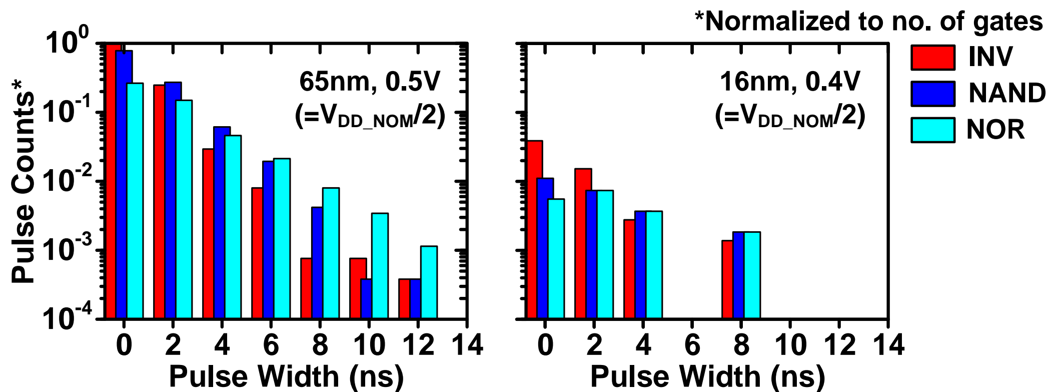

Fig. 15: Measured pulse width distributions for the standard logic gate variants considered collectively and illustrated above for the 65nm planar CMOS version (left), and the 16nm bulk FinFET version (right), at technologically identical bias points viz. half the nominal VDD.

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