An All BTI (N-PBTI, N-NBTI, P-PBTI, P-NBTI) Odometer based on a Dual Power Rail Ring Oscillator Array

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Purpose

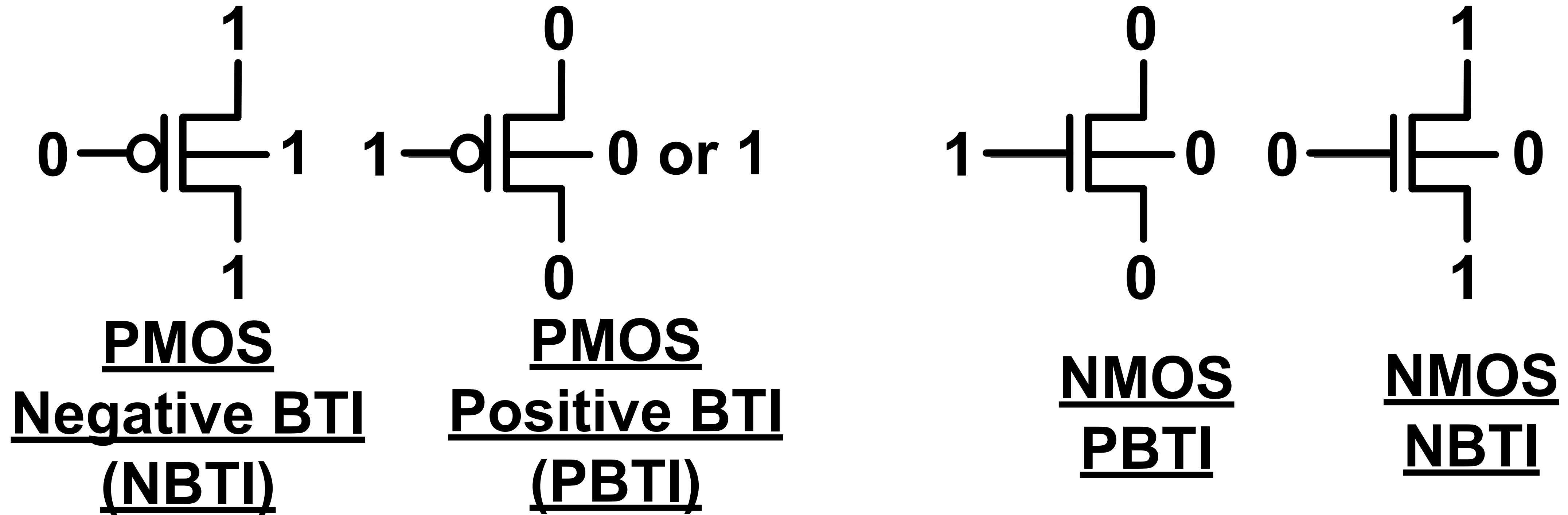
- **A new dual-power rail odometer circuit for separating different Bias Temperature Instability (BTI) effects**

- **Characterization of different BTI modes (i.e. PMOS NBTI/PBTI, NMOS NBTI/PBTI)**

Outline

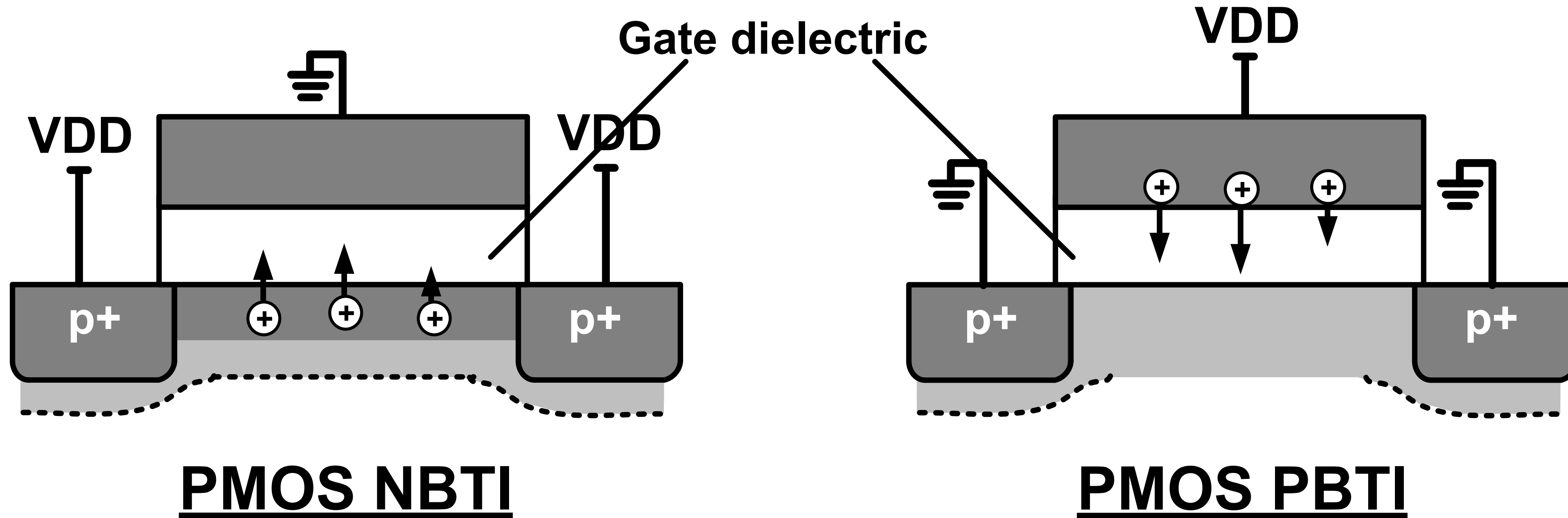
- Motivation
- Proposed all BTI odometer concept
- 65nm odometer chip test results
- Conclusions

Bias Condition for All 4 BTI Stress



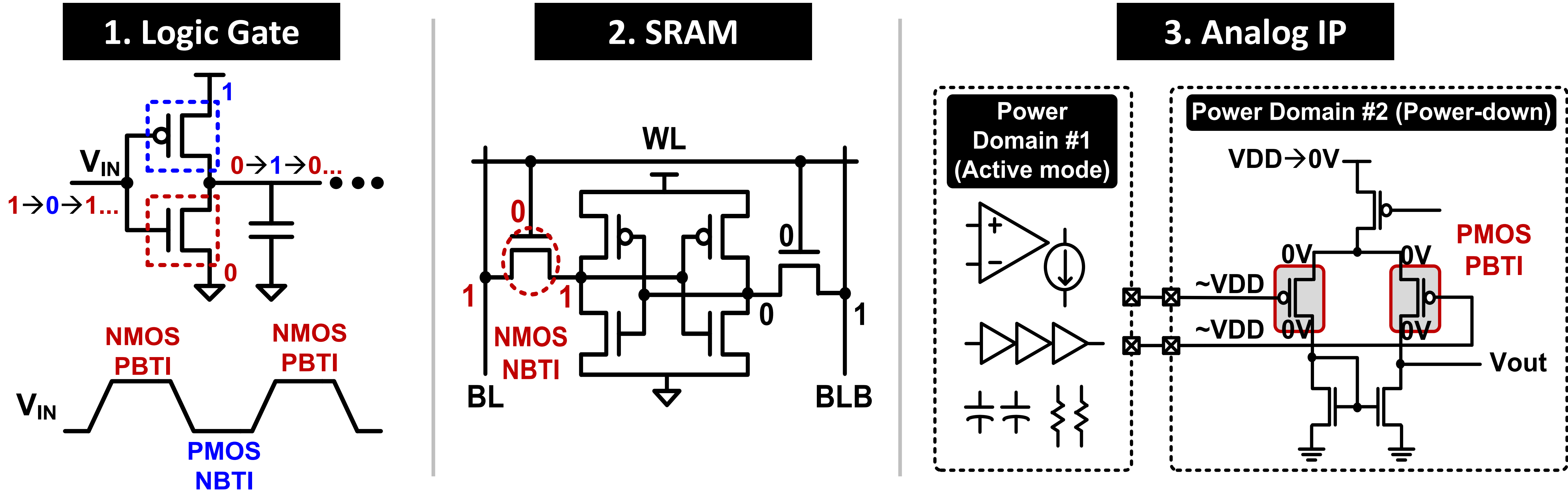
- Negative gate voltage w.r.t. drain-source/body → NBTI on P/NMOS
- Positive gate voltage w.r.t. drain-source/body → PBTI on P/NMOS

BTI Aging Mechanism



- PMOS NBTI: positive channel carriers get captured in dielectric/interface
- PMOS PBTI: positive poly/metal carriers get captured in dielectric/interface
- Both NBTI and PBTI increase |Vth|
- NMOS also follows similar mechanism with negative carriers

Different BTI Modes in Real Designs



- Different circuits in the same chip can be exposed to different BTI modes
- No prior works on separately monitoring circuit degradation caused by each BTI mode

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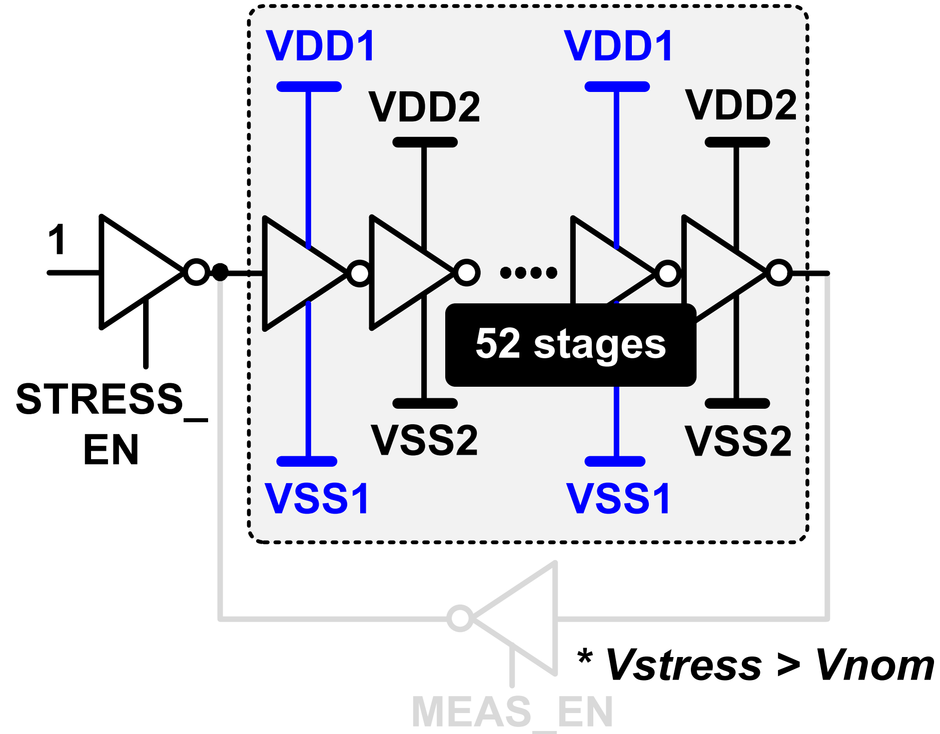
Proposed Dual Power Rail ROSC in Stress Mode

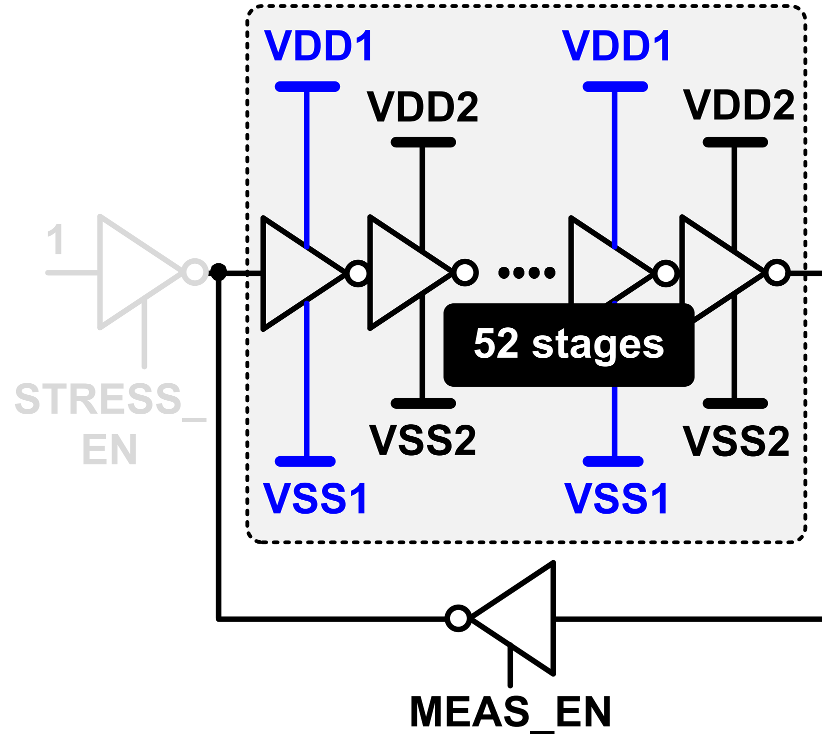


Mode 1	PMOS NBTI + NMOS PBTI
Mode 2	Mode1 + PMOS PBTI
Mode 3	Mode1 + NMOS NBTI
Mode 4	Mode1 + PMOS PBTI + NMOS NBTI

Power Supply Conditions				
Stress Mode	VDD1	VSS1	VDD2	VSS2
Mode 1	Vstress	0	Vstress	0
Mode 2	Vstress	0	0	0
Mode 3	Vstress	Vstress	Vstress	0
Mode 4	Vstress	Vstress	0	0
Meas. Mode	Vnom	0	Vnom	0

- Dual power rails, a 52 stage inverter chain, and two tri-state inverters.
- VDD1,VSS1 for odd stages, VDD2, VSS2 for even stages
- 4 power configurations to apply 4 stress modes.
- In stress mode, ROSC configured as an open loop inverter chain.

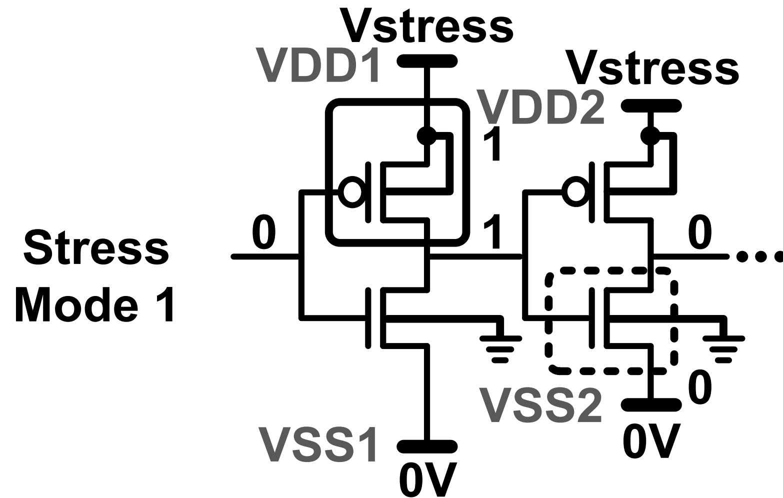
Proposed Dual Power Rail ROSC in Meas. Mode



Power Supply Conditions				
Stress Mode	VDD1	VSS1	VDD2	VSS2
Mode 1	Vstress	0	Vstress	0
Mode 2	Vstress	0	0	0
Mode 3	Vstress	Vstress	Vstress	0
Mode 4	Vstress	Vstress	0	0
Meas. Mode	Vnom	0	Vnom	0

- In measurement mode, inverter chain configured as a ROSC.
- Power rail voltages switched to nominal VDD and VSS.
- Measure ROSC frequency to detect Vth degradation of inverters.

Two Stages of Dual Power ROSC in Stress Mode 1



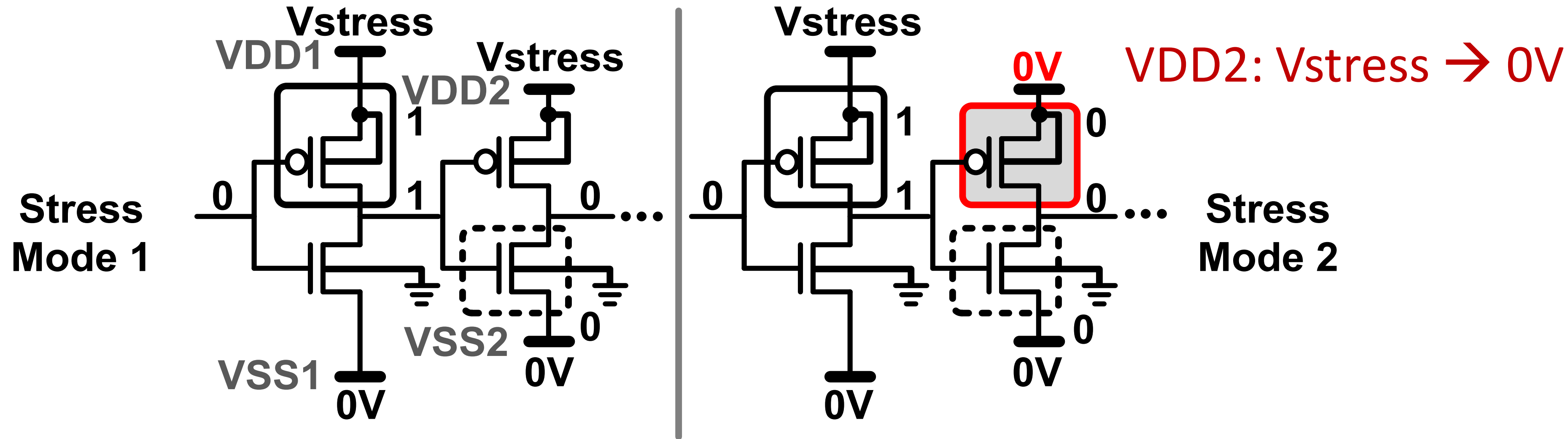
VDD1=VDD2=Vstress (> Vnom)
VSS1=VSS2=0V

PMOS NBTI in 1st stage
NMOS PBTI in 2nd stage.

- Stress mode 1 represents typical stress condition of an inverter circuit

Two Stages of Dual Power ROSC in Stress Mode 2

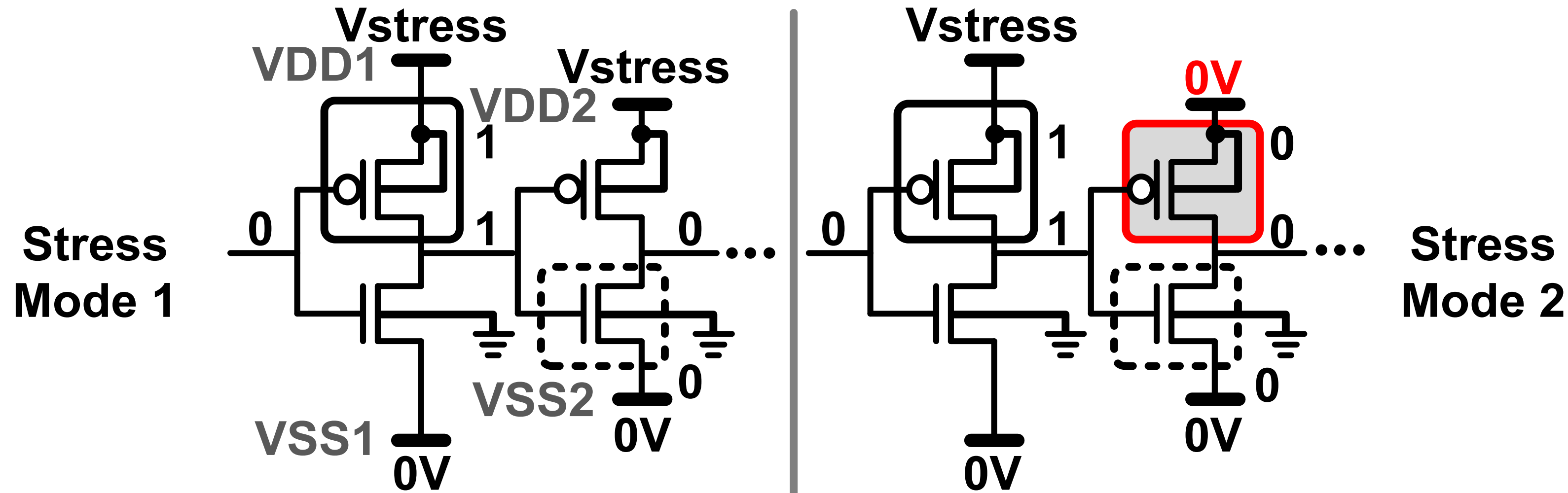
PMOS NBTI NMOS PBTI PMOS PBTI

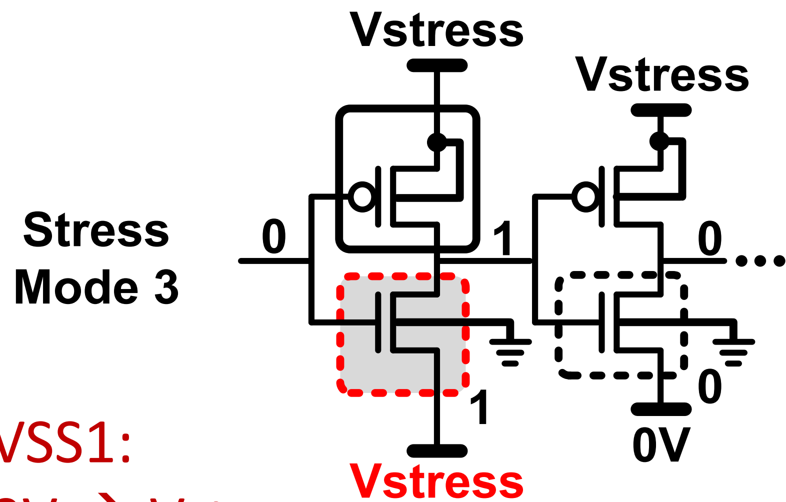


- In stress mode 2, VDD2 switched to 0V → PMOS PBTI added in 2nd stage
- Thus, mode1 stress + PMOS PBTI
  - PMOS NBTI in 1st stage
  - NMOS PBTI + PMOS PBTI in 2nd stage

Two Stages of Dual Power ROSC in Stress Mode 3

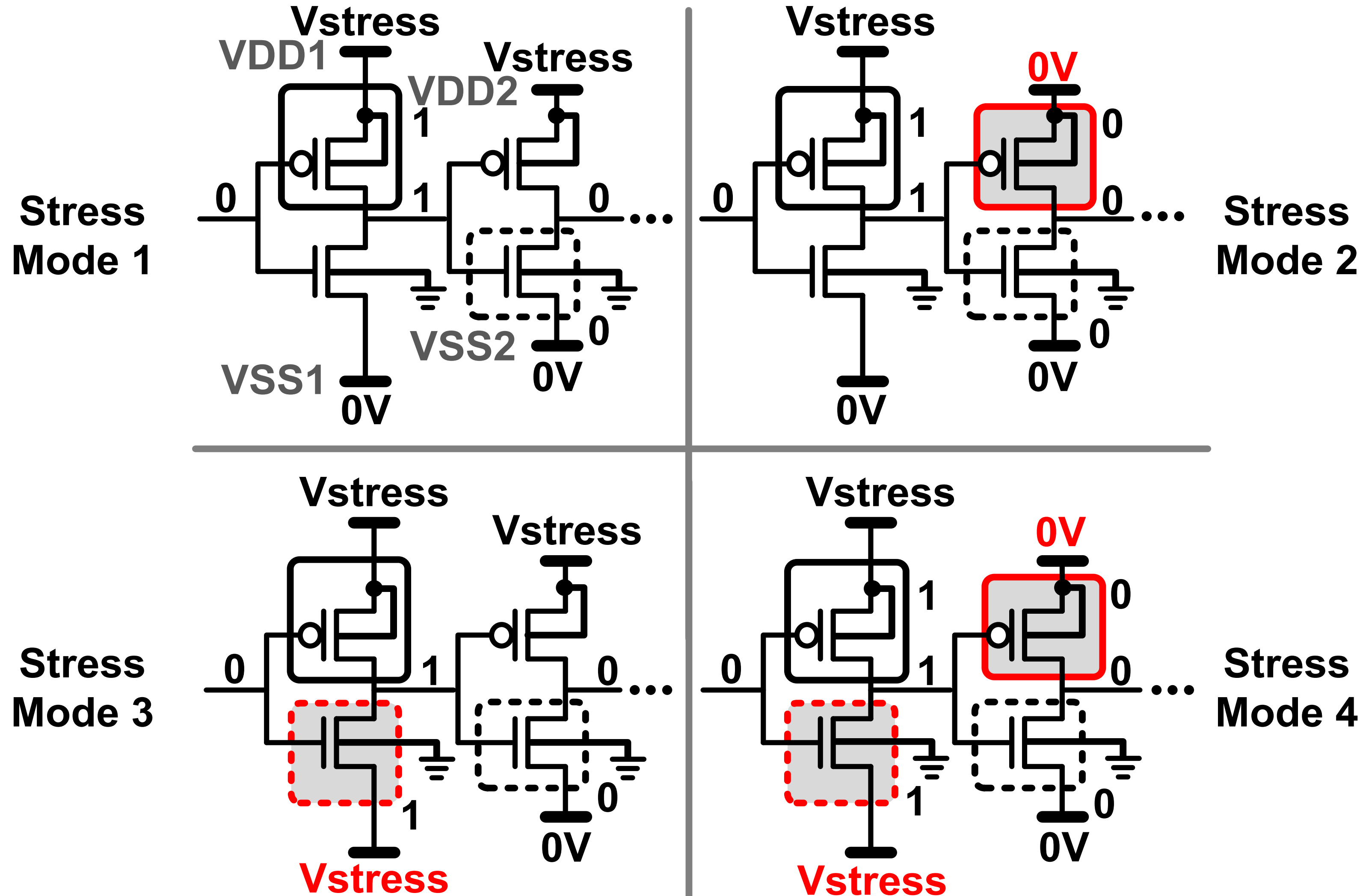
PMOS NBTI　NMOS PBTI　PMOS PBTI　NMOS NBTI





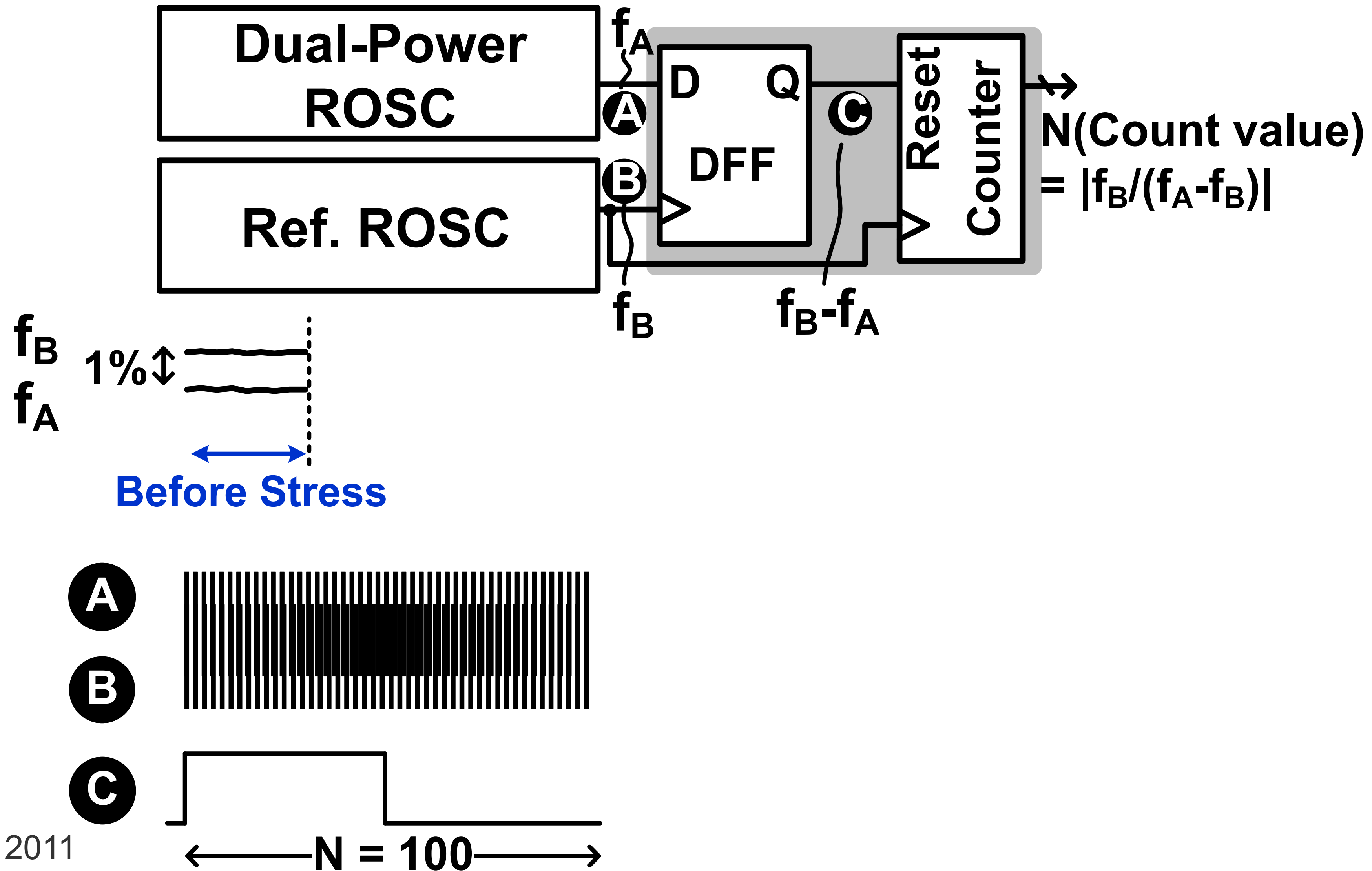
- In stress mode 3, VSS1 switched to Vstress
- Mode1 stress + NMOS NBTI
    - PMOS NBTI + NMOS NBTI in 1st stage
    - NMOS PBTI in 2nd stage

Two Stages of Dual Power ROSC in Stress Mode 4



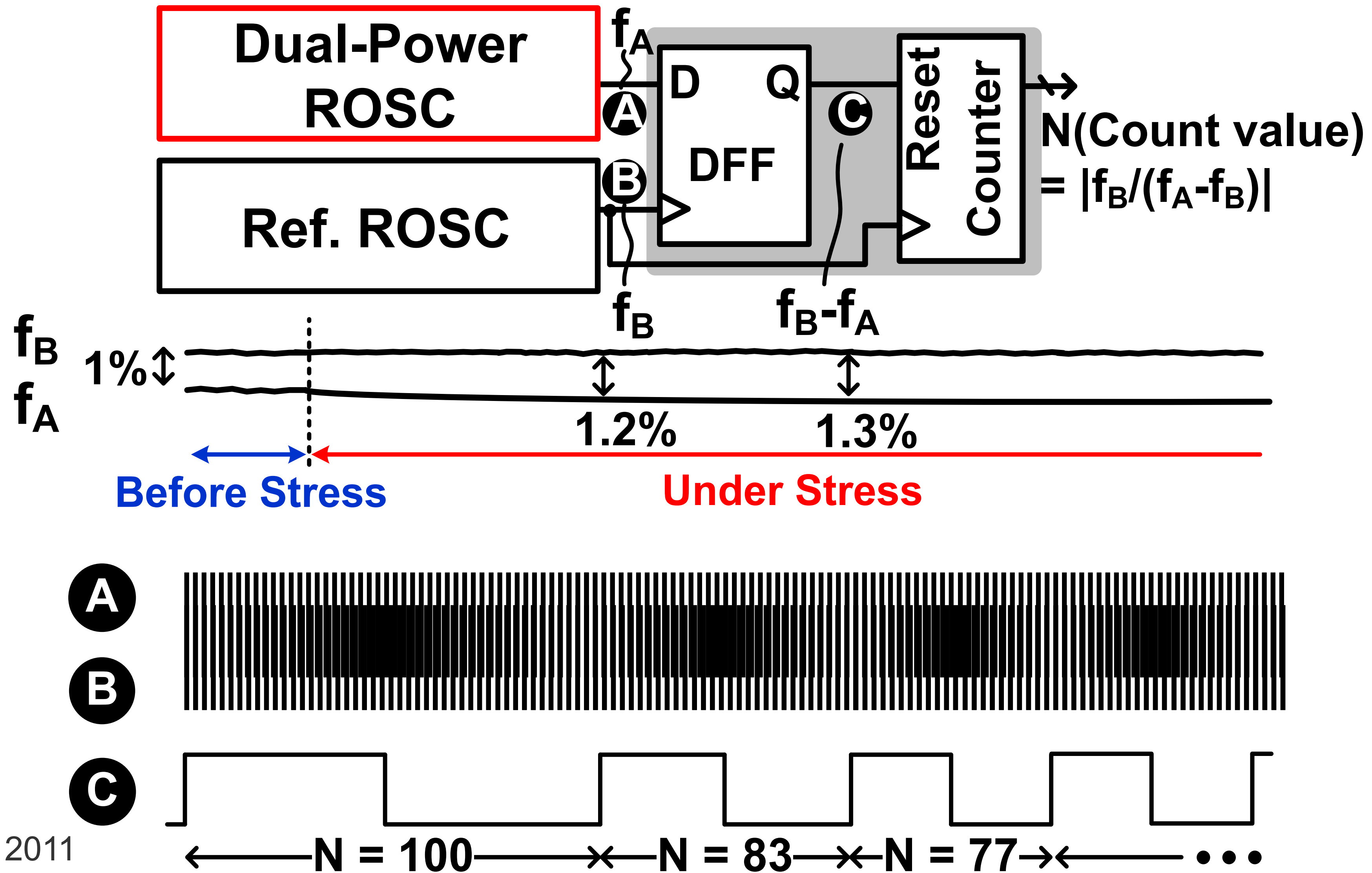
- In stress mode 4, all four devices undergo BTI stress
- Δf between the 4 stress modes → Individual BTI components

Beat Frequency Detection (BFD) Before Stress



J. Keane, et al., JSSC, 2011
J. Keane, et al., JSSC, 2010
T. Kim, et al., JSSC, 2008

Beat Frequency Detection (BFD) Under Stress



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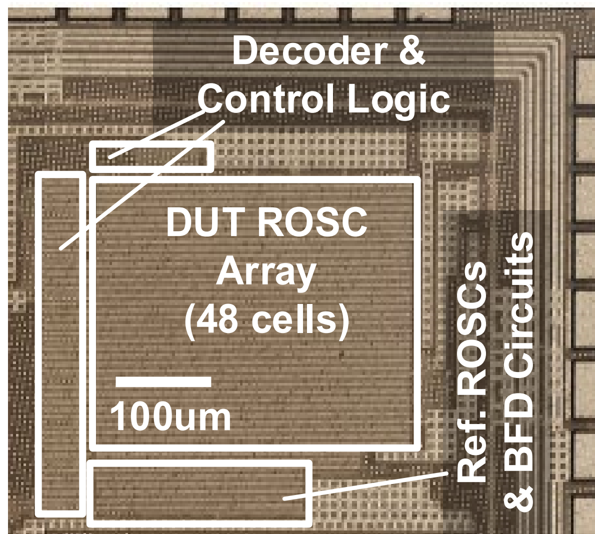
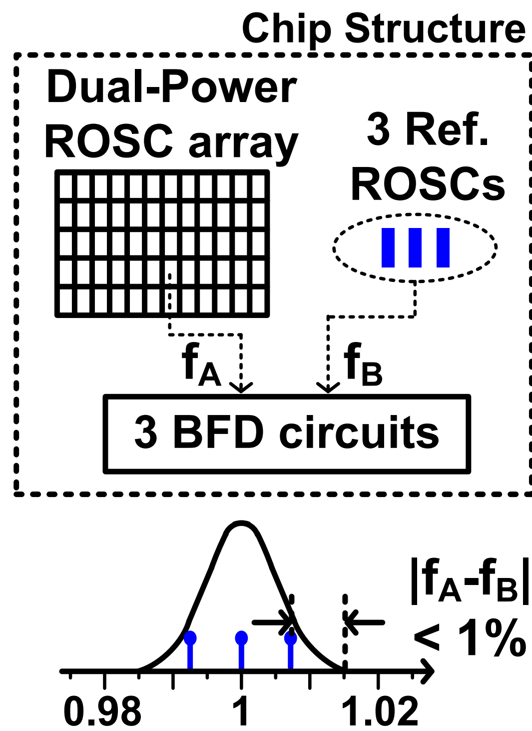
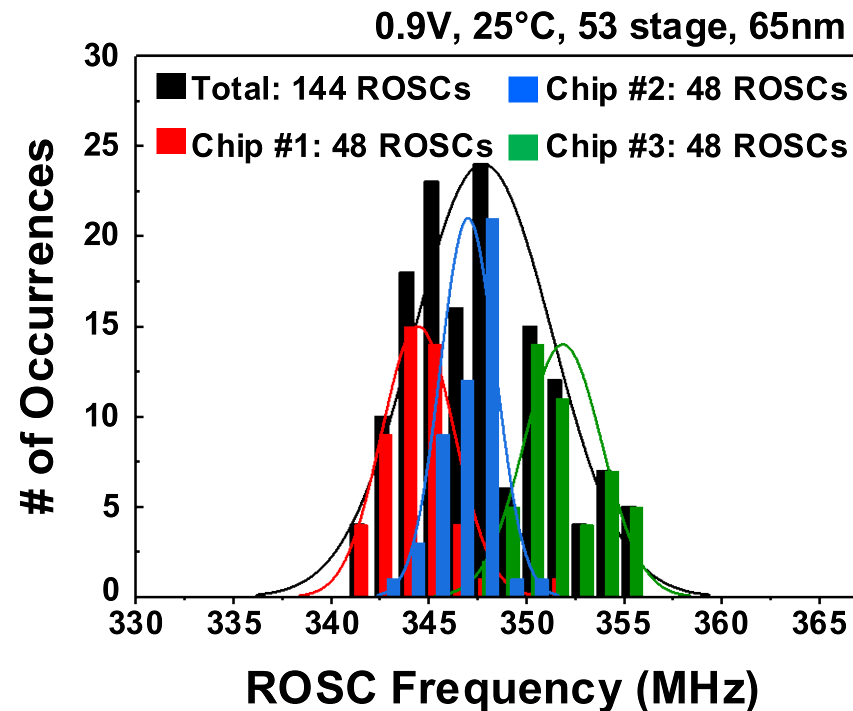
3 Reference ROSCs & Initial Frequency Distribution

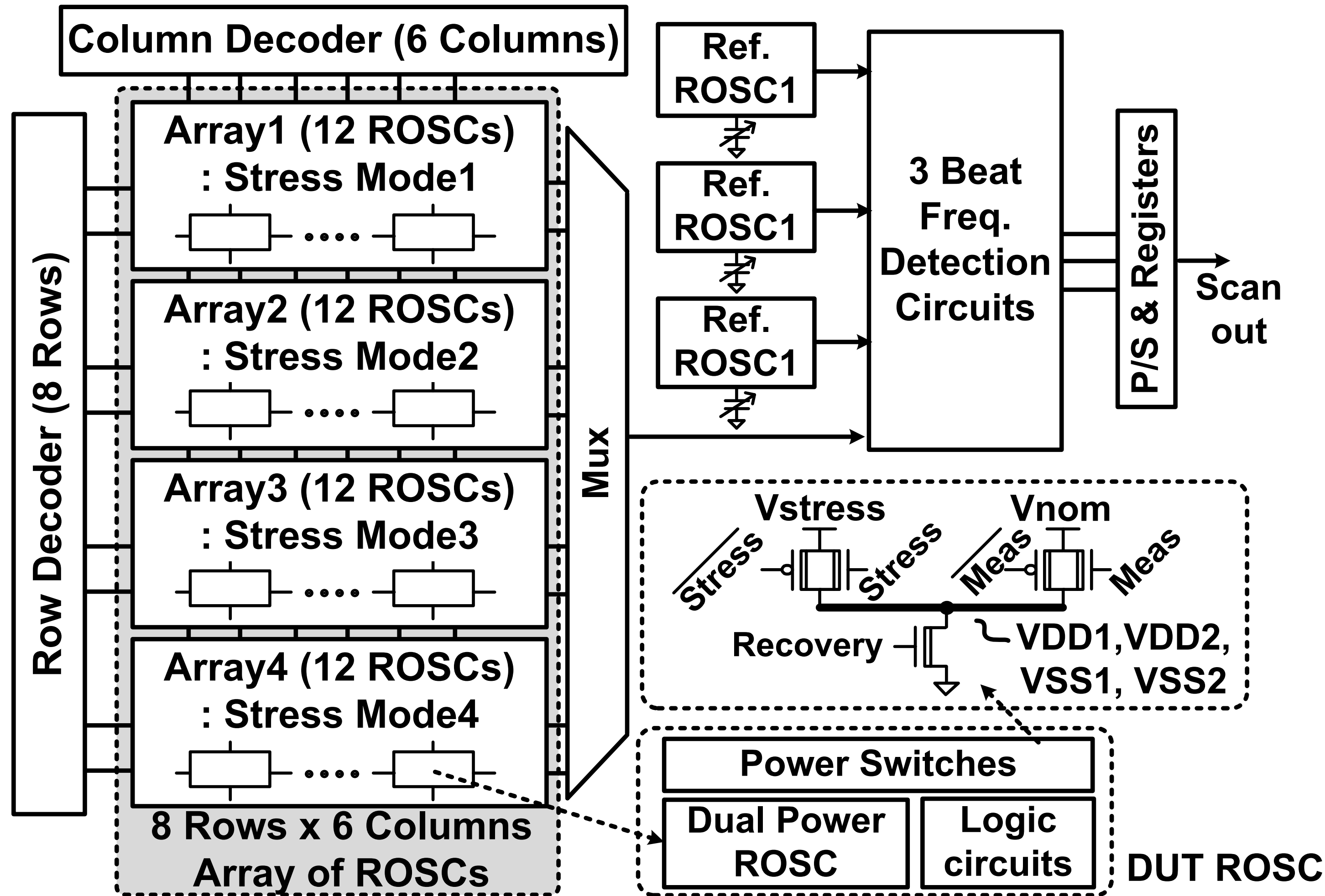






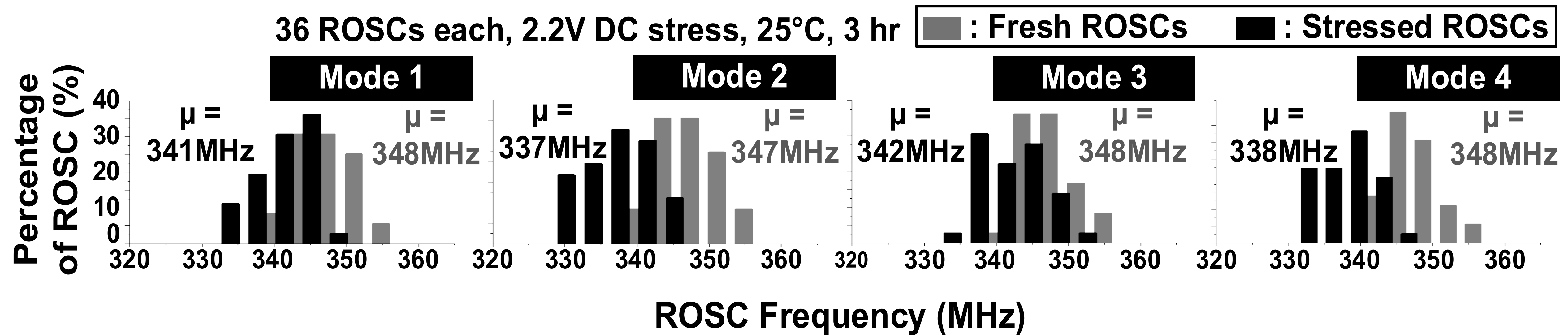
- 3 ref. frequencies separated using on-chip trimming capacitors to cover the frequency range (~3%) of the ROSC array
- Of the 3 beat frequency counts, choose the one giving the highest resolution
- Before applying stress, measure frequency distribution of fresh DUTs

Test Chip Organization: 12x4 ROSC Array



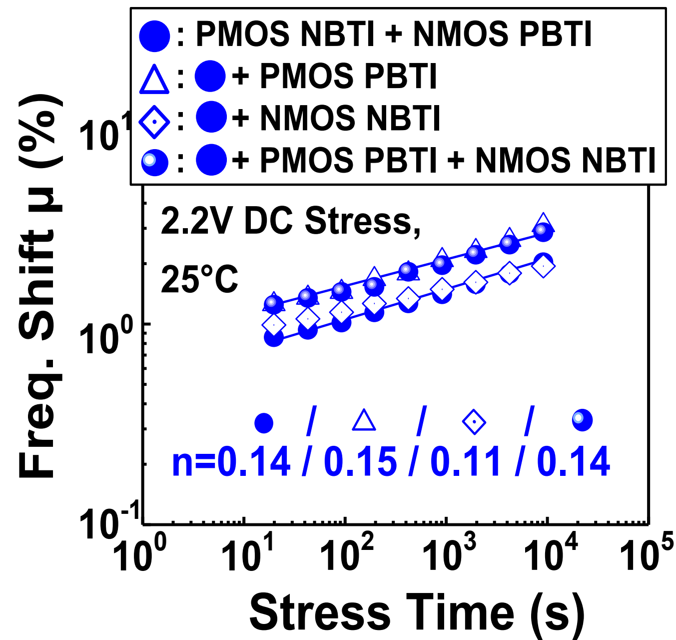
- 48 ROSC array grouped into four 12 ROSC sub-arrays
- Each sub-array assigned to one of the 4 stress modes
- 3 reference ROSCs + 3 parallel BFD circuits
- Power switches control two VDD and VSS pairs according to stress modes

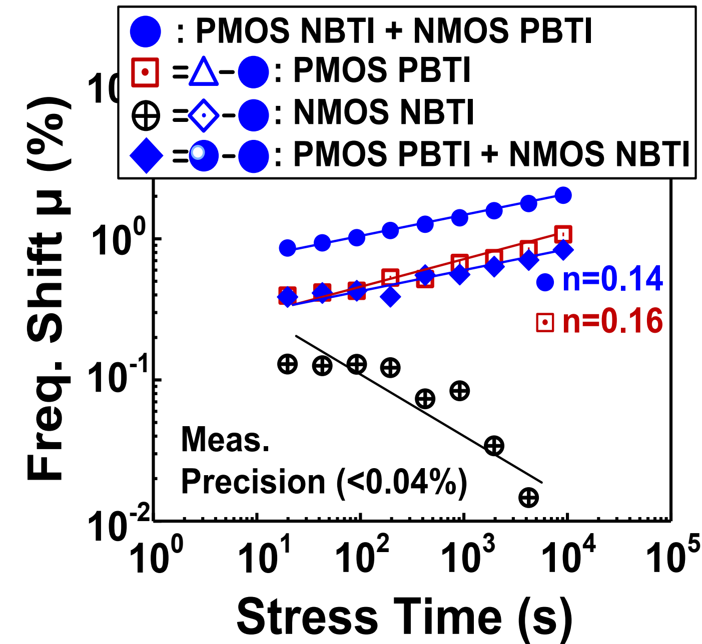
Frequency Distributions After 3 Hours of Stress



- Freq. shift of stress mode2 (Δf =2.88%) & mode4 (Δf=2.87%) > stress mode1 (Δf=2.01%) → additional PMOS PBTI
- Freq. shift of stress mode3 (Δf =1.72%) ≈ stress mode1 (Δf=2.01%)
  → NMOS NBTI is negligible compared to PMOS PBTI

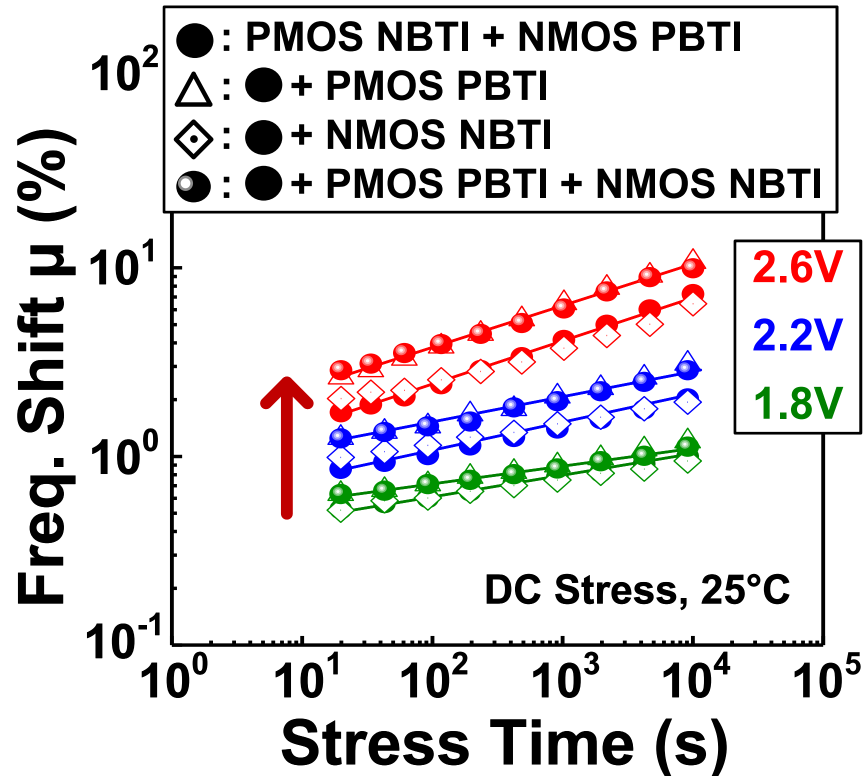
Frequency Shift Data for 2.2V DC Stress, 25°C

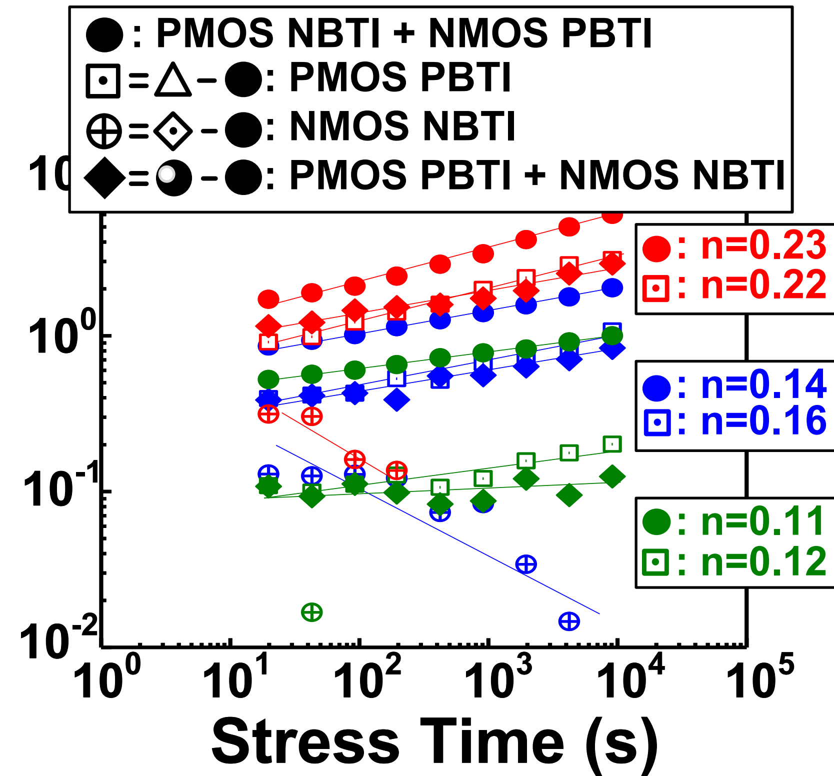




- 'P-NBTI + N-PBTI' and 'P-PBTI' → freq. shift increase
- N-NBTI shows two different trends
  - Short-term: increase in frequency shift / Long-term: decrease in frequency shift
- Stress effect in early stage: P-NBTI + N-PBTI(~7x) > P-PBTI (~3x) > N-NBTI (1x)

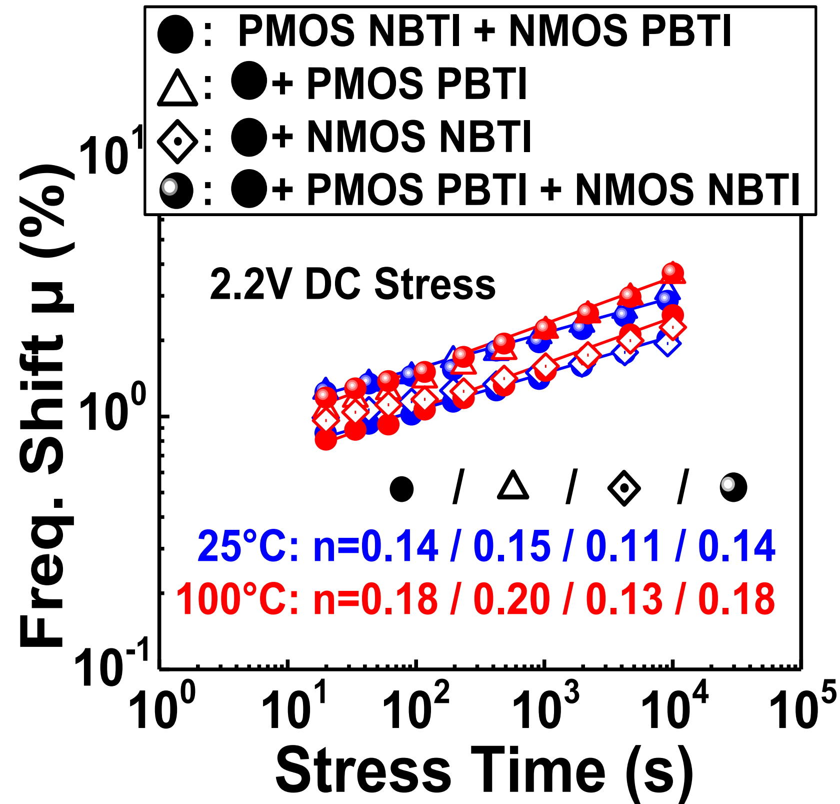
Frequency Shift Data Under Different Stress Voltages

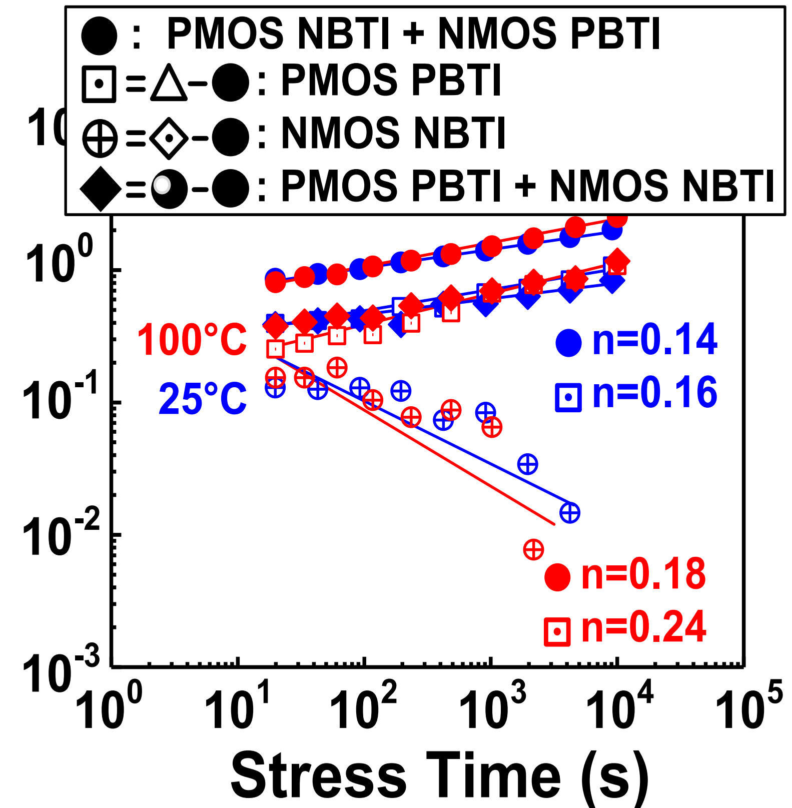




- Larger frequency shift at a higher stress voltage for all 4 stress modes

Frequency Shift Data at 25°C and 100°C





- Slightly higher time exponent at higher temperatures for different BTI modes

Conclusions

- New odometer circuit capable of separating different BTI modes
  - Dual power rails
  - Beat frequency detection technique
- Statistical frequency shift data collected from a 65nm all BTI odometer test chip
  - P-NBTI + N-PBTI : P-PBTI : N-NBTI = ~7 : ~3 : 1

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