An All BTI (N-PBTI, N-NBTI, P-PBTI, P-NBTI) Odometer based on a Dual Power Rail Ring Oscillator Array

Gyusung Park
Intel Corporation (this work was done during PhD studies at the University of Minnesota)
2501 NE Century Blvd, Hillsboro, OR 97124, USA
e-mail: park1582@umn.edu / gyusung.park@intel.com

Hanzhao Yu, Minsu Kim, and Chris H. Kim
Department of Electrical and Computer Engineering, University of Minnesota
200 Union Street SE, Minneapolis, MN 55455, USA

***Abstract*— An on-chip reliability monitor capable of characterizing all four bias temperature instability (BTI) modes is proposed. Stressed ring oscillators with independent dual power rails are implemented in which odd and even stages of an inverter chain are subject to different stress voltage configurations. A beat frequency detection technique with 3 reference ring oscillators achieves a frequency measurement resolution as low as 0.01% with a short measurement interruption time of 4µs. Extensive BTI data collected from a 65nm ROSC array is presented for different stress conditions.**

Keywords –Bias temperature instability (BTI); odometer; dual power rail; ring oscillator array

I. INTRODUCTION

Parametric shifts caused by negative and positive bias temperature instabilities (NBTI and PBTI) have become a growing concern in advanced CMOS technologies. Without the necessary timing or voltage guardbands, these reliability mechanisms can cause premature circuit failures. Fig. 1 shows the bias condition of the four different BTI modes. When a device is biased in strong inversion mode, PMOS and NMOS devices undergo NBTI and PBTI stresses, respectively, whereas in accumulation mode, the devices experience PBTI and NBTI, respectively. Previous works have shown that the device current decreases for all four BTI modes [1]. PMOS NBTI and NMOS PBTI have been extensively studied as they affect the performance of digital logic or memory circuits during normal operation [2-5]. In contrast, very few papers have shown the impact of PMOS PBTI and NMOS NBTI on circuit operation since these mechanisms mainly occur under specific operating scenarios in mixed-signal circuits [6][7]. Also, [1] shows PMOS input transistors in analog circuits such as op-amp can be exposed to PBTI in power down mode. Despite the importance of this stress mode for mixed-signal applications, no circuit level measurements have been reported on PMOS PBTI or NMOS NBTI. Most of the previous works focus on device level measurements and modeling aspects of these two BTI modes.

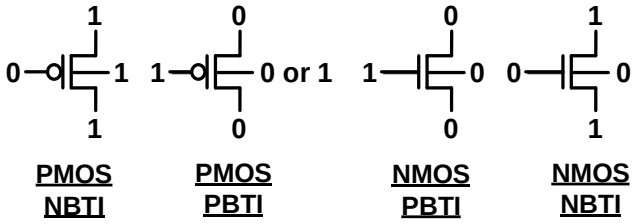
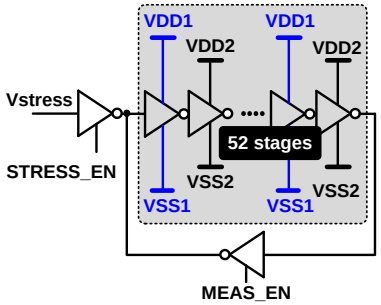


Fig. 1. Bias condition for all four BTI modes.

In this work, we demonstrated for the first time, an on-chip beat frequency based monitor circuit capable of separately characterizing frequency shifts caused by all four BTI modes. The main idea of the design is a ring oscillator



Mode 1	PMOS NBTI + NMOS PBTI
Mode 2	Mode1 + PMOS PBTI
Mode 3	Mode1 + NMOS NBTI
Mode 4	Mode1 + PMOS PBTI + NMOS NBTI

Power Supply Conditions				
Stress Mode	VDD1	VSS1	VDD2	VSS2
Mode 1	Vstress	0	Vstress	0
Mode 2	Vstress	0	0	0
Mode 3	Vstress	Vstress	Vstress	0
Mode 4	Vstress	Vstress	0	0
Meas. Mode	Vnom	0	Vnom	0

Fig. 2. (left) Proposed dual power rail ROSC. (middle) BTI stress modes. (right) Power supply configuration

(ROSC) circuit with dual power rails enabling different BTI stress modes. The proven-and-tested beat frequency detection scheme achieves a high frequency measurement precision (>0.01%) with minimal unwanted device recovery during measurements owing to the short microsecond-order stress interrupt time [8-11].

II. DUAL POWER ROSC STRUCTURE AND BEAT FREQUECY CIRCUIT

A. *Test ROSC Supporting Four BTI Stress Modes*

The proposed ROSC circuit shown in Fig. 2 consists of two power rails, a 52 stage inverter chain, and two tri-state inverters. During stress mode, the ROSC is configured as an open loop inverter chain whose input is set to 0V. To apply different BTI stress modes to the inverter chain, two sets of power supplies are used; VDD1 and VSS1 for odd inverter stages and VDD2 and VSS2 for even inverter stages. In measurement mode, the inverter chain is configured into a ROSC and the power rail voltages are switched to the nominal VDD and VSS voltages.

Fig. 3 shows the transistor-level schematic of two ROSC stages for the 4 distinct stress modes. Stress mode 1 represents the typical stress condition of an inverter circuit with VDD1=VDD2=Vstress and VSS1=VSS2=0V. This induces PMOS NBTI in the first stage and NMOS PBTI in the second stage. In stress mode 2, VDD2 is switched to 0V which induces PMOS NBTI in the first stage and PMOS PBTI in the second state. VSS1 is switched to Vstress in stress mode 3 which results in PMOS NBTI and NMOS NBTI in the first stage, and NMOS PBTI in the second stage. Finally, in stress mode 4, all four devices undergo BTI stress using the specific stress voltage configuration in Fig. 3 (lower right). The individual BTI components can be obtained by taking the difference between the measured frequency shifts of the respective stress modes. In our

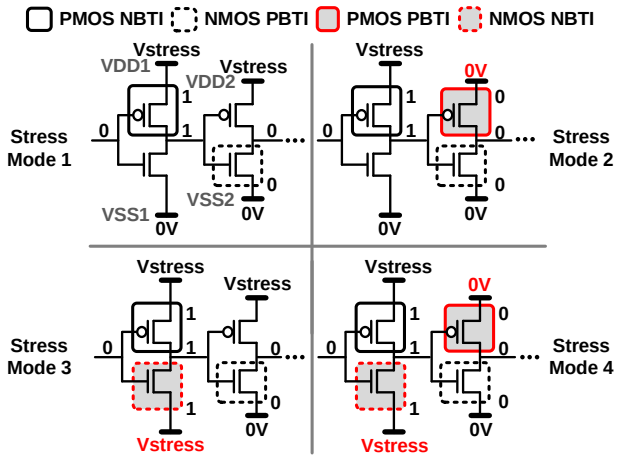


Fig. 3. (a) Stress mode 1, (b) stress mode 2: stress mode 1 + PMOS PBTI, (c) stress mode 3: stress mode 1 + NMOS NBTI, (d) stress mode 4: stress mode 1 + PMOS PBTI + NMOS NBTI.

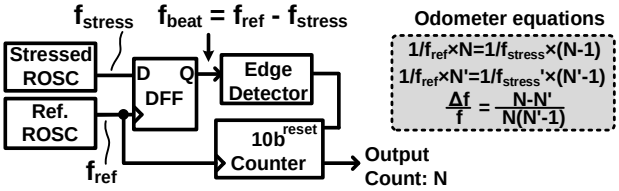


Fig. 4. Frequency degradation monitor based on the silicon odometer beat frequency detection (BFD) scheme.

implementation, the PMOS body was tied to the source terminal so Vstress is applied between the gate terminal and the other three terminals (i.e. source, drain, body) of the PMOS device. On the other hand, NMOS body is connected to 0V so Vstress is applied between the gate terminal and the source/drain terminals (not body terminal) during NMOS NBTI stress mode.

B. *Array based Beat Frequency Measurement Circuit*

Fig. 4 shows the beat frequency detection (BFD) circuit for measuring the frequency shift of the stressed ROSC [8]. The output signal of the D-flip-flop exhibits the beat frequency, fbeat = fref - fstress. The beat frequency between the stressed and reference ROSC is measured by counting the number of reference ROSC periods that can fit within one period of the phase comparator output signal. Using the 10 bit output codes (e.g. N: the output codes before stress, and N': the output codes after stress), we can compute the frequency shift of the stressed ROSC with picosecond accuracy [8-10].

The top level diagram of the 65nm test vehicle is shown in Fig. 5. It consists of a 48 ROSC array grouped into four 12 ROSC sub-arrays, 3 reference ROSCs, and 3 parallel BFD circuits. Each sub-array is assigned to one of the four different stress modes, and power switches control the two VDD and VSS pairs depending on the stress mode. Before applying stress, we measured the frequency distribution of fresh DUTs. The frequencies of the three reference ROSCs were separated using on-chip trimming capacitors to cover the frequency range (~3%) of the ROSC array. During stress

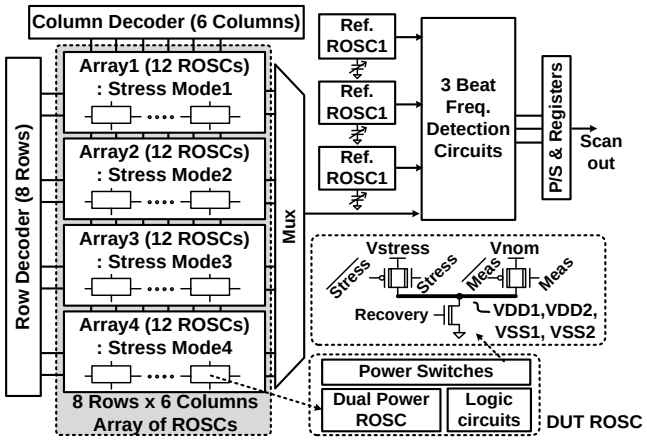


Fig. 5. 6x8 ROSC array, three reference ROSCs, power switches, and BFD circuits

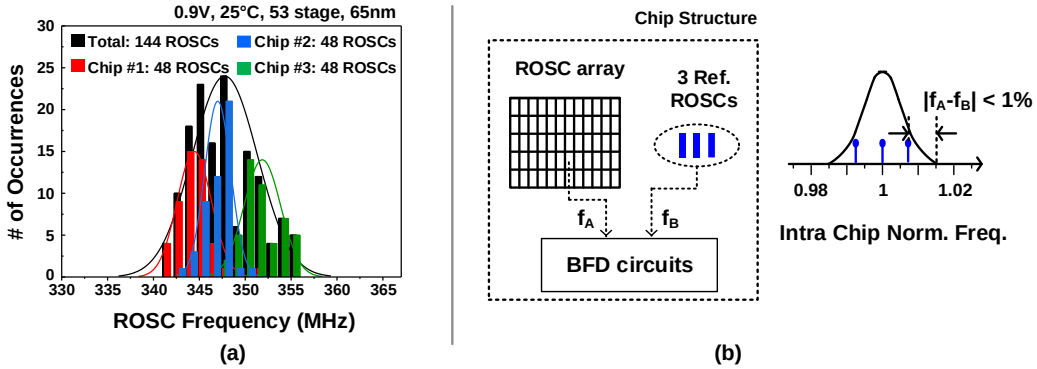


Fig. 6. (a) Fresh frequency distribution of three chips. (b) 3 reference ROSCs with frequency trimming to cover frequency range.

mode, one ROSC is selected at a time for frequency measurements using column and row decoders while the other ROSCs are kept in stress mode. The output of the selected DUT is multiplexed out and compared with the three reference ROSC frequencies using the BFD circuits. Of the three beat frequency counts, we chose the one providing a high accuracy for data analysis. The frequency difference between the stressed ROSC and reference ROSC was kept within ~2% to maintain a high measurement precision throughout the entire stress period (Fig. 6).

III. TEST CHIP STRESS RESULTS

The 65nm ROSC array chip was tested under different DC stress conditions. All testing results are based on a 4μs stress interruption time which is short enough to prevent unwanted BTI aging [9]. Fig. 7 shows the frequency distribution before and after 3 hours of 2.2V DC stress at 25°C. The DUT frequencies were characterized at 0.9V. Each distribution was obtained from 36 ROSCs measured from 3 test chips. To extract the individual BTI components, we took the difference between the frequency shifts measured under different stress modes. For instance, PMOS PBTI induced frequency shift was obtained by subtracting the frequency shift of stress mode 1 from that of stress mode 2. The average frequency shifts at the end of the stress period (i.e. after 3 hours of 2.2V DC stress at 25°C) were higher for stress mode 2 ($\Delta f = 2.88\%$) and stress mode 4 ($\Delta f = 2.87\%$) as compared to that of stress mode 1 ($\Delta f = 2.01\%$), due to the additional PMOS PBTI effect. On the other hand, the frequency shift for stress mode 3 ($\Delta f = 1.72\%$) was less than that for stress mode 1 ($\Delta f = 2.01\%$) by a small margin, indicating that NMOS NBTI is negligible compared to PMOS PBTI. The additional frequency shifts compared to the baseline 'PMOS NBTI + NMOS PBTI' induced shift at the end of the stress period are: (i) 0.87% for PMOS PBTI; (ii) -0.29% for NMOS NBTI; and (iii) 0.86% for 'PMOS PBTI + NMOS NBTI'.

Fig. 8 shows frequency shift data for a 2.2V DC stress measured at 25°C. Both 'PMOS NBTI+NMOS PBTI' and 'PMOS PBTI' show a similar increase in average frequency shift, indicating an increase in Vth, while NMOS NBTI exhibits the opposite trend, albeit with a much smaller magnitude. As shown in Fig. 8 (right), PMOS PBTI shows a higher time slope than PMOS NBTI. Also, PMOS N/PBTI induced shifts show a power law time dependence. However, the shift caused by NMOS NBTI does not follow the power law and instead shows two different trends. Short-term stress results in an increased frequency shift (i.e. degradation), as in

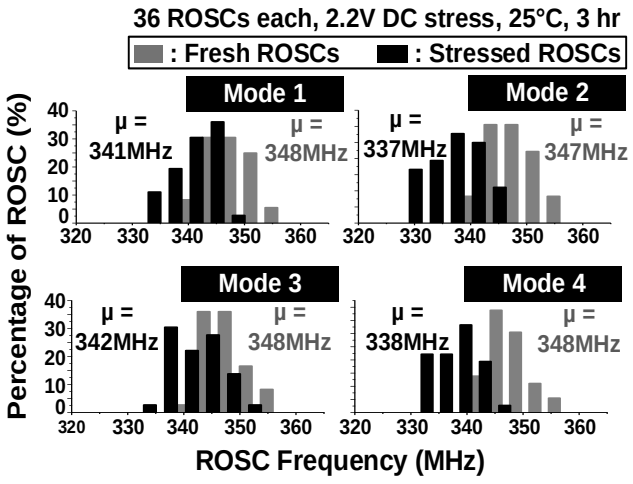


Fig. 7. Frequency distributions after 3 hours of stress (black bars), along with the fresh distributions (gray bars). Each histogram was generated from 36 ROSC.

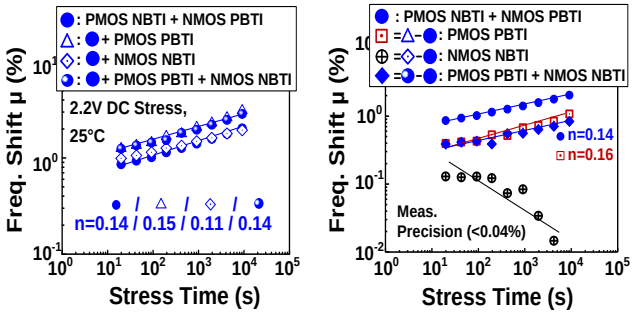


Fig. 8. 2.2V, 25°C DC stress data. Data in the right figure is obtained by subtracting the PMOS NBTI and NMOS PBTI components from the combined stress results

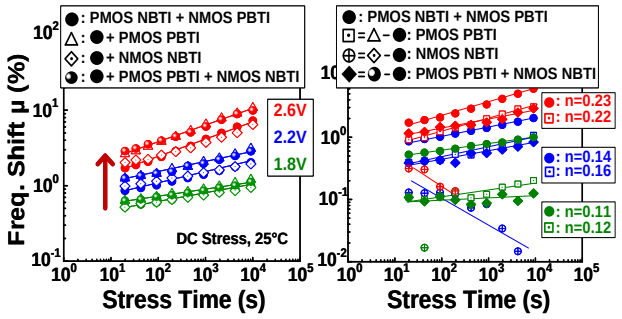


Fig. 9. Frequency shift for different BTI modes under different supply voltage.

PMOS NBTI/PBTI stress modes, while long-term stress results in a decrease in the frequency shift (i.e. recovery). These observations are consistent with the results reported in [6] [7]. Furthermore, Fig. 8 (right) shows the relative magnitude of frequency shifts for the different BTI modes. NMOS PBTI is assumed to be negligible compared to PMOS NBTI since the 65nm technology used in this work does not employ high-k dielectrics [8-10]. In the early stage of stress, PMOS NBTI effect is most pronounced (~7x higher compared to NMOS NBTI effect), followed by PMOS PBTI effect (~3x higher), and then NMOS NBTI effect. Note that the degradation caused by PMOS PBTI effect is known to increase when a positive bias is applied between the gate and body node [6].

Frequency shift measurements for different stress voltages (2.6V, 2.2V, and 1.8V) at 25°C are shown in Fig. 9, indicating a larger frequency shift at a higher stress voltage for all 4 stress modes. As shown in Fig. 9 (right), the time slope of the PMOS PBTI is higher than that of the PMOS NBTI at 1.8V and 2.2V. However, the trend does not hold at 2.6V.

Frequency shifts measured at 25°C and 100°C under a 2.2V stress are shown in Fig. 10. All 4 BTI components have a positive correlation with temperature while the power law exponent increases at higher temperatures. The time slope trend (i.e. PMOS PBTI's > PMOS NBTI's) is also observed under 100°C as shown in Fig. 10 (right).

Fig. 11 shows the die photo and chip summary of the 65nm test chip.

IV. Conclusion

In this work, we proposed an odometer circuit for characterizing frequency degradation caused by different BTI stress modes. Using independent dual power rails and the proven-and-tested beat frequency detection technique, we were able to separate the frequency degradations under different BTI stress conditions with sufficient resolution. Statistical reliability data from the proposed ROSC array fabricated in a 65nm process is presented under different stress voltage and temperature conditions.

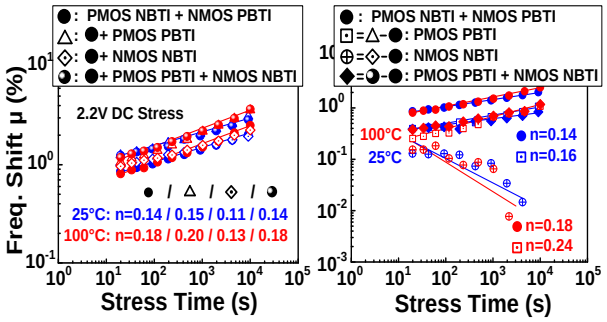
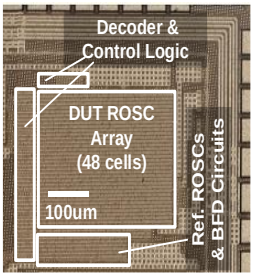


Fig. 10. Frequency shifts under different temperatures.



Process	65nm GP
BTI Stress Modes	PMOS NBTI, NMOS PBTI, PMOS PBTI, NMOS NBTI
Core/IO Supply	1.0V / 2.5V
Stress Voltage	1.8V, 2.2V, 2.6V
Meas. Voltage	0.9V
DUT Device	Core Deivce
Area	425 x 360 μm^2

Fig. 11. Die photo and chip specification summary.

Acknowledgment

This work was supported in part by Semiconductor Research Corporation Task No. 2712.017 through the Texas Analog Center of Excellence (TxACE). The authors would also like to thank Drs. Vijay Reddy and Srikanth Krishnan at Texas Instruments for introducing PMOS PBTI issues to us and for the technical feedback and encouragement throughout the project.

References

[1] G. Hall, T. Myers, L. Ou, J. Slezak, A. Litschmann, D. Price, T. Clear, J. Gambino, "PBTI and PBTS testing of 0.25 μm pMOSFET devices for analog circuits", *IEEE International Reliability Physics Symposium (IRPS), April 2017.*

[2] R. Fernandez, B. Kaczer, A. Nackaerts, S. Demuynck, R. Rodriguez, M. Nafria, G. Groeseneken, "AC NBTI studied in the 1 Hz -- 2 GHz range on dedicated on-chip CMOS circuits", *IEEE International Electron Device Letters (IEDM)*, December 2006.

[3] J.-J Kim, R. M. Rao, J. Schaub, A. Ghosh, A. Bansal, K. Zhao, B. P. Linder, J. Stathis, "PBTI/NBTI monitoring ring oscillator circuits with on-chip Vt characterization and high frequency AC stress capability", *IEEE Symposium on VLSI Circuits*, June 2011.

[4] P. Jain, A. Paul, X. Wang, C.H. Kim, "A 32nm SRAM Reliability Macro for Recovery Free Evaluation of NBTI and PBTI ", *International Electron Devices Meeting (IEDM)*, Dec. 2012

[5] M. Seok, P. R. Kinget, T. Yang, J. Li, D. Kim, "Recent Advances in In-situ and In-field Transistor-Aging and Compentation Techniques*," IEEE International Reliability Physics Symposium (IRPS)*, March 2018.

[6] H. Park, P. E. Nicollian, and V. Reddy, "Positive bias temperature instability induced positive charge generation in P+ Poly/SiON pMOSFET's", *IEEE International Reliability Physics Symposium (IRPS)*, April 2012.

[7] A. Benabdelmoumene, B. Djezzar, A. Chenouf, B. Zatout, and M. Kechouane, "Analysis of NBTI Degradation in nMOS-Capacitors and

nMOSFETs", *IEEE Transactions on Device and Materials Reliability (TDMR)*, vol. 18, no. 4, December 2018.

[8] T. Kim, R. Persaud, and C. H. Kim, "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 43, pp. 874-880, April 2008.

[9] J. Keane, W. Zhang, and C.H. Kim, "An Array-Based Odometer System for Statistically Significant Circuit Aging Characterization", *IEEE Journal of Solid-State Circuits(JSSC)*, pp.2374-2385, October 2011.

[10] J. Keane, W. Zhang, C.H. Kim, "An Array-Based Odometer System for Statistically Significant Circuit Aging Characterization ", *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 46, issue 10, 2011

[11] G. Park, B. Kim, M. Kim, V. Reddy, and C. H. Kim, "All-Digital PLL Frequency and Phase Noise Degradation Measurements Using Simple On-Chip Monitoring Circuits", *International Reliability Physics Symposium (IRPS)*, Mar. 2018.