Coupled Oscillator base Computing: Using Nature to Solve Difficult Problems

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Outline

- Introduction to Ising Computers
- Case Study: 560 Coupled Oscillator Test Chip
- Summary

Ising Spin Glass Model









 A promising approach for efficiently solving NP-hard or NP-complete problems (e.g. combinatorial optimization problems, Boltzman machines, associative memories, Karp's 21 NPcomplete problems)
$$\begin{split} H(s) &= -\sum_{\langle i,j \rangle} J_{ij} s_i s_j - \sum_i h_i s_i &: \text{Ising Hamitonian (Cost Function)} \\ s_i, s_j : \text{Spin state } \{+1 \text{ or } -1\} & J_{ij} : \text{Coupling strength} \quad h_i : \text{local field strength} \end{split}$$



Using Nature to Find the Ground State





Random states (time=0)



Same states (time = 1 min)

Youtube: Coupled Metronomes

Example Problem #1: Factorizing 15

p =
$$(x_1 \ 1)_2$$
, q = $(x_2 \ x_3 \ 1)_2$
H = $(15 - pq)^2$

$$H = 128x_1x_2x_3 - 56x_1x_2 - 48x_1x_3 + 16x_2x_3 - 52x_1 - 52x_2 - 96x_3 + 196$$

$$H_{mod} = 200x_1x_2 - 48x_1x_3 - 512x_1x_4 + 16x_2x_3 - 512x_2x_4 + 128x_3x_4 - 52x_1 - 52x_2 - 96x_3 + 768x_4 + 196$$

S. Jiang, et al., "Quantum Annealing for Prime Factorization", Scientific Reports 2018

Example Problem #2: Graph Coloring

For graph G(V, E) of the map problem—no two vertices, V, connected by an edge, E, should select the same color from set C—construct a cost function with binary variables, $x_{v,c} = 1$ when $v \in V$ selects color $c \in C$, by implementing two constraints:

$$(\sum_{c} x_{v,c} - 1)^2,$$

which has minimum energy (zero) when vertices select one color only, and

$$\sum_{c} \sum_{v_a, v_b \in E} x_{v_a, c} x_{v_b, c},$$

which adds a penalty if the vertices of an edge select the same color. These constraints give a QUBO,

$$E(x_{v}, x_{v_{a}, v_{b}}) = \sum_{v} (\sum_{c} x_{v, c} - 1)^{2} + \sum_{c} \sum_{v_{a}, v_{b} \in E} x_{v_{a}, c} x_{v_{b}, c}$$

D-Wave Problem-Solving Handbook, 8/13/20

e.g. $x_{Minn,Red} = 0, x_{Minn,Blue} = 0,$ $x_{Minn,Sand} = 1, x_{Minn,Green} = 0$ $x_{Wisc,Red} = 0, x_{Wisc,Blue} = 1,$ $x_{Wisc,Sand} = 0, x_{Wisc,Green} = 0$



Example Problem #3: Finding Max-cut



- The problem of finding a maximum cut in a graph is known as the Max-Cut Problem
- Finding max-cut of a graph is an *NP-hard* problem



Example Problem #3: Finding Max-cut





 σ_i = Spin status of magnet i {+1 or -1} w_{ij} = weight between magnets i and j

• Ising Hamiltonian = [sum of all weights] – 2×[cut size]

Other NP Problems Mappable to the Ising Model

- Partitioning problems (e.g. max cut)
- Binary integer linear programming
- Covering and packing problems
- Problems with inequalities
- Coloring problems (e.g. graph coloring)
- Hamiltonian cycles (e.g. traveling salesman)
- Tree problems
- Graph isomorphisms
- •

A. Lucas, "Ising formulations of many NP problems", Frontiers in Physics, Feb. 2014

Using Coupled Oscillators to Find the Ground State





 $H(s) = -J_{ij}s_is_j$ if $J_{ij} > 0$, then $\{s_i, s_j\} = \{+1, +1\}$ or $\{-1, -1\}$: Same phase if $J_{ij} < 0$, then $\{s_i, s_j\} = \{+1, -1\}$ or $\{-1, +1\}$: Opposite phase

Using Coupled Oscillators to Find the Ground State



Other Oscillator Devices



Superconducting qubits



Phase transition material



Magnetic tunnel junctions



CMOS



Cavity parametric oscillator



MEMS/NEMS



Ferroelectric

Sources: Google image, IEDM 20, EDL2017, Science 2016

Comparison of Coupled Oscillator Technologies

	Qubit	Optical	Phase transition	Spintronic	CMOS
Conceptual figure		Putter Later Putte	VDD VO2 Oscillator output Injection VGS	Nonconstitution of the second	Phase comparator ROSC1 ROSC1 EN1
# of oscillators	~2000	100-2000	4	8	2000+
	(single chip)	(lab setup)	(probe station)	(board level)	(1.3mm ² chip in 65nm)
Advantages	Under debate	Room temperature	Room temperature	Room temperature	Room temperature, leverages CMOS, cloud/edge computing
Disadvantages	Cryogenic cool, 25kW power, premature tech. cloud only	1km optical fiber, FPGA chip, complex setup	Premature device, no real area advantage over CMOS	Premature device, no real area advantage over CMOS	Will it outperform GPUs and software solvers?
Integrated system in 10 yrs?	No	No	No	No	Yes
Target	NP-hard and NP-complete combinatorial optimization problems (e.g. supply chain, AI/ML, transportation,				
applications	smart grid, communication, IC design, bioinformatics, computer vision, and robotics)				

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ROSC Coupled Using Digital Latches



- Any coupling medium that enables energy transfer may couple ROSCs
- ROSC and digital latches are designed with global and local enable signals

Choice of Architecture



- Hexagonal unit cell maximizes the number of neighbors in 2D plane
- Latch based coupling between cells is digitally controlled

Die Photo and Chip Summary



- 28x20=560 coupled oscillators (only limiting factor is chip area)
- Oscillator area < 5% of the full chip area

Embedding Ising Problem to Hardware



Max-cut Results for 15x15 Graphs



- 150 difficult COPs are mapped and max-cut results are measured for each graph sizes
- Measured results are compared with 1 million randomly sampled solutions from the solution-space for each specific graph.

Max-Cut Results for Different Graph Sizes



Repeated Experiment for Same Graph



Temperature versus Solution Quality



Takeaways

- NP-hard problems could be the key driver for future computing growth
- A true coupling based integrated CMOS Ising chip was demonstrated in 65nm
 - No emerging devices needed (old saying: anything that can be done in CMOS, will be done in CMOS)
 - Probabilistic exploration of various local minima
 - Mapped and solved 1,000 COPs in the chip with an accuracy of 82%-100%
- For oscillator based computing to be a viable approach however, there has to be a clear and significant power-performance-area advantage over
 - Mathematical optimizers (available today)
 - GPU, FPGA, Custom ASICs, digital annealers (available today)
 - Quantum computers