Extreme Temperature Characterization of Amplifier Response up to 300°C Using Integrated Heaters and On-chip Samplers

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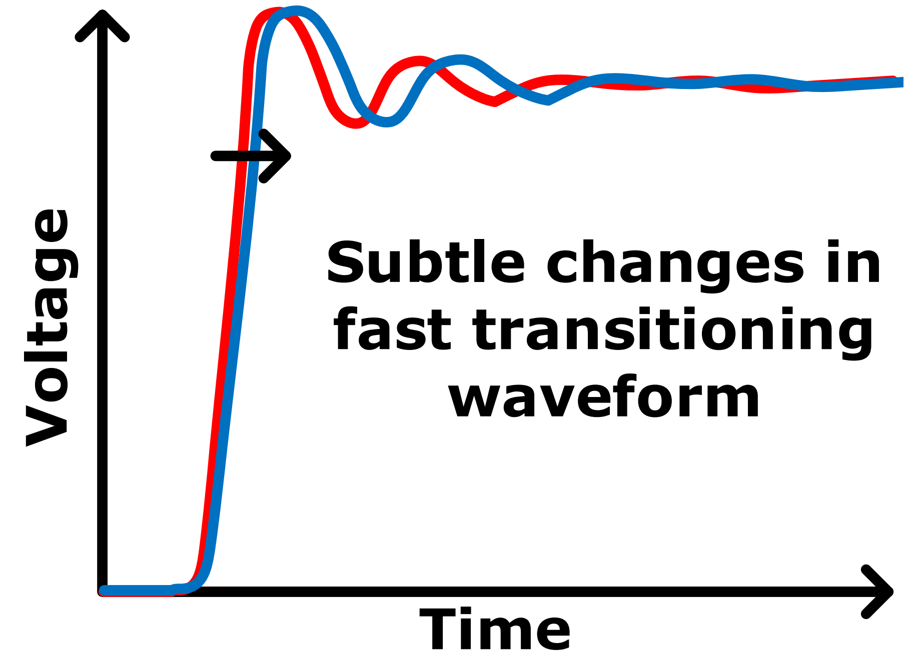
***Equal contribution, ^Now with Intel Corporation, OR, USA**

Outline

- **Introduction**
- **Proposed on-chip analog response monitor**
- **65nm test chip results**
- **Conclusion**

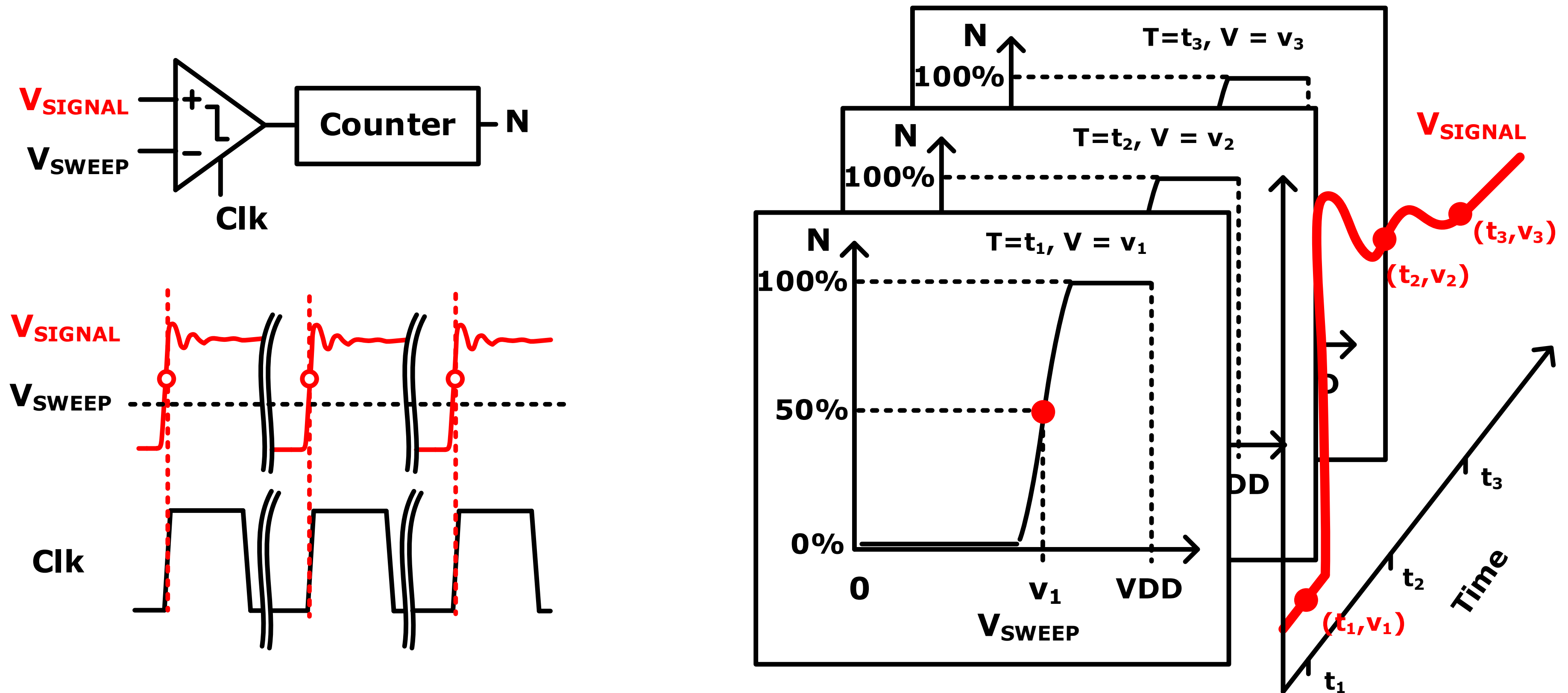
*From Google → NEED TO BE MORE SPECIFIC, PLEASE IDENTIFY ACTUAL PHOTO SOURCE, ALSO SHOULD WE SHOW AN EV RATHER THAN AN ICE CAR?

Motivation



- Special applications require analog circuits to work reliably under extreme temperatures.
- Subtle performance shifts in fast transient response are hard to measure using off-chip testing methods.

Sub-sampling a Repetitive Signal



- ☐ Clock rising edge determines sampling position.
- ☐ Post-processing required to re-create the response.

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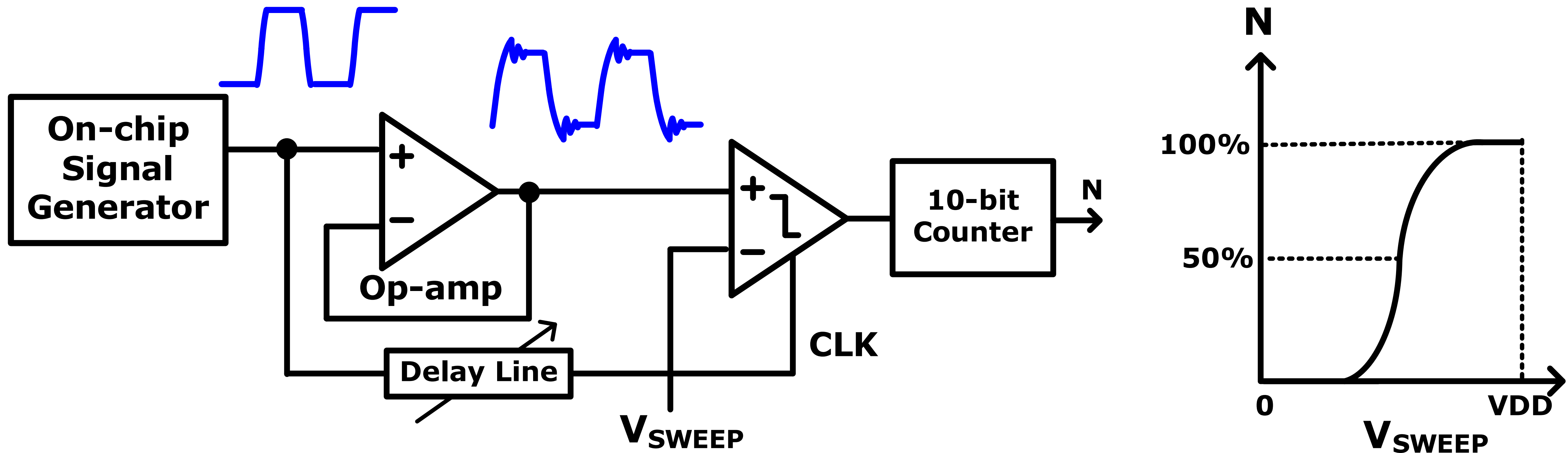
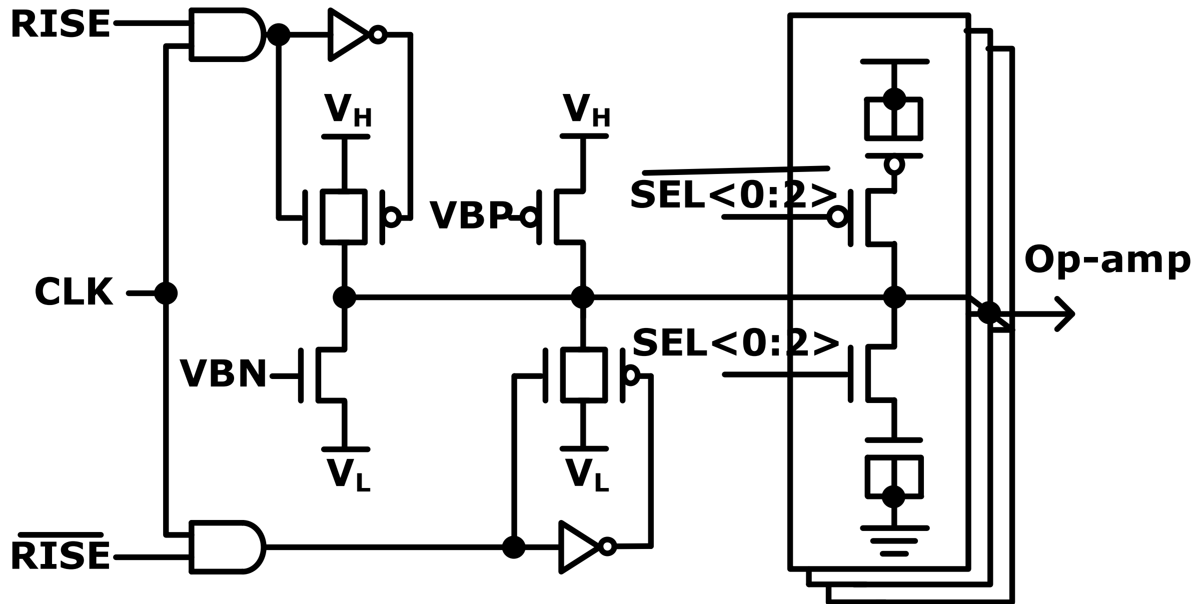
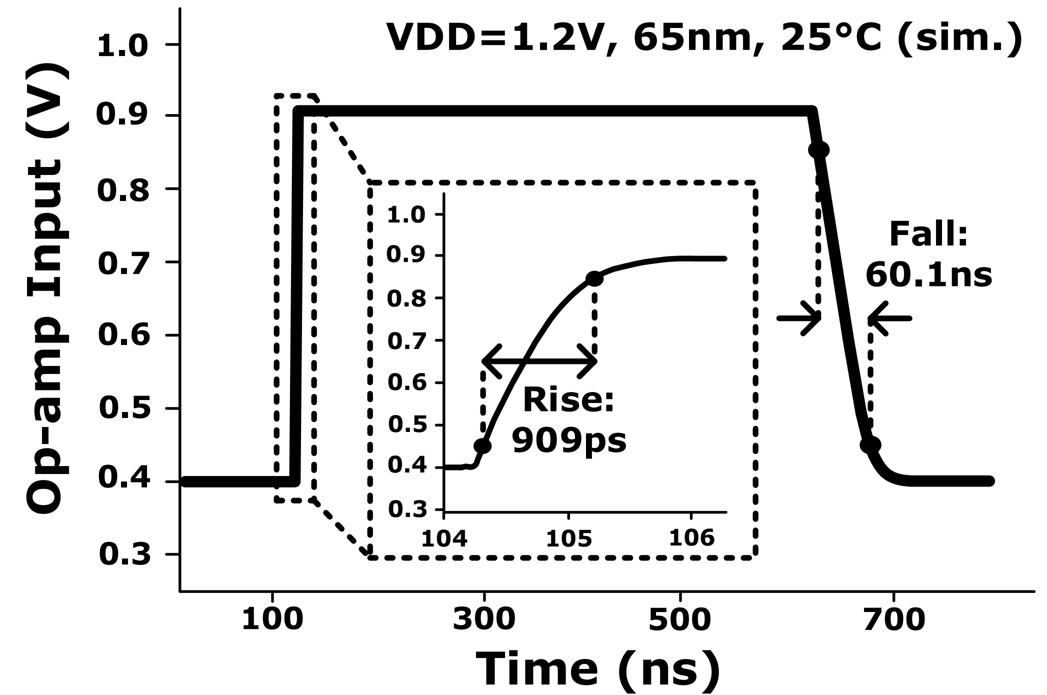
Input Step Response Sampling Concept



- Signal generated on-chip and fed into unity gain buffer.
- 10 bit count versus V_{sweep} curve obtained for average voltage level extraction

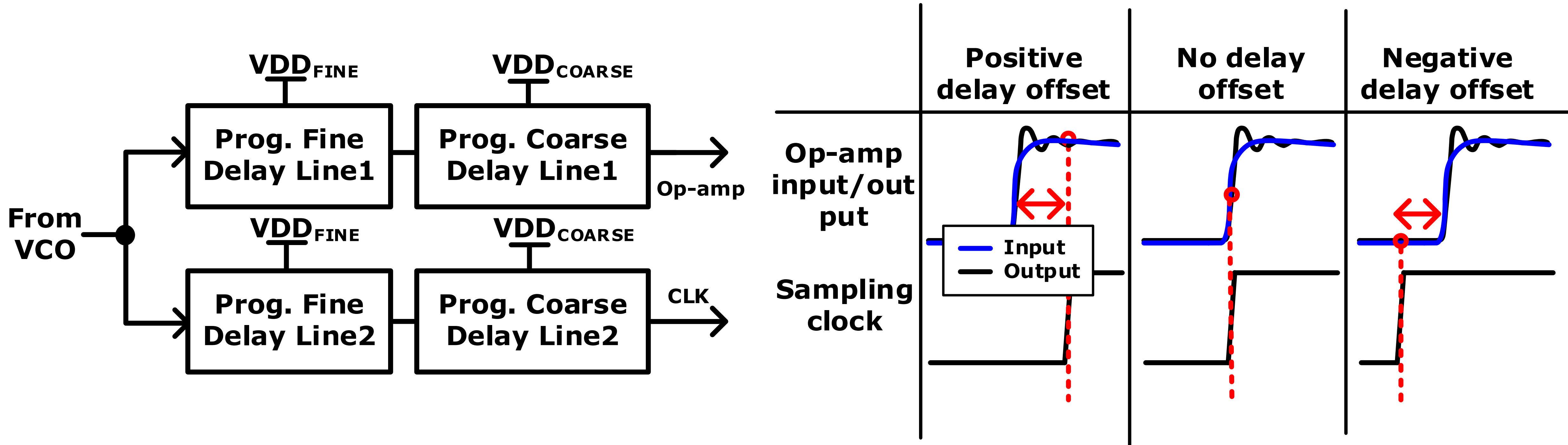
On-Chip Step Input Generation Circuit





- Strong switch + weak bias current combination eliminates glitches while switching.
- Programmable load capacitance to vary slew rate.

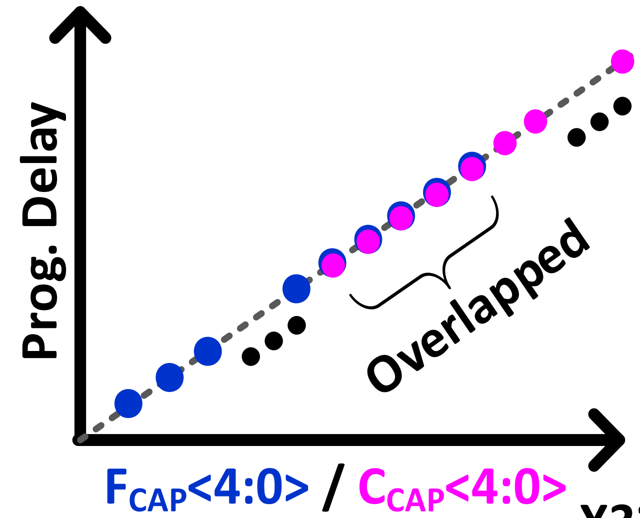
Programmable Delay Lines



- Two identical programmable delay lines generate delay difference between sampling clock and op-amp input.
- Programmable delay allows us to measure entire waveform.

Programmable Delay Lines

VDDFINE
VDDCOARSE
Prog. Fine Delay Line1
Prog. Coarse Delay Line1
Op-ampIN
From VCO
Prog. Fine Delay Line2
Prog. Coarse Delay Line2
CLK

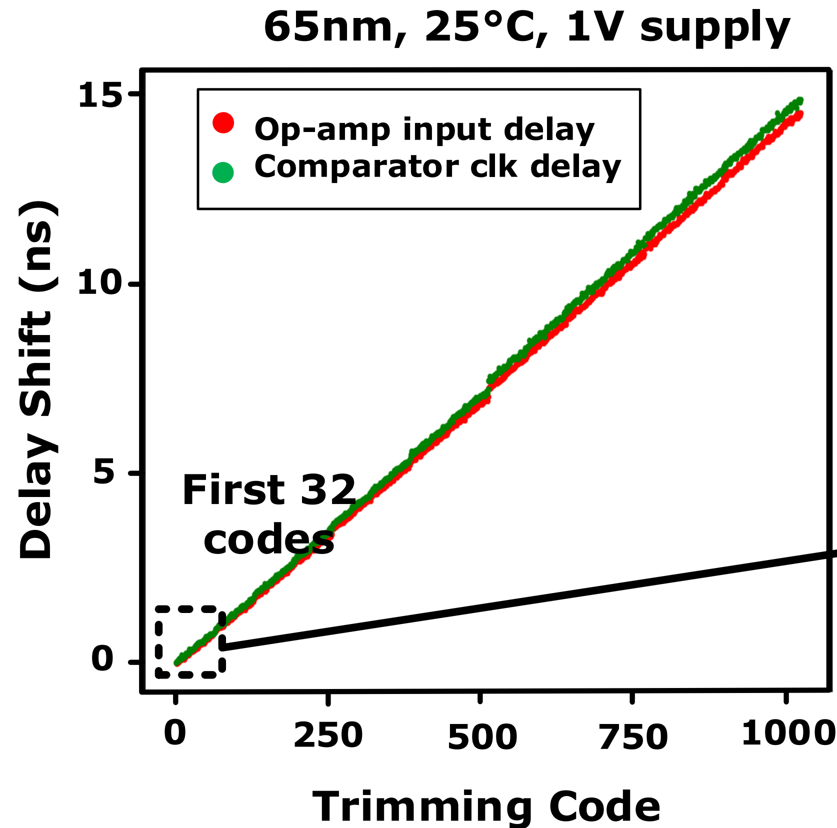


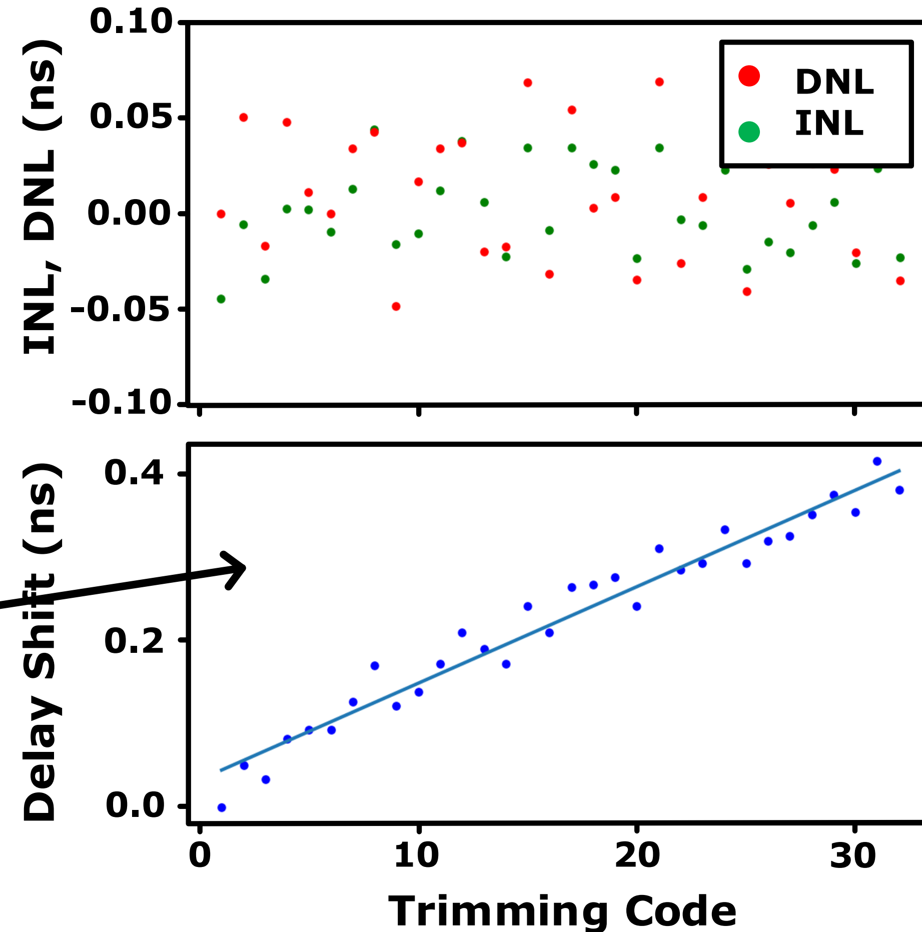
VDDFINE
1 Stage
FCAP<4:0>
VDDCOARSE
28 Stages
CCAP<4:0>
X32

- Overlapping delay range ensures we can visit the entire time space with no gaps.

Upper right figure is not very clear. I tried to update but still doesn’t look very accurate. Please revise.

Delay Line Control Resolution

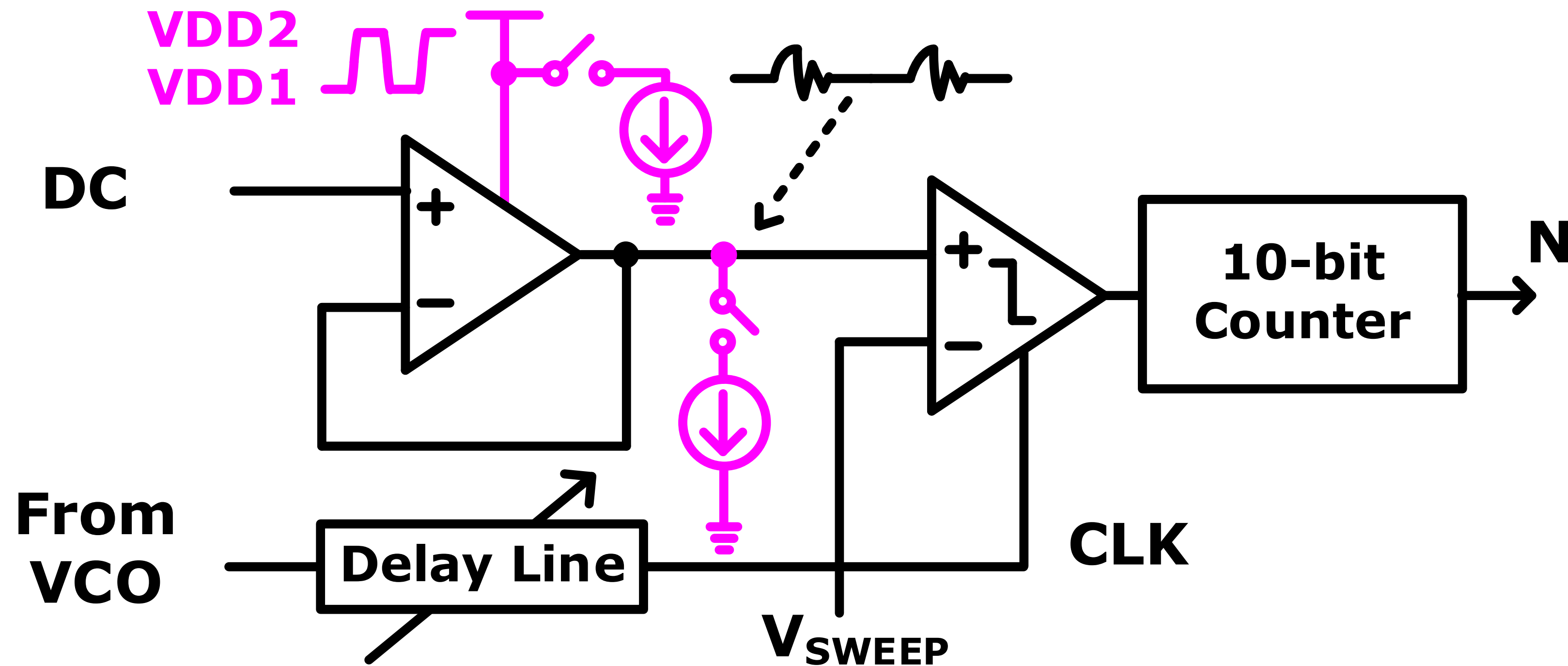




- 50ps delay programming resolution

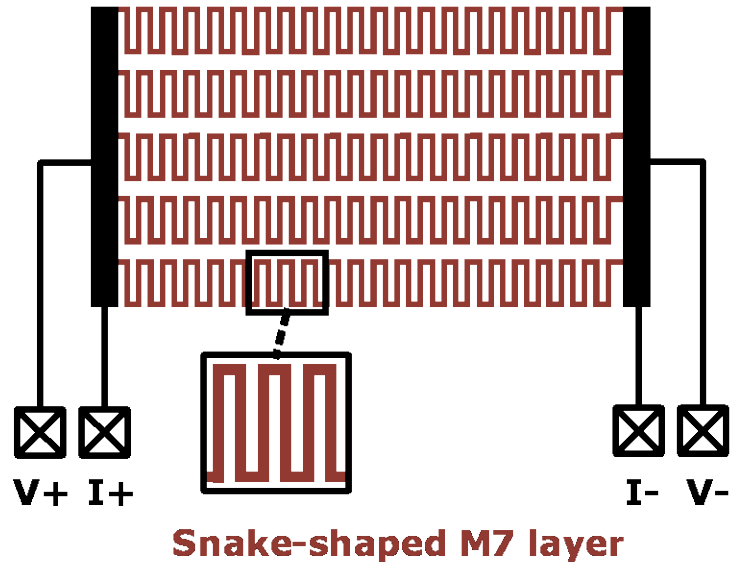
Should we report INL and DNL instead of the 50ps delay number?

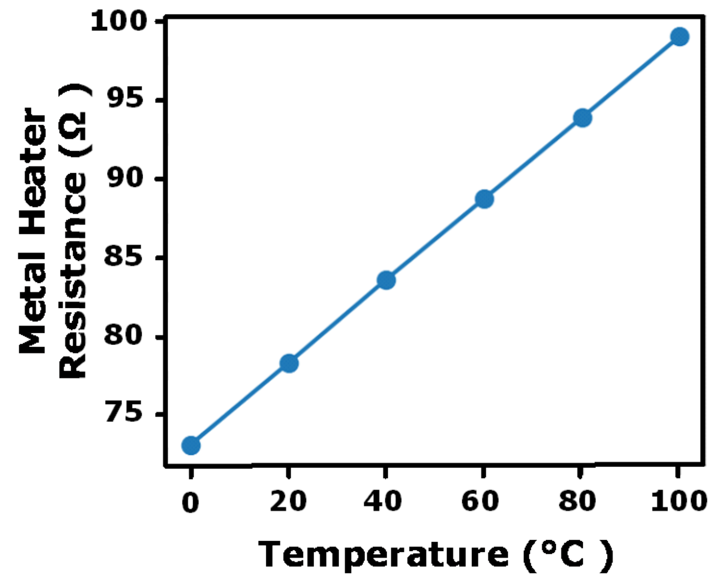
Power and Load Step Response Measurements

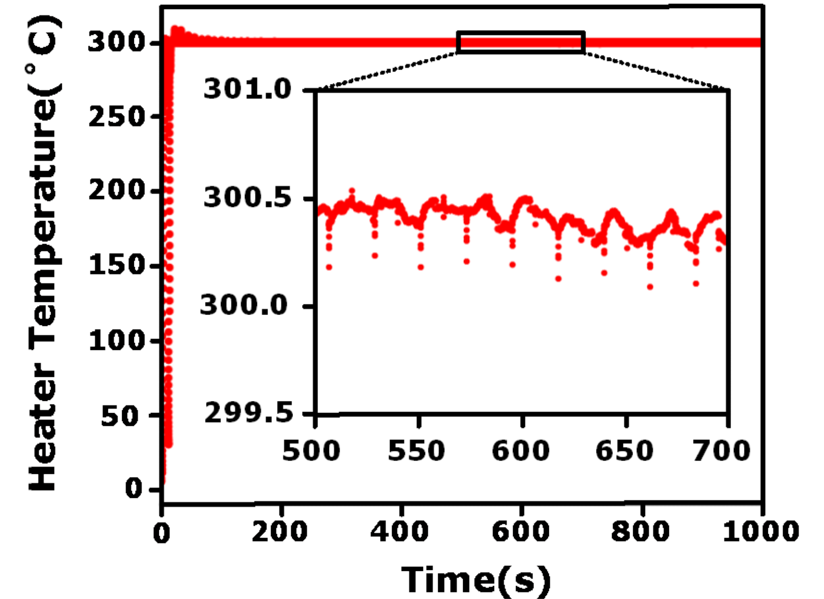


- Toggle load current
  - between VDD and ground → Power Transition
  - between Op-amp output and ground → Load Transition

M7 Metal Heater for High Temperature Testing







- Snake shaped metal wire.
- Stable temperature control for over 100hrs of test time.

Metal layer	M7
Resistance @ 0°C	73.1Ω
Heater area	10,241μm^2
Target Power Density	6.5x10^{-5}W/μm^2
T_{MAX} / Test Time	350°C / 100hrs

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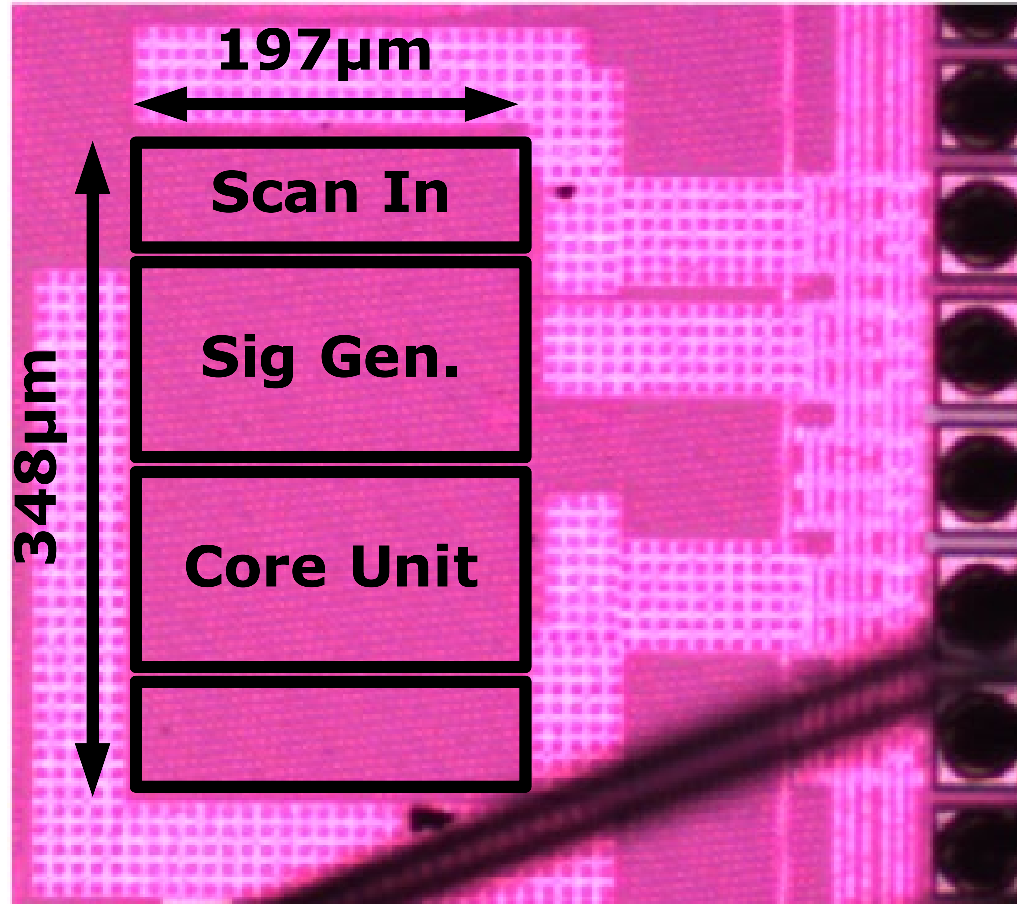
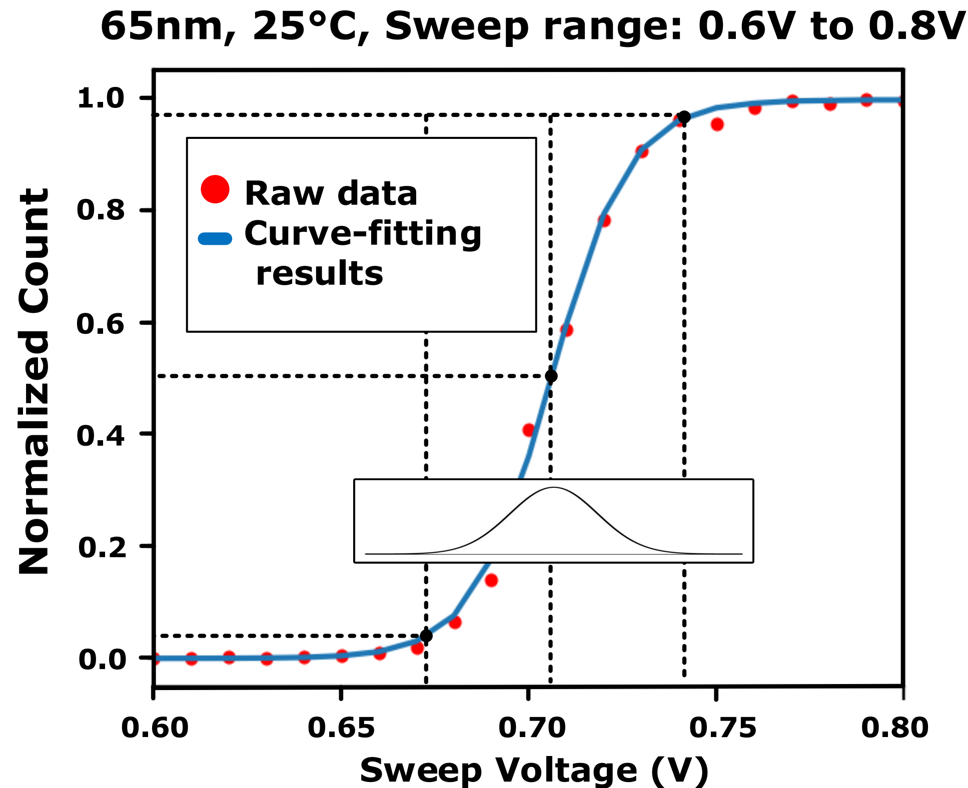
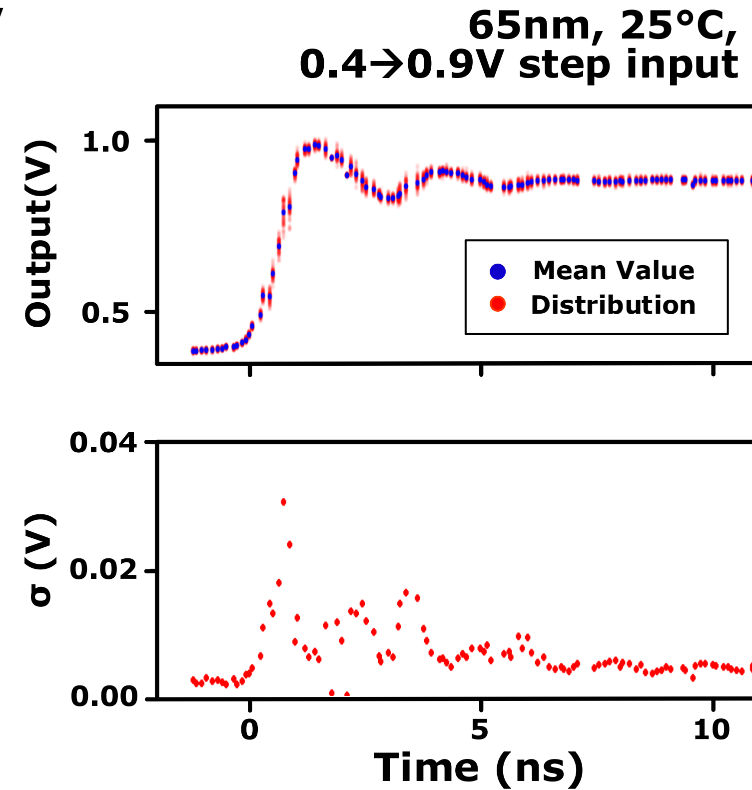
65nm Test Chip Die Photo and Summary



Technology	65nm LP CMOS
Core Size	348 X 197 μm^2
VDD (Core/IO)	1.2V/2.5V
# of Unit Cells (Op-amp + Monitor)	8
# of Signal Generation Blocks	1

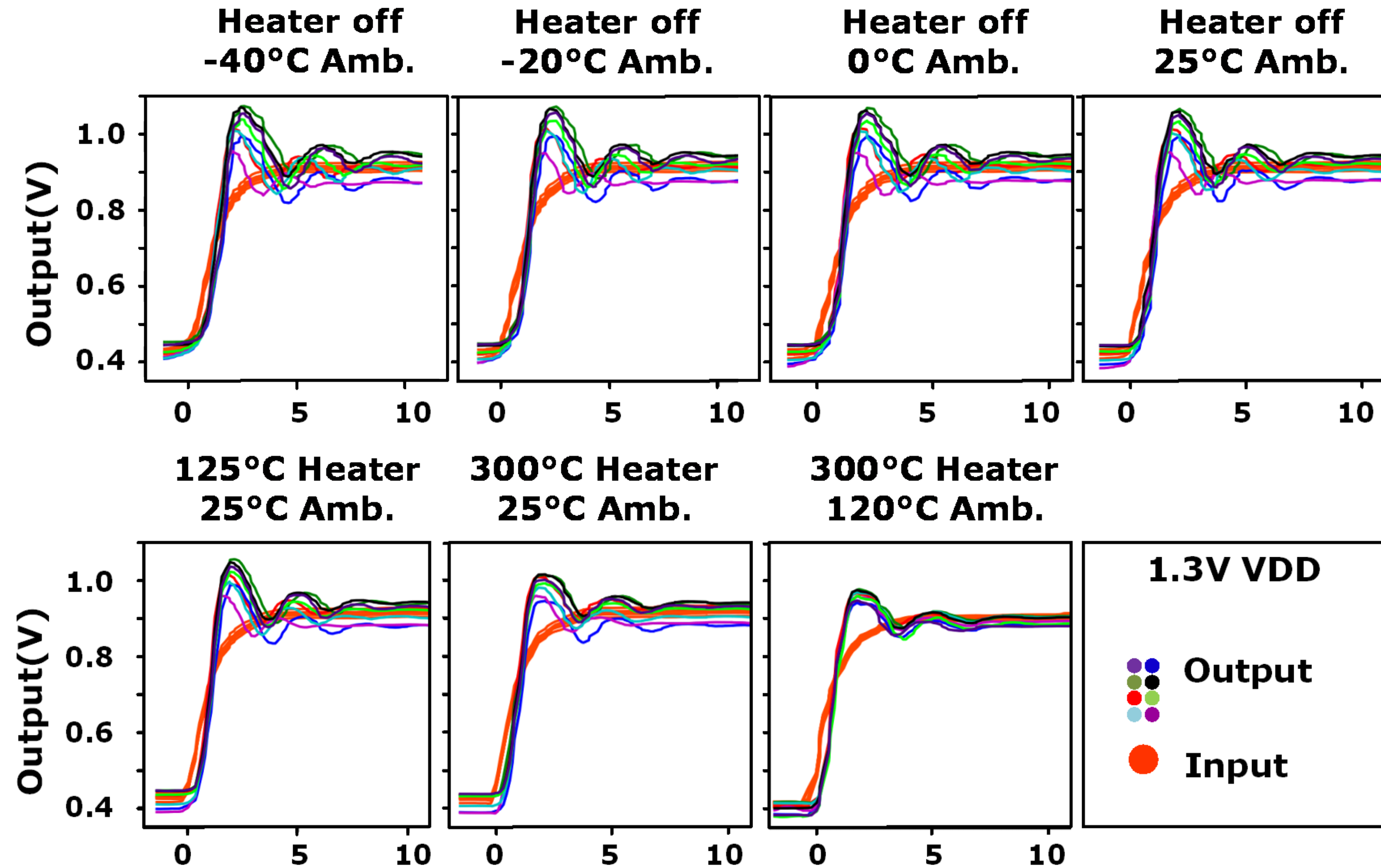
Waveform Reconstruction from Voltage Sweeps





- 50% voltage value from different sweeps are stitched together to re-create the step response waveform.
- Voltage spread < 32mV

Measured Step Response Waveforms



- 8 op-amps from the same chip.
- Temperature chamber + on-chip metal heater used together for temperature control.

Measured Step Response Parameters

op-amp#

1 2 3 4 5 6 7 8

Overshoot/(V2-V1)

0.2
0.1
0

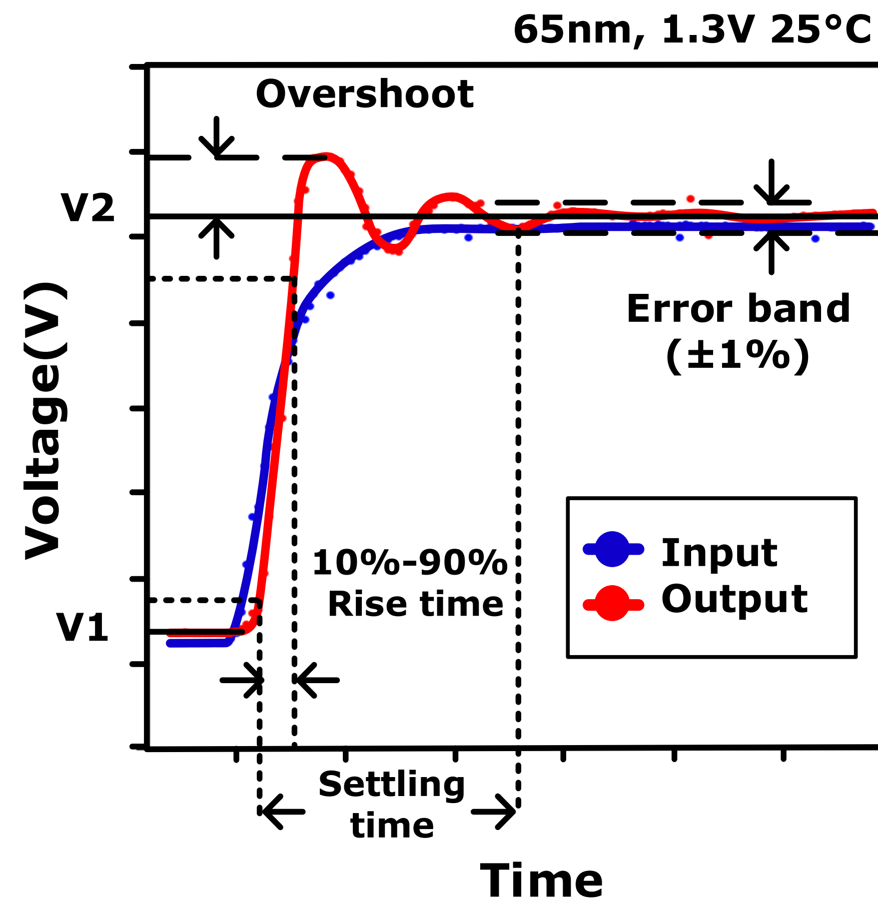
10% to 90% Slew Rate(V/ns)

0.6
0.4
0.2
0

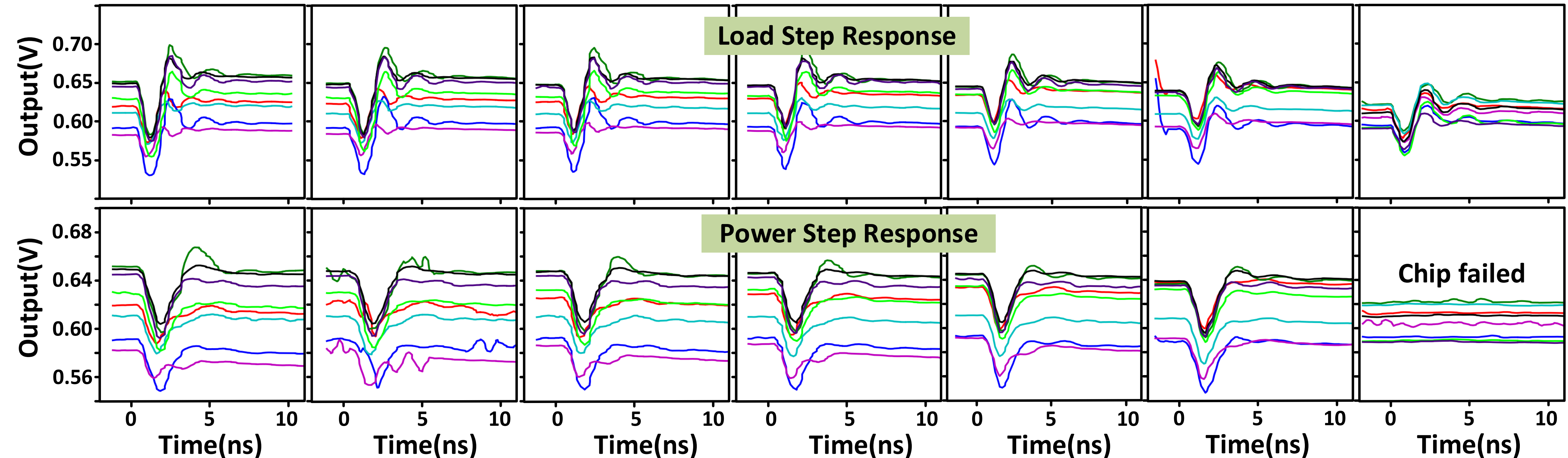
Settling Time(ns)

10
5
0

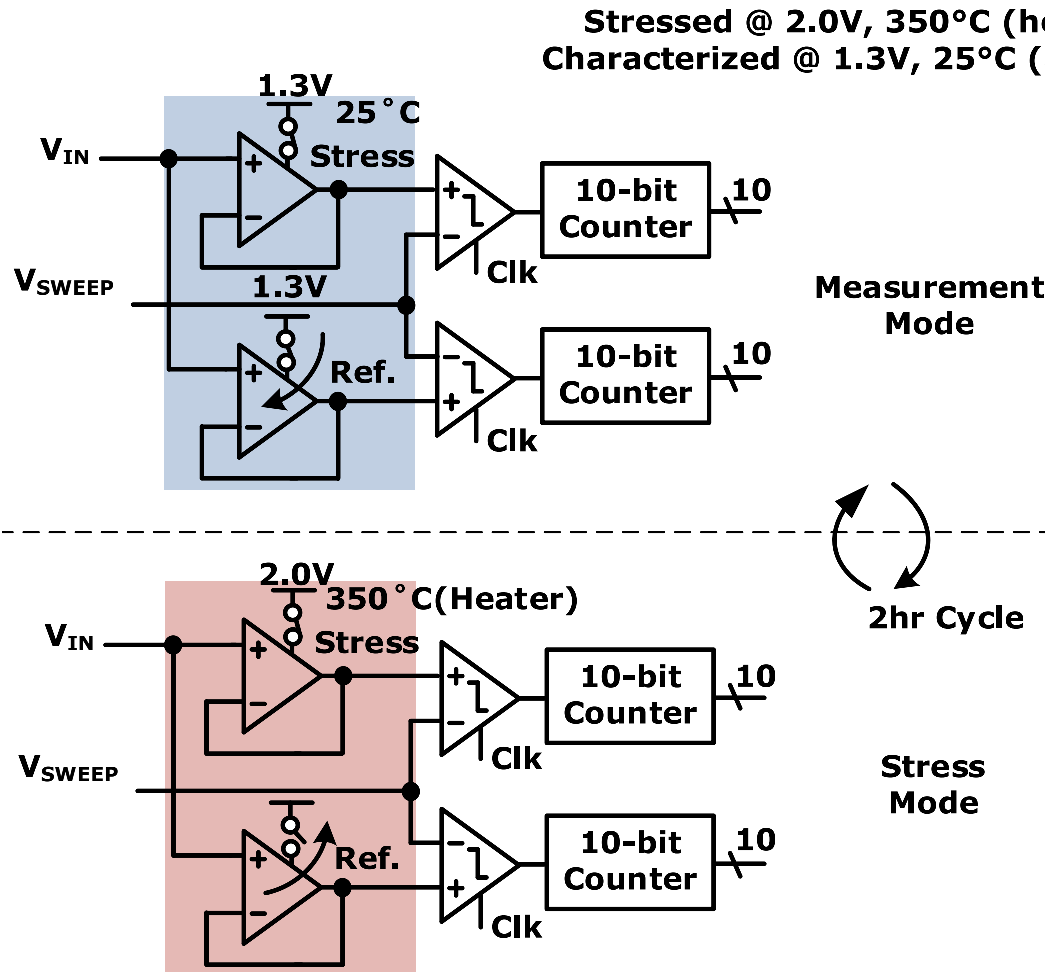
- Heater off, -40°C Amb.
- Heater off, -20°C Amb.
- Heater off, 0°C Amb.
- Heater off, 25°C Amb.
- 125°C(heater), 25°C Amb.
- 300°C(heater), 25°C Amb.
- 300°C(heater), 120°C Amb.

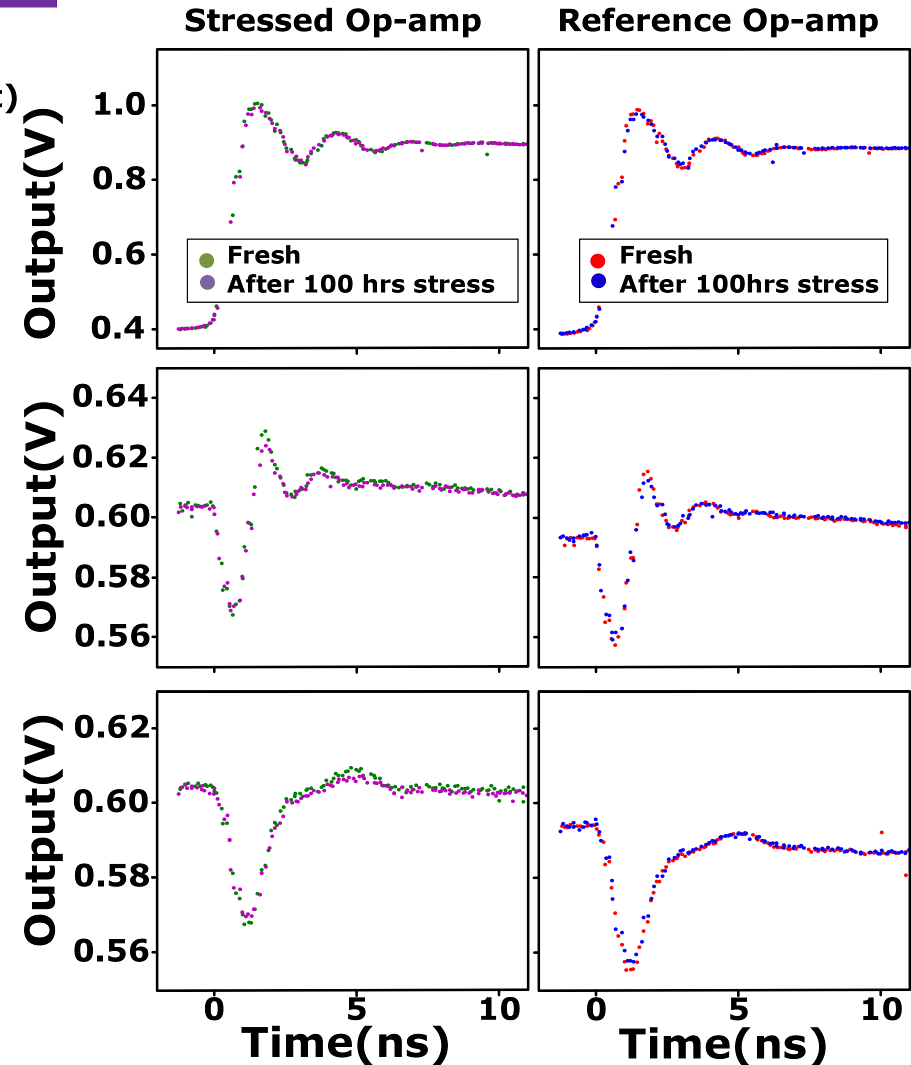


Power and Output Step Responses



High Temperature, High Voltage Stress Results





Comparison with Prior Art

	This Work	VLSI98 [1]	JSSC02 [2]	TVLSI03 [3]	JSSC07 [4]	VTS13 [5]
Technology	65nm	250nm	350nm	250nm	180nm	32nm
Voltage	1.2-1.3V	2.5V	3.3V	2.5V	1.8V	1.0V
Timing Resolution	50ps	7ps	180ps	10ps	14ps	50ps
Testing Temperature	300°C/120°C (Heater/Amb.)	-	-	-	-	< 85°C
On-Chip Clock Generation	Yes	No	Yes	No	No	No

[1] R. Ho et al., VLSI, 1998 [2] M.M. Hafed et al., JSSC, 2002 [3] Y. Zheng, K.L. Shepard, Trans. VLSI Syst. 2003 [4] M. Safi-Harb et al., JSSC, 2007 [5] K.A. Jenkins et al., VTS 2013

Conclusions

- **On-chip analog response monitor based on sub-sampling concept demonstrated in 65nm LP CMOS.**
- **Op-amp response recorded from -40°C up to 300°C (heater) with 50ps timing resolution.**

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