Extreme Temperature Characterization of Amplifier Response up to 300 Degrees Celsius Using Integrated Heaters and On-chip Samplers

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Abstract—An on-chip analog waveform sampling system was demonstrated in a 65nm process focusing on extreme temperature step response measurements. Amplifier output waveforms were measured under different temperatures ranging from -40 degrees Celsius to 300 degrees Celsius. For reliability testing, the amplifiers were stressed at a 1.6x supply voltage and a 350 degrees Celsius stress temperature for a total stress time of 100 hours.

Keywords—Analog waveform, sub-sampling, extreme temperature, reliability testing

I. INTRODUCTION

Testing analog circuits has become a major challenge in scaled technologies due to the higher operating speed, limited number of I/O pins, and signal integrity issues in the measurement setup [1][2][3][4]. Measuring aging induced parameter shifts in analog circuits is particularly challenging because of the small shift and the fact that accelerated stress data does not correlate well with real-world usage scenarios. Furthermore, analog circuits used in specialty applications such as automotive, aerospace, and oil/gas exploration must operate reliably at extreme temperatures in excess of 300°C necessitating significant characterization effort. In this work, we demonstrate a fully-integrated measurement system targeted for characterizing analog signal waveforms at extremely high temperatures up to 300°C. We employed the sub-sampling technique [5], where the signal level of a repetitive high-speed analog signal is detected by sweeping a known reference voltage until the signal level is reached. The voltage sweep measurement is repeated while incrementing the time offset between the triggering clock and the sampling clock to reconstruct the full waveform. In order to raise the local circuit temperature without damaging the package and test board, we integrated a metal heater with serpentine wires above the circuit under test [6][7].

II. PROPOSED ANALOG SIGNAL SAMPLER CIRCUIT

Fig. 1 shows the operating principle of the sub-sampling technique used in this work. For a repetitive analog signal, we obtain the sweep voltage versus occurrence curve at each sampling time. If sweep voltage is below the analog signal voltage, then the occurrence is low, and vice versa. The 50% point represents the sampled voltage. The occurrence curve is recorded while incrementing the sampling time offset until the time window of interest is measured. The occurrence curves
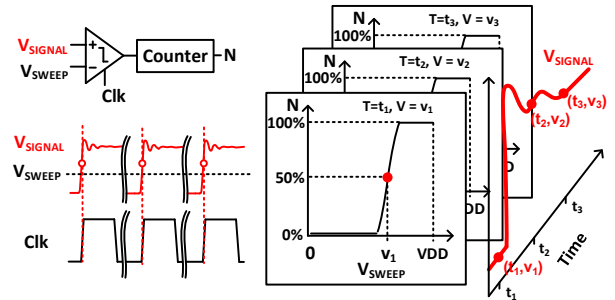
Fig. 1. On-chip sub-sampling of repetitive analog signals and waveform reconstruction method.
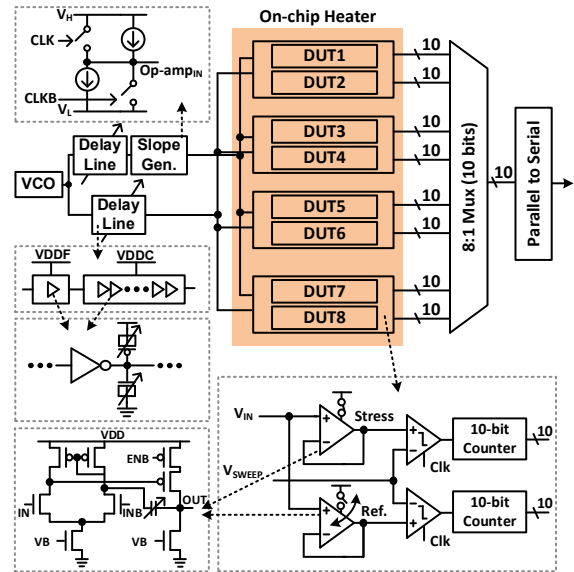

Fig. 2. Overall schematic of the proposed on-chip analog waveform monitor including sub-sampling circuits and an integrated heater.

are stitched together to recreate the analog waveform. Fig. 2 shows the diagram of the proposed on-chip response monitor, consisting of a signal generator, eight unity gain amplifiers, a readout circuit, and an integrated metal heater. The on-chip signal generation block is shared amongst all eight devices under test (DUTs). It consists of a VCO, two fine (5bit) + coarse (5bit) delay lines, and a step input generation circuit. The fine and coarse delay lines use dedicated power supplies of VDD$_{FINE}$ and VDD$_{COARSE}$, respectively, for additional delay control. Each DUT contains three components: the unity-gain voltage buffer under test, a comparator, and a 10-bit counter. The eight identical DUTs are divided into four pairs, with two physically adjacent DUTs forming a pair. One of the DUTs can be stressed (i.e. powered on) while the other DUT is kept fresh by turning off the power gate switches. The occurrence
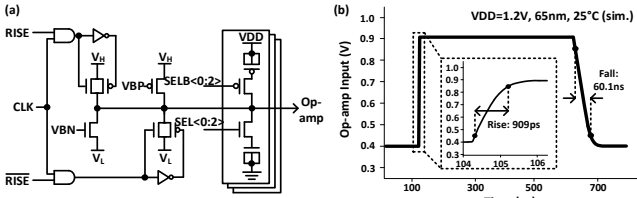
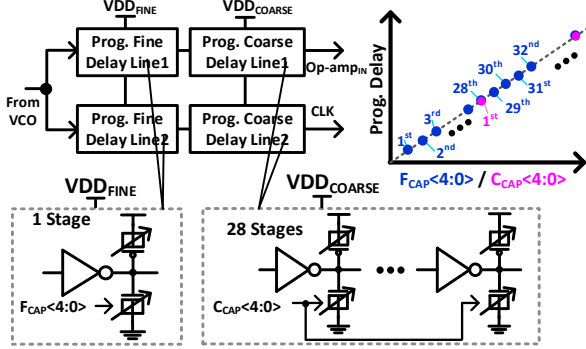Fig. 3. (a) Schematic and (b) simulation result of step input voltage generator.
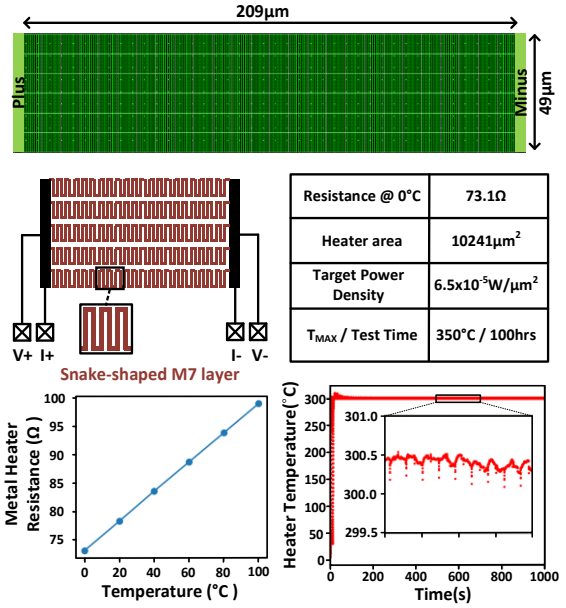

Fig. 4. Fine and coarse delay line operation.

Fig. 5. (Upper) Layout of the integrated heater. (Middle, left) Four terminals are used for accurate resistance measurements. (Middle, right) Heater design specifications. (Lower) Temperature coefficient of resistance (TCR) and temperature feedback control measurements.
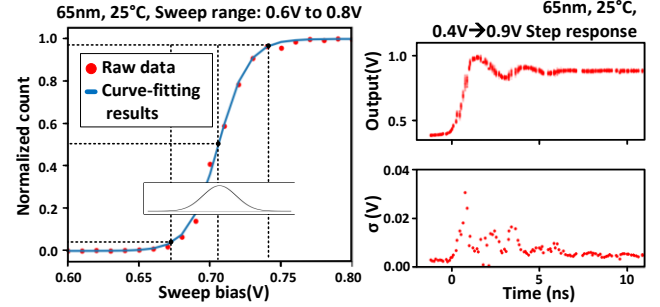

Fig. 6. (Left) Measured voltage sweep data. 2.5%, 50%, and 97.5% values are used for curve fitting and sampled voltage extraction. (Right) Raw data showing a measurement error of 30mV or less.

count is read out through a digital multiplexer and a parallel-to-serial register. Fig. 3(a) shows the detailed design of the step input generator. The VCO generates a shared clock signal, which is split into two paths with separate programmable delay lines. The first clock is applied to the unity gain amplifier, and the second clock is applied to the comparators. Fig. 3(b) shows the simulated waveform and the slew rate. The low and high voltages V_L and V_H are externally provided. We use a combination of a strong pull-up switch and a weak pull-down transistor to generate a fast positive edge and a slow negative edge. This design provides fewer glitches in the waveform compared to other switch designs we tried. Although this paper focuses on fast positive edge transitions, a strong pull-down + weak pull-up combination is also implemented and could be selected for the negative edge testing, controlled by the "RISE" signal in Fig. 3(a). A programmable load circuit was implemented to generate step inputs with different slew rates for testing purposes. As shown in Fig. 4, the fine delay line consists of one inverter stage, and the coarse delay line consists of 28 inverter stages, meaning that the delay increment of the coarse delay line is 28x that of the fine delay line under the same trimming cap configuration. Since 1 LSB in coarse level (i.e., 28 levels) is smaller than 5 bits in fine level (i.e., 32 levels), four delay levels are overlapped between coarse and fine steps ensuring a continuous sampling time. As will be demonstrated later, using the two delay lines helps us move the measuring point in both positive and negative directions in the time domain, and the delay line has shown excellent linearity and high timing resolution (Fig.13). A snake-shaped metal heater was implemented on M7 metal layer, covering all of the amplifier units. The amplifier circuit layout utilizes up to M6 layer. Four-terminal Kelvin sensing is used for accurate heater resistance measurement. The design details of the heater, measured temperature coefficient of resistance (TCR), and measured temperature traces are shown in Fig. 5. The TCR curve is perfectly linear allowing us to estimate the heater temperature with high confidence. By applying a large current through the metal wire, Joule heating raises the local die temperature. Using a dedicated temperature control feedback loop, the heater temperature is maintained within 1°C of the target. In terms of heater reliability, it can sustain a temperature as high as 350°C for over 100 hours without failing.

III. Waveform Reconstruction Methodology

For a given delay line trimming code, the relative position between the clock and unity gain amplifier output is fixed. Therefore, the same position of the amplifier output is compared with an external DC voltage (i.e. V_{SWEEP} in Fig. 2) repeatedly at each clock cycle. If the bias voltage is higher than the amplifier output, the counter value (N) will increment in each clock cycle; otherwise, it stays unchanged. An "S" shaped curve as shown in Fig. 6 (left), was obtained and stored in the host computer. For post-processing, the 50% occurrence criteria was chosen to represent the voltage level of the amplifier output at the given time stamp. Curve fitting was performed on each voltage sweep plot using a sigmoid function which is plotted in Fig. 6 (left). The slope in the "S" shaped curve is caused by the jitter in the delay lines as well as the voltage measurement error between different clock cycles. The slope of the fitted curve is steeper with less noise. Assuming that the sample voltage including noise follows a normal distribution, the voltage difference between the 2.5% and 97.5% occurrences is roughly four times the standard deviation (σ). The time stamp of each data point is determined by the delay difference between the two identical
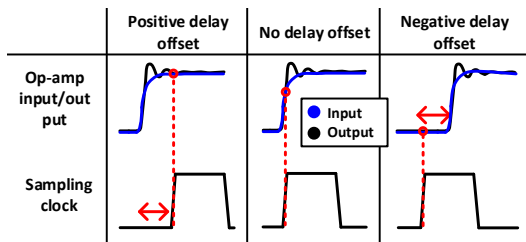
Fig. 7. Delay between the unity gain amplifier step input and the sample clock can be programmed to measure the full step response waveform.

programmable delay lines. By changing the delay trimming code, the delay difference between the two delay lines can be controlled as shown in Fig. 7. By increasing the clock signal delay, we can visit data points later in the time axis, and by increasing the amplifier input signal delay, we can visit data points earlier in the time axis. The relationship between trimming code and delay value was recorded prior to the sampling and used to reconstruct the waveform.

IV. TEST CHIP MEASUREMENT RESULTS

The output voltages of a unity gain voltage buffer circuit for a step input voltage, a step power supply voltage (power transition mode), and a step load current (load transition mode) were measured. All three step response modes use the measurement methodology described in section III. As shown in Fig. 8 (b), the step response is obtained by applying the voltage from the input step generator circuit in Fig. 3 to the amplifier. The power/load transition modes are shown in Fig. 8 (c). The power transition is achieved by periodically toggling the load current between the power rail and the ground. Measurements show that the 1.3V supply voltage drops by 160mV under our test condition. Similarly, load transition is achieved by periodically toggling the load current connected to the amplifier output. The integrated heater was

used for measurements at 125°C and 300°C, and for stressing the circuit at 350°C. The chip temperature could also be controlled by a temperature chamber for low temperature testing. Fig. 9 shows the characterization results of 8 amplifiers from the same chip at 1.3V. For the reader's convenience, we highlighted one of the eight responses in red. The input step voltage is switched from 0.4V to 0.9V. The 1.3V supply voltage used in the experiments is 100mV higher than the nominal voltage to allow more headroom during voltage overshoot events. Fig. 10 shows a summary of the overshoot, slew rate, and settling time. We can see that the overshoot decreases slightly until 125°C but degrades significantly at 300°C. The slew rate increases at higher temperatures likely due to the lower threshold voltage. The relatively small difference between the 125°C and 300°C results suggests that the threshold voltage is the dominant factor affecting amplifier slew rate rather than mobility. The settling time is generally longer below 0°C compare with room temperature and 300°C cases. Eight amplifiers were divided into stressed and fresh groups as described in section II. Before applying stress, the responses of all 8 amplifiers were characterized under 25°C and 1.3V supply voltage. Three types of signals (sinusoidal, square, and DC) were applied directly to the amplifier using a signal generator, for 40 minutes each. The amplifier response was measured every 2 hours at 25°C, 1.3V while the stress condition was applied between the measurements. 100 hours of total stress was applied. The delay line was also powered on to maintain correct operation. Since we were concerned about the degradation in the delay line, we re-characterized them after each 2 hour stress cycle. All three types of transition are characterized under 25°C. The measurement (counter toggling) of different amplifiers occurs simultaneously and then read out serially. By using two identical structures (i.e., two delay lines and two DUTs), common-mode effects could
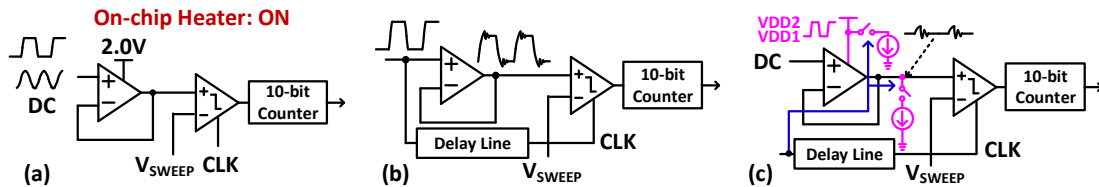

Fig. 8. Testing modes supported by the test chip: (a) High-temperature high-voltage stress mode. (b) Step response measurement mode. (c) Load transition and power transition response measurement mode.
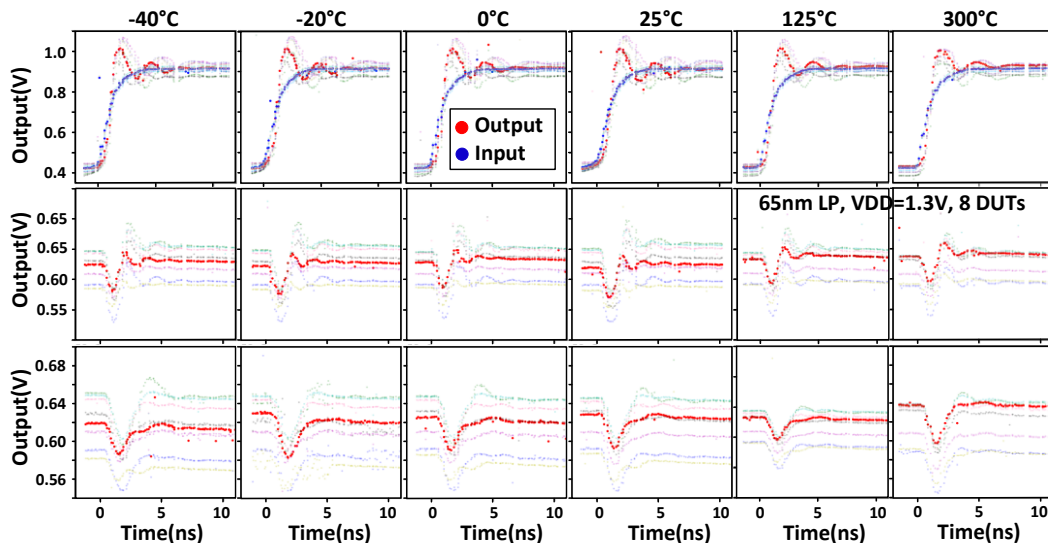

Fig. 9. Unity gain amplifier step response (first row), load transition response (second row), and power transition response (third row) at -40°C, -20°C, 0°C, 25°C, 125°C (on-chip heater), and 300°C (on-chip heater)
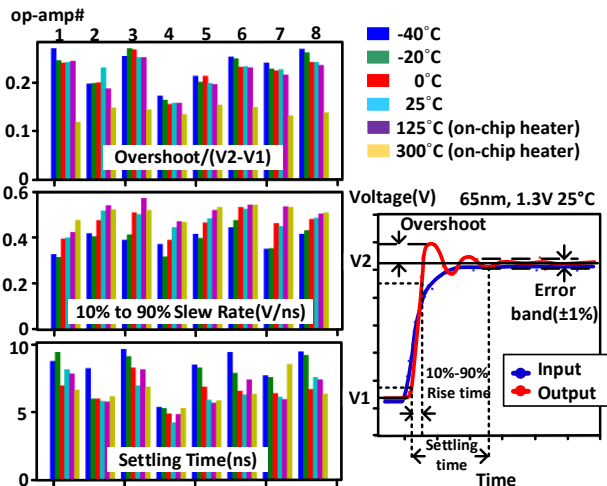
Fig. 10. Overshoot (normalized to voltage swing), slew rate, and settling time measured from eight identical amplifiers at five different temperatures.
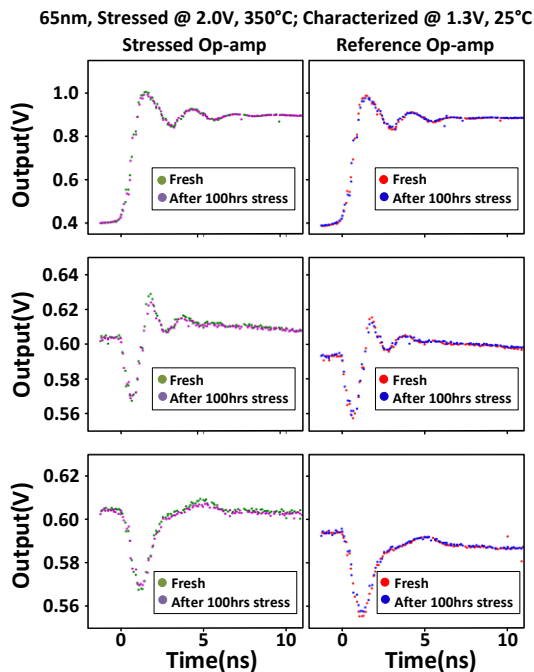

Fig. 11. Amplifier response before (fresh) and after 100 hours of stress for stressed (VDD=2.0V) and reference amplifiers (VDD=0V).
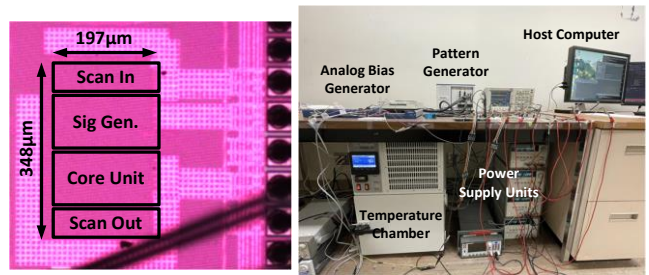

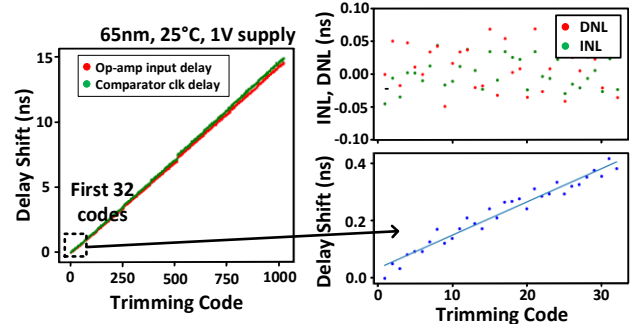Fig. 12. 65nm test chip die photo and testing setup.

Fig. 13. Measured delay shift, DNL, and INL of the programmable delay line

V. CONCLUSION

In this paper, an on-chip amplifier response monitor based on the sub-sampling technique is presented. For characterization at extremely high temperatures, we implemented an on-chip heater that is placed above the amplifier circuits. Three types of step responses were recorded and analyzed under different temperatures, ranging from -40°C to 300°C. The amplifier circuits were exposed to a 350°C stress temperature and an overdrive voltage of 2.0V for reliability assurance. Stress data revealed no noticeable degradation in the amplifier response characteristics.

be rejected, ensuring high linearity and high accuracy. Fig. 11 shows all three response types for both stressed and reference amplifiers, compared with their time zero behavior. The amplifier behavior before and after 100 hours of stress did not show an observable difference. Similar trends were observed for both load transition and power transition responses. We can conclude that the amplifiers used in this study are extremely robust and hence suitable for extreme temperature operation. Fig. 12 shows the 65nm test chip die photo and testing environment. Fig. 13 (left) shows the measured delay versus the 10-bit trimming code. Delays of the first 32 trimming code are shown, together with the ideal linear curve, in Fig. 13 (lower right). In Fig. 13 (upper left), the differential nonlinearity (DNL, delay difference between consecutive trimming steps) and integrated nonlinearity (INL, difference between generated delay and ideal level) are displayed together with the trimming code. Both show equally distributed positive and negative points. From the INL plot, we can conclude that the resolution of the programmable delay line is 50psec.

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