CICC

IEEE Custom Integrated Circuits Conference

Coupled Oscillator based Computing: Using Nature to Solve Difficult Problems

Chris Kim

University of Minnesota

March 26th 2021

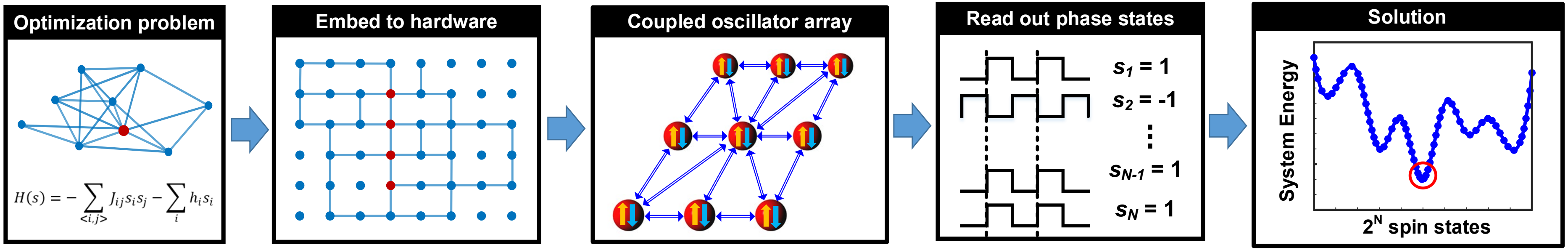
Outline

- Introduction to Ising Computers
- Current State of the Art
- Case Study: 560 Coupled Oscillator Test Chip
- Commercialization Effort and Outlook
- Summary

Context and Disclaimer

- This presentation focuses on
  - a new computing paradigm
  - in early stages of research
  - that is highly exploratory and somewhat finicky
  - with very little experimental data available in public domain
- Sit back and relax (with an open mind)

Ising Spin Glass Model

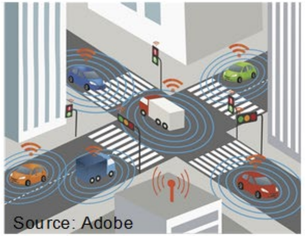


- A promising approach for efficiently solving NP-hard or NP-complete problems (e.g. combinatorial optimization problems, Boltzman machines, associative memories, Karp's 21 NP-complete problems)

$H(s) = -\sum_{<i,j>} J_{ij} s_i s_j - \sum_i h_i s_i$: Ising Hamitonian (Cost Function)

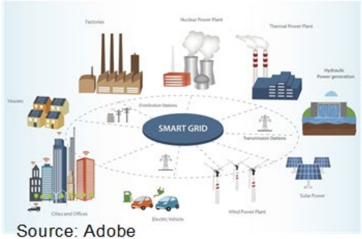
s_i, s_j : Spin state {+1 or -1} J_{ij} : Coupling strength h_i : local field strength

Autonomous vehicles

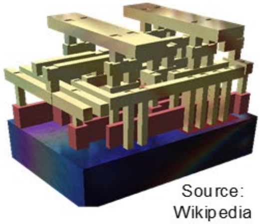


Communication networks

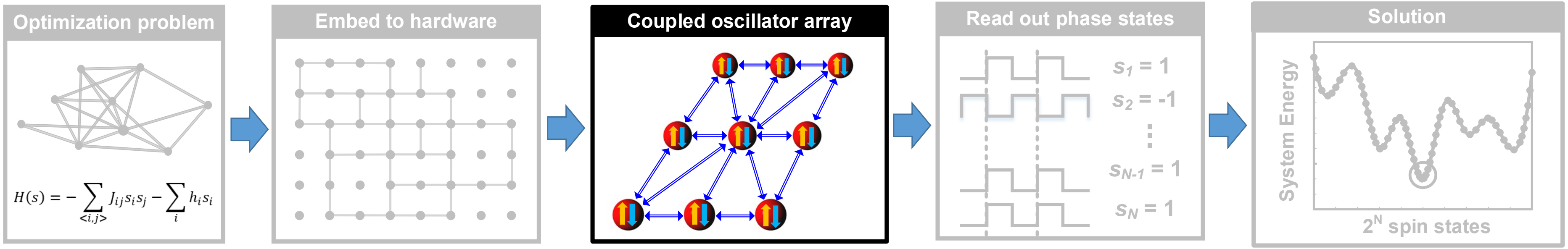
Smart grid



VLSI routing



Using Nature to Find the Ground State



Random states (time=0)

Same states (time = 1 min)

Youtube: Coupled Metronomes

Example Problem #1: Factorizing 15

$$\mathrm{p} = (x_1\ 1)_2\ ,\mathrm{q} = (x_2\ x_3\ 1)_2$$
$$H = (15 - pq)^2$$

$$H = 128x_1x_2x_3 - 56x_1x_2 - 48x_1x_3 + 16x_2x_3 - 52x_1 - 52x_2 \text{-} 96x_3 + 196$$

$$H_{mod} = 200x_1x_2 - 48x_1x_3 - 512x_1x_4 + 16x_2x_3 - 512x_2x_4 + 128x_3x_4 - 52x_1 - 52x_2 - 96x_3 + 768x_4 + 196$$

S. Jiang, et al., “Quantum Annealing for Prime Factorization”, Scientific Reports 2018

Example Problem #2: Graph Coloring

For graph $G(V,E)$ of the map problem—no two vertices, V, connected by an edge, E, should select the same color from set C—construct a cost function with binary variables, $x_{v,c} = 1$ when $v \in V$ selects color $c \in C$, by implementing two constraints:

$$(\sum_c x_{v,c} - 1)^2,$$

which has minimum energy (zero) when vertices select one color only, and

$$\sum_c \sum_{v_a,v_b \in E} x_{v_a,c} x_{v_b,c},$$

which adds a penalty if the vertices of an edge select the same color.

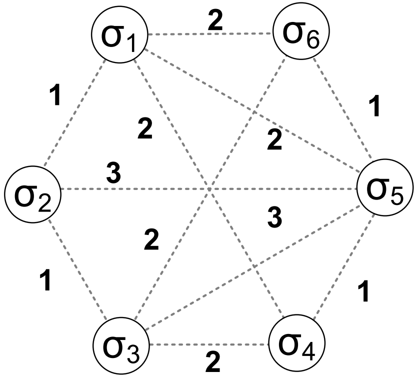
These constraints give a QUBO,

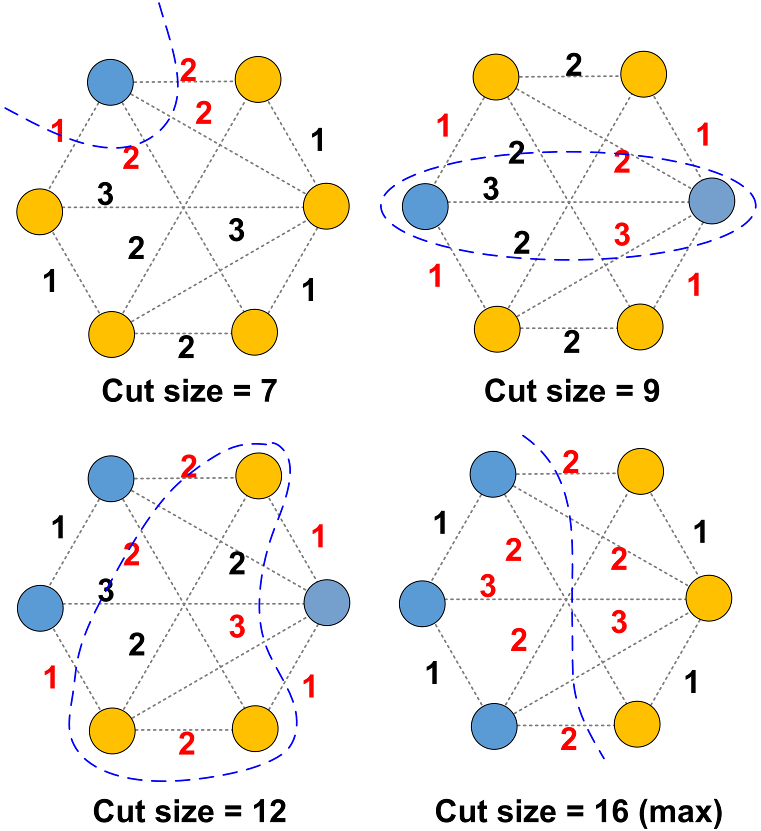
$$E(x_v, x_{v_a,v_b}) = \sum_v (\sum_c x_{v,c} - 1)^2 + \sum_c \sum_{v_a,v_b \in E} x_{v_a,c} x_{v_b,c}.$$

D-Wave Problem-Solving Handbook, 8/13/20

e.g. $x_{Minn,Red} = 0, x_{Minn,Blue} = 0,$
$x_{Minn,Sand} = 1, x_{Minn,Green} = 0$
$x_{Wisc,Red} = 0, x_{Wisc,Blue} = 1,$
$x_{Wisc,Sand} = 0, x_{Wisc,Green} = 0$

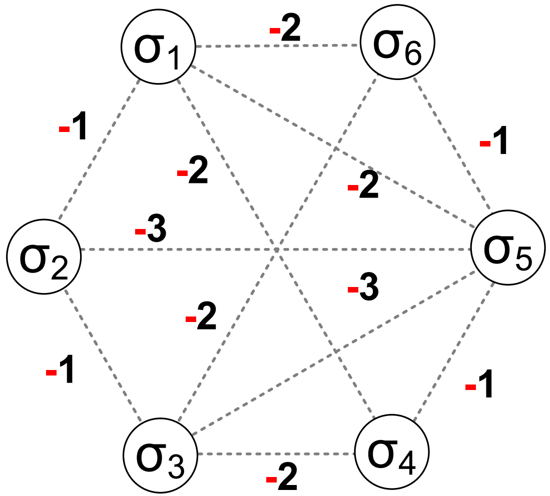
Example Problem #3: Finding Max-cut





- The problem of finding a maximum cut in a graph is known as the Max-Cut Problem
- Finding max-cut of a graph is an *NP-hard* problem

Example Problem #3: Finding Max-cut



$$
\begin{aligned}
H(\sigma) &= -\sum_{i,j}(-w_{ij})\,\sigma_i\sigma_j \\
&= \sum_{diff\ group}(-w_{ij}) + \sum_{same\ group} w_{ij} \\
&= \sum_{diff\ group}(-w_{ij}) + \left[\sum_{i,j} w_{ij} - \sum_{diff\ group} w_{ij}\right] \\
&= \sum_{all} w_{ij} - 2 \times \underbrace{\sum_{diff\ group} w_{ij}}_{\text{Cut size}}
\end{aligned}
$$

H = Hamiltonian of the system

σ_i = Spin status of magnet i {+1 or -1}

w_{ij} = weight between magnets i and j

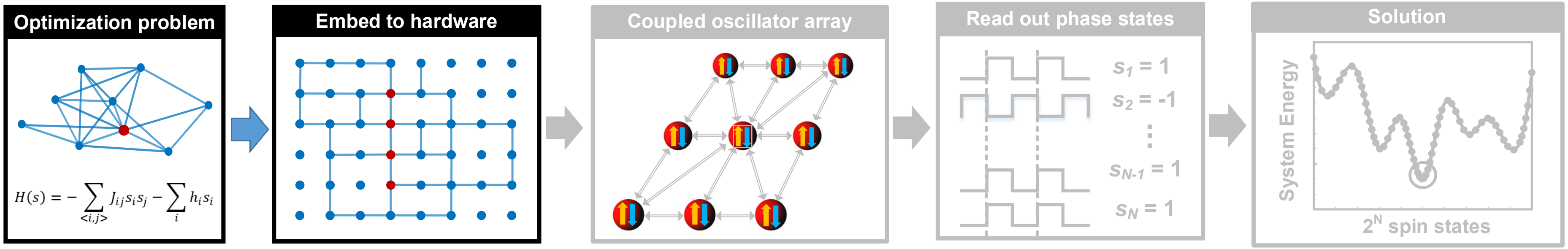
- Ising Hamiltonian = [sum of all weights] – 2×[cut size]

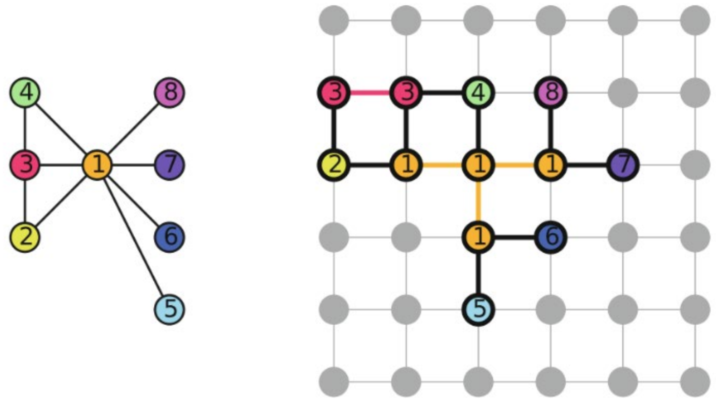
Other NP Problems Mappable to the Ising Model

- Partitioning problems (e.g. max cut)
- Binary integer linear programming
- Covering and packing problems
- Problems with inequalities
- Coloring problems (e.g. graph coloring)
- Hamiltonian cycles (e.g. traveling salesman)
- Tree problems
- Graph isomorphisms
- …

A. Lucas, "Ising formulations of many NP problems", Frontiers in Physics, Feb. 2014

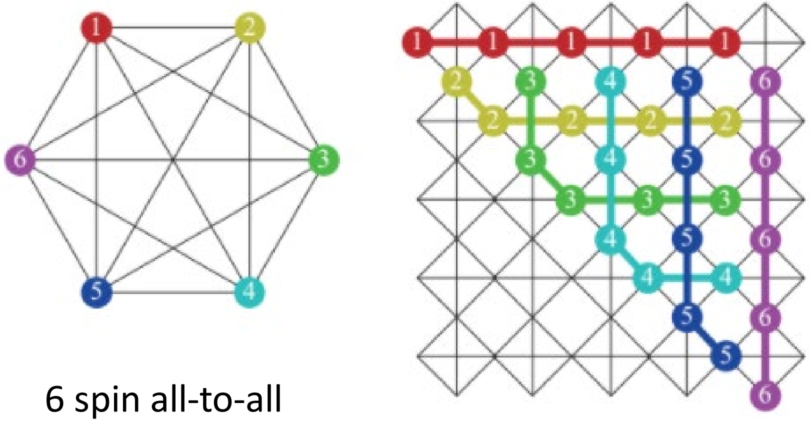
Example of Graph Embedding





G

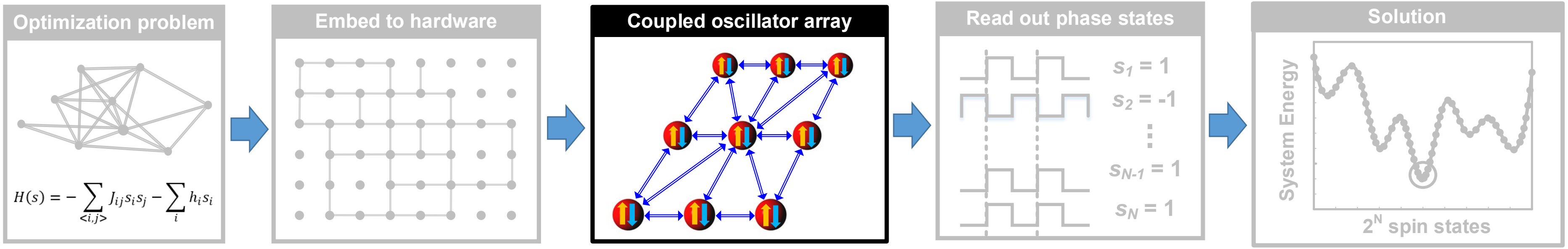
Gemb

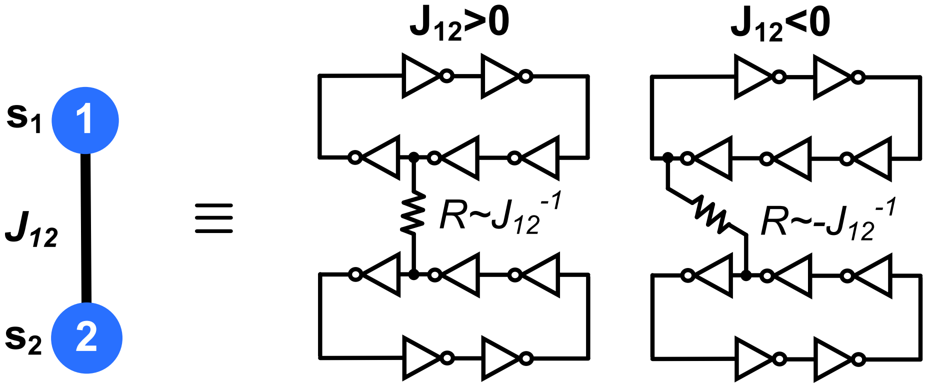


6 spin all-to-all

King's architecture

Using Coupled Oscillators to Find the Ground State



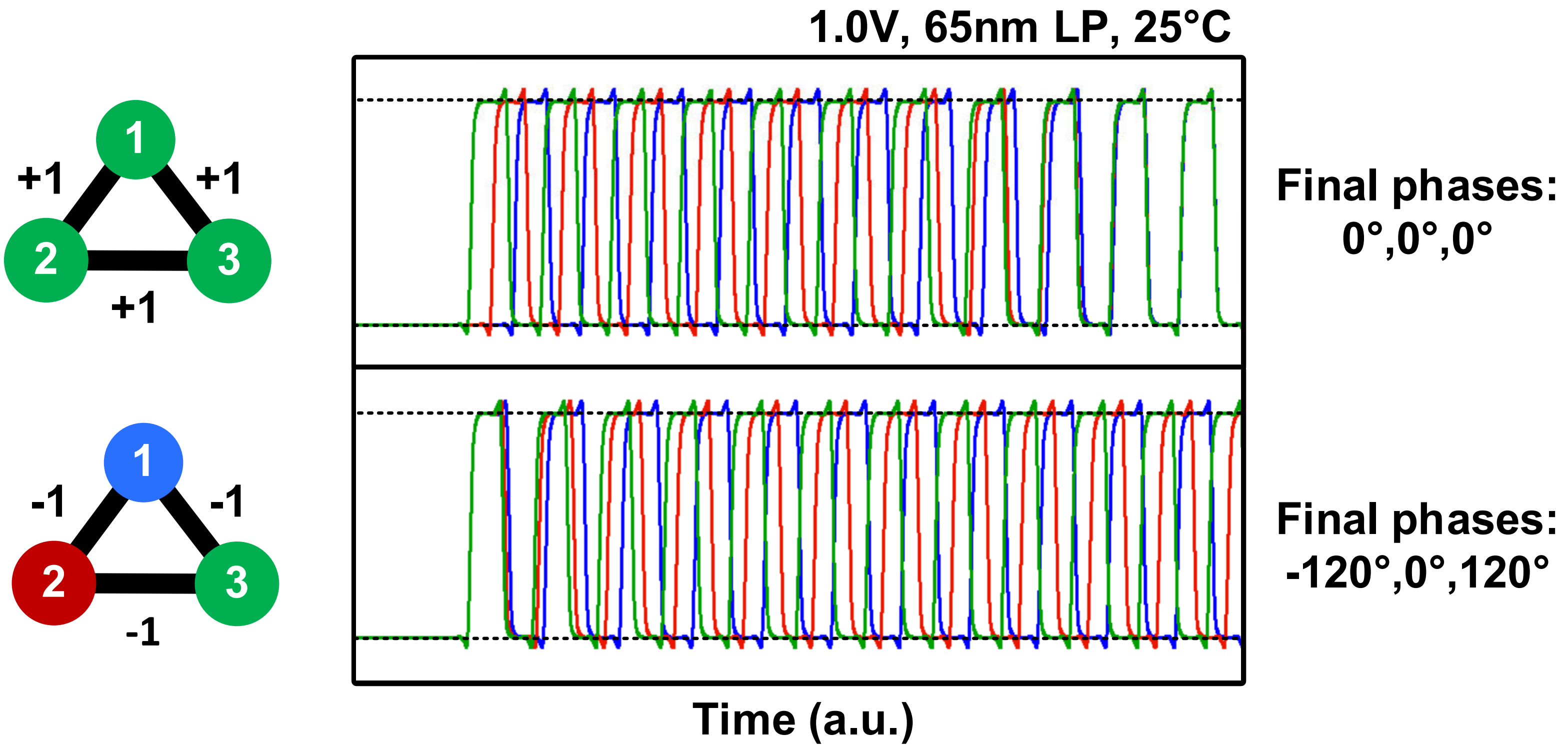


$$H(s) = -J_{ij} s_i s_j$$

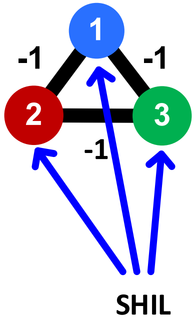
if $J_{ij} > 0$, then $\{s_i, s_j\}$={+1,+1} or {-1,-1} : Same phase

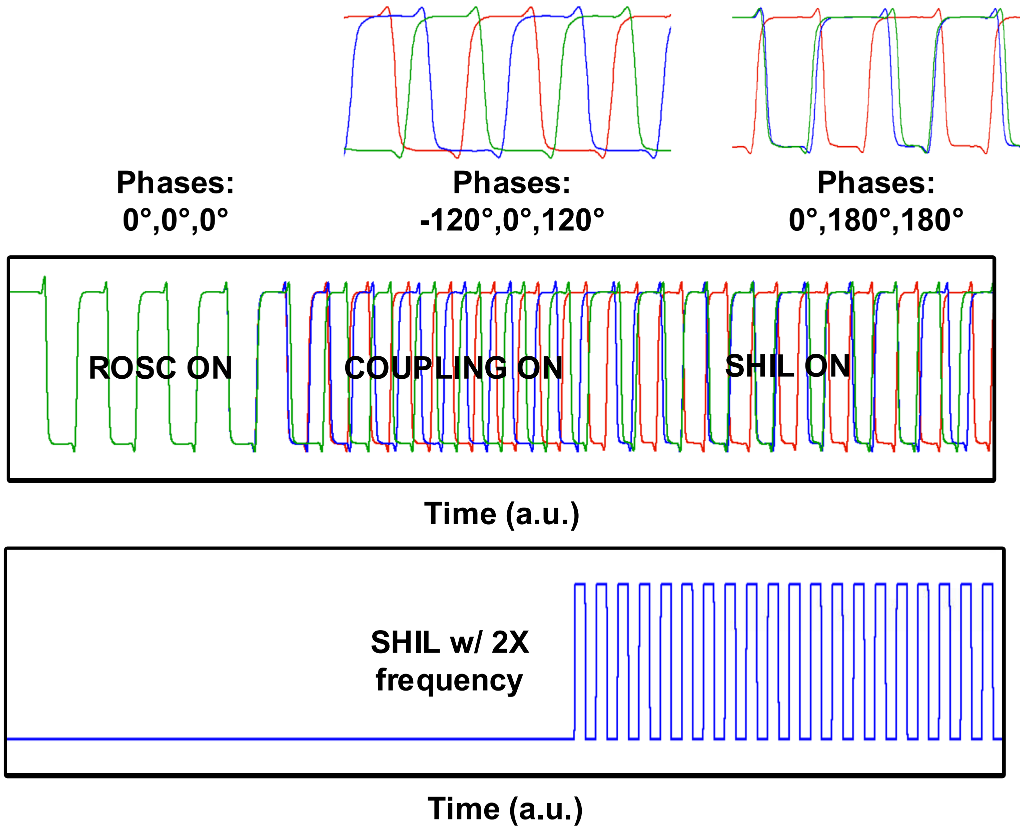
if $J_{ij} < 0$, then $\{s_i, s_j\}$={+1,-1} or {-1,+1} : Opposite phase

Using Coupled Oscillators to Find the Ground State

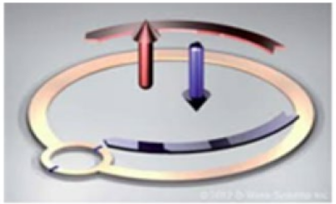


Super Harmonic Injection Locking (SHIL) Signal

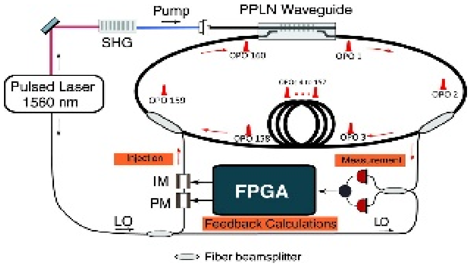




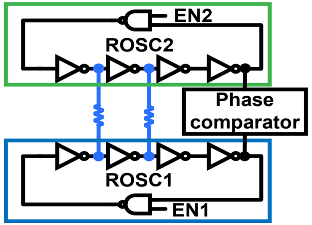
Other Oscillator Devices



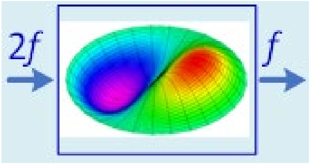
Superconducting qubits



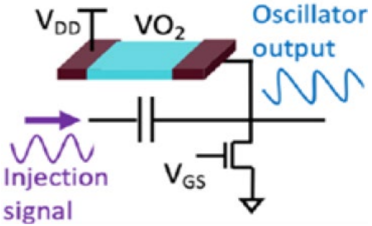
Optical fiber



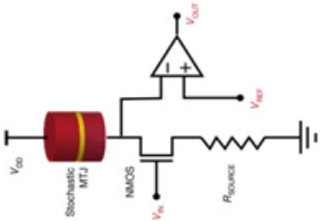
CMOS



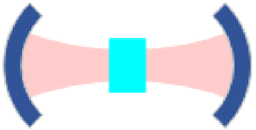
MEMS/NEMS



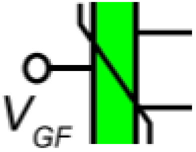
Phase transition material



Magnetic tunnel junctions



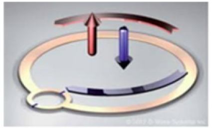
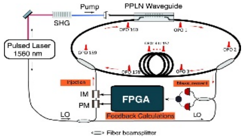
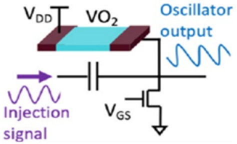
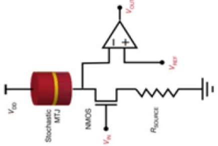
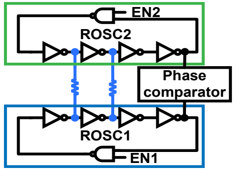
Cavity parametric oscillator



Ferroelectric

Sources: Google image, IEDM 20, EDL2017, Science 2016

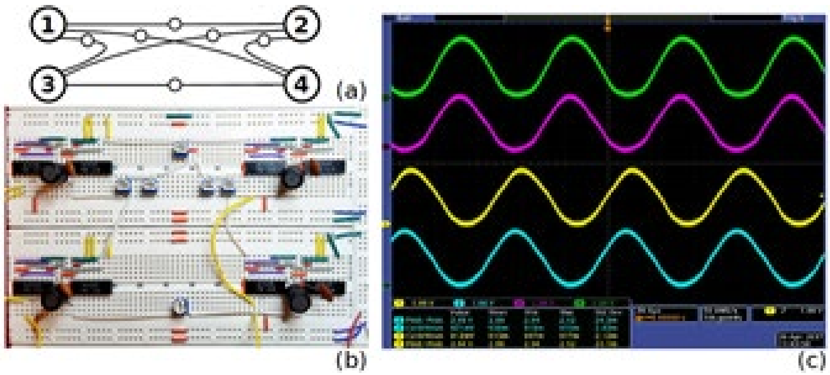
Comparison of Coupled Oscillator Technologies

	Qubit	Optical	Phase transition	Spintronic	CMOS
Conceptual figure					
# of oscillators	~2000 (single chip)	100-2000 (lab setup)	4 (probe station)	8 (board level)	2000+ (1.3mm^2 chip in 65nm)
Advantages	Under debate	Room temperature	Room temperature	Room temperature	Room temperature, leverages CMOS, cloud/edge computing
Disadvantages	Cryogenic cool, 25kW power, premature tech. cloud only	1km optical fiber, FPGA chip, complex setup	Premature device, no real area advantage over CMOS	Premature device, no real area advantage over CMOS	Will it outperform GPUs and software solvers?
Integrated system in 10 yrs?	No	No	No	No	Yes
Target applications	NP-hard and NP-complete combinatorial optimization problems (e.g. supply chain, AI/ML, transportation, smart grid, communication, IC design, bioinformatics, computer vision, and robotics)				

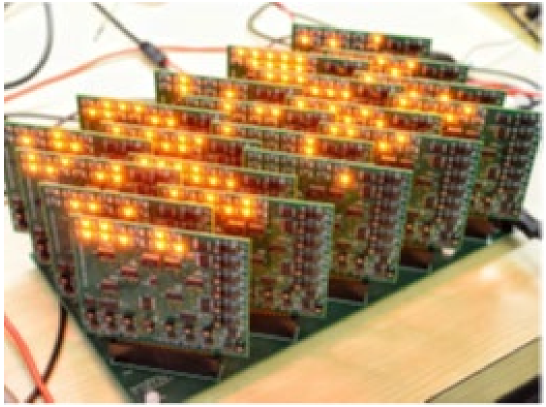
Outline

- Introduction to Ising Computers
- Current State of the Art
- Case Study: 560 Coupled Oscillator Test Chip
- Commercialization Effort and Outlook
- Summary

Breadboard and PCB Implementation



T. Wang, *arXiv*, 2017 (UC Berkeley)



T. Wang, *arXiv*, 2019 (UC Berkeley)

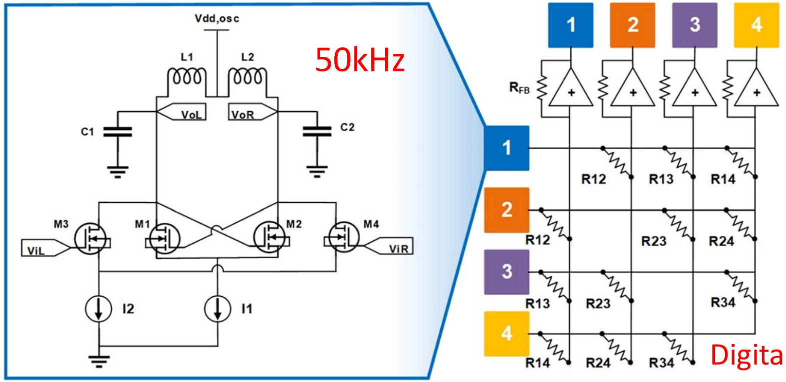
Pros:

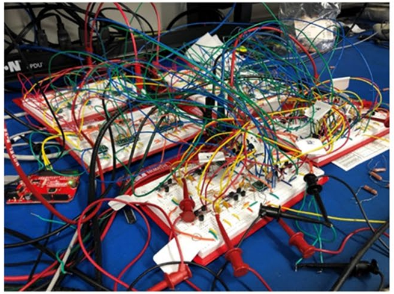
Can achieve coupling dynamics, good for proving the concept

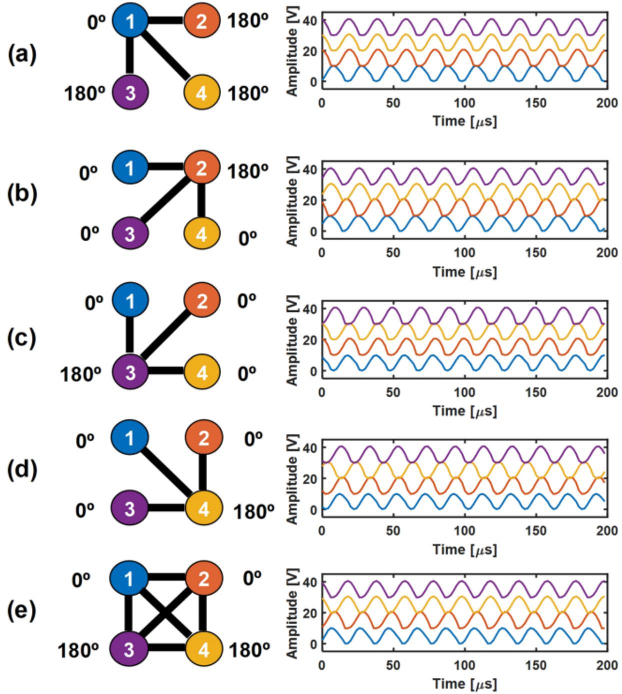
Cons:

Not practical for large number of programmable spins, not an integrated solution

Breadboard and PCB Implementation







J. Chou, S. Bramhavar, et al., Scientific Reports, 2019 (MIT Lincoln Labs)

Pros:

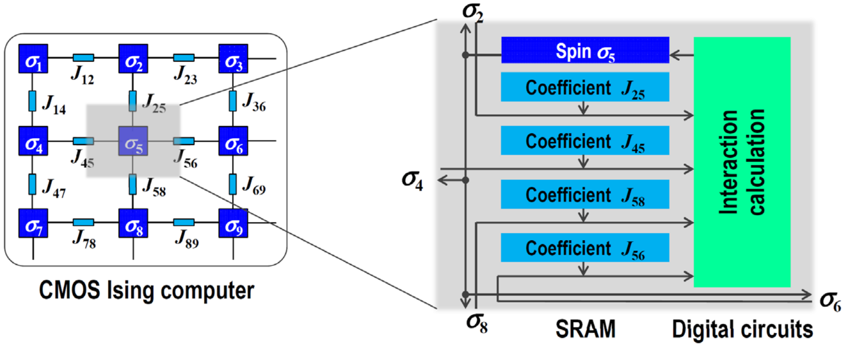
Can achieve coupling dynamics, good for proving the concept, **all-to-all coupling using crossbar architecture**

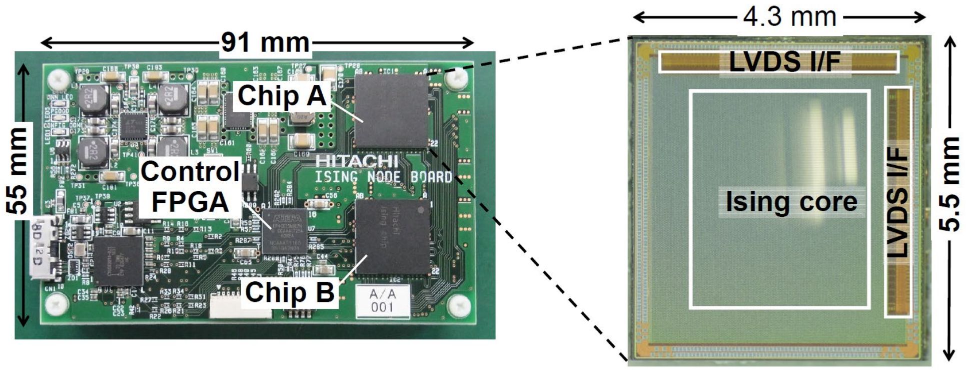
Cons:

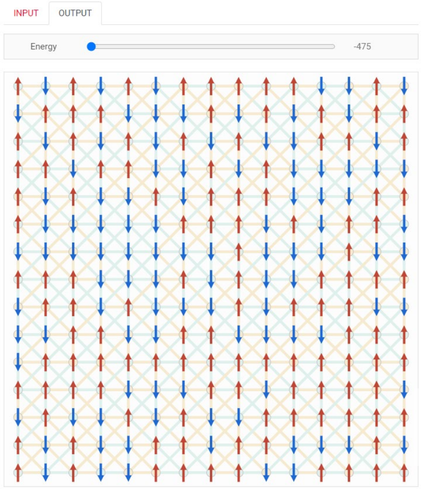
Not practical for large number of programmable spins, not an integrated solution

ASIC Implementation

M. Yamaoka, *JSSC*, 2016 (Hitachi)
T. Takemoto, *ISSCC*, 2019 (Hitachi)







Pros:

Can theoretically solve a wide variety or problems

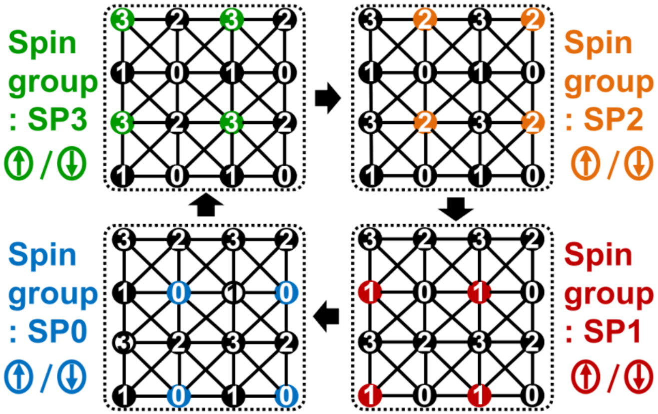
Cons:

1. No coupling dynamics : computation time and energy may be higher
2. Search for better solution is time dependent

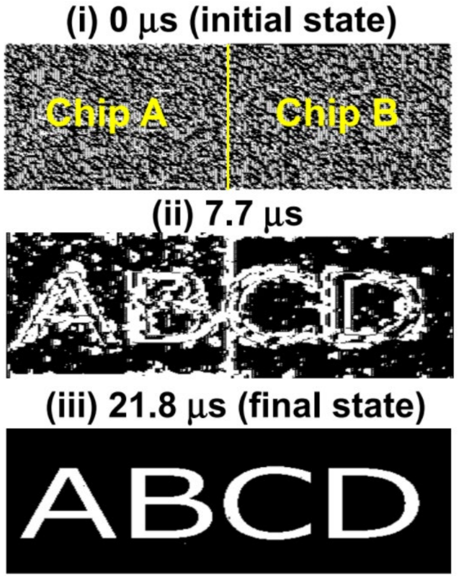
Real time demo available at www.annealing-cloud.com

ASIC Implementation

T. Takemoto, *ISSCC,* 2019 (Hitachi)



	D-Wave 2000Q	ISSCC2015 (previous)	This work
Method	Quantum annealing	Simulated annealing	
Accuracy	Better	Not so good	Good
Implementation	Superconductor	65-nm CMOS	40-nm CMOS
Number of connected chips	No	No	2 (multichip in principle)
Number of spins	2k	20k	2×30k
Bit width of coefficients	N/A	2 bits	3 bits
Annealing time*	N/A	10 ms***	22 μs
Energy efficiency*, **	N/A	2200 times***	1.75×10^5 times



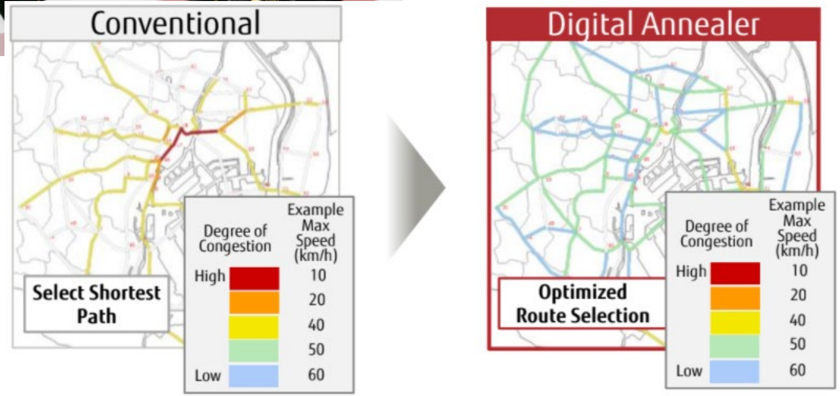
Pros:

Can theoretically solve a wide variety or problems

Cons:

1. No coupling dynamics : computation time and energy may be higher
2. Search for better solution is time dependent

ASIC Implementation



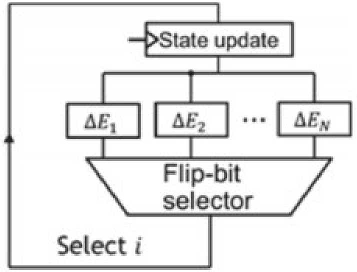


Fig. 1. A diagram of the parallel search technique

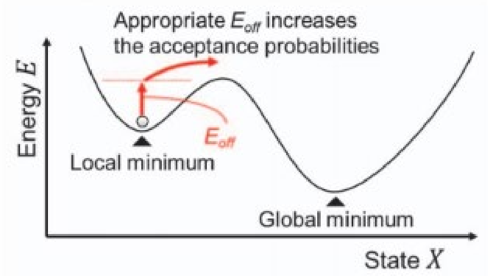


Fig. 2. A diagram of the escape technique

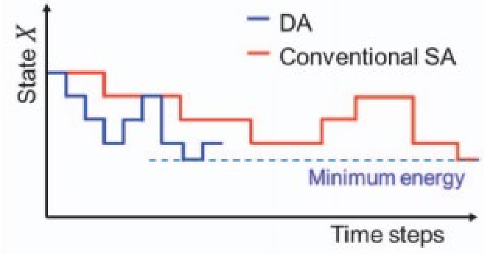


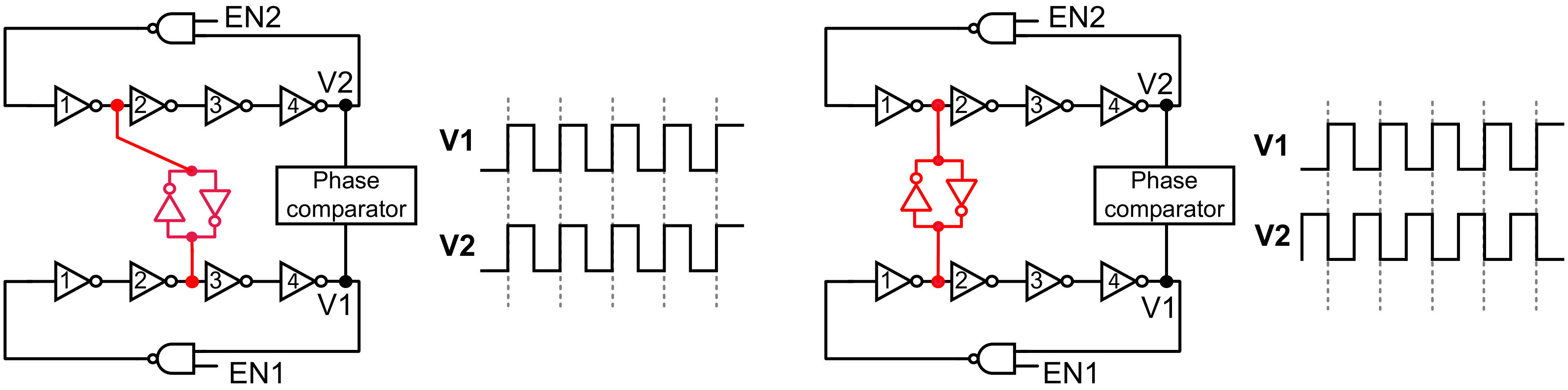
Fig. 3. Conceptual diagram of speed-up achieved by DA

S. Matsubara, et al., ASP-DAC 2020 (Fujitsu)

Outline

- Introduction to Ising Computers
- Current State of the Art
- Case Study: 560 Coupled Oscillator Test Chip
- Commercialization Effort and Outlook
- Summary

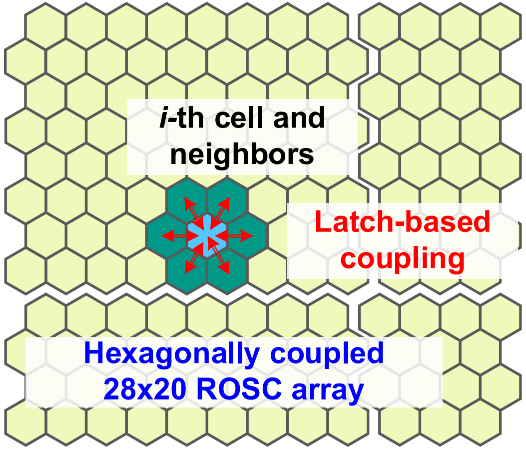
ROSC Coupled Using Digital Latches



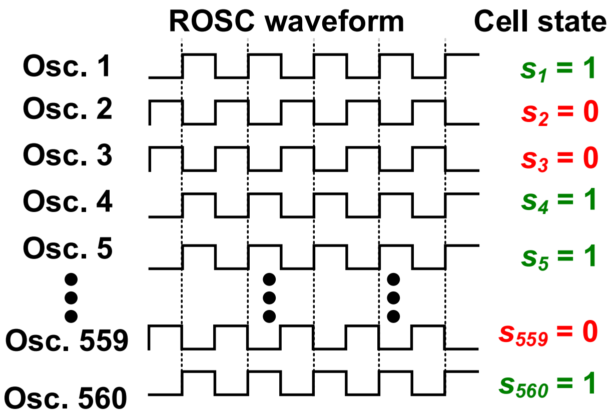
a) Positive coupling **b) Negative coupling**

- Any coupling medium that enables energy transfer may couple ROSCs
- ROSC and digital latches are designed with global and local enable signals

Choice of Architecture



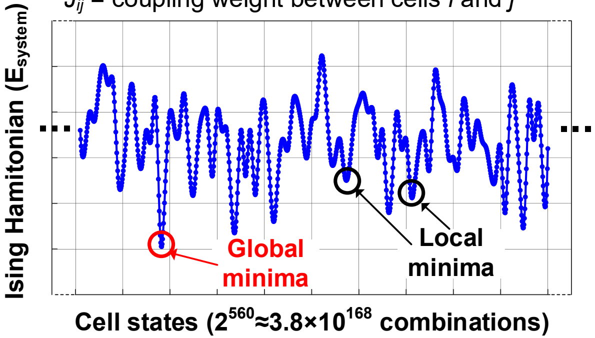
Proposed architecture



ROSC waveform and unit cell states

$$E_{system} = -\sum_{i=1}^{N}\sum_{j=1}^{n_i} J_{ij} \cdot s_i \cdot s_j$$

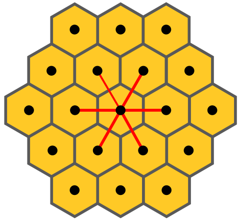
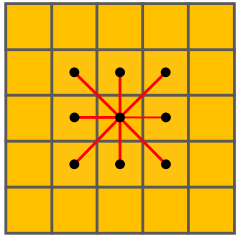
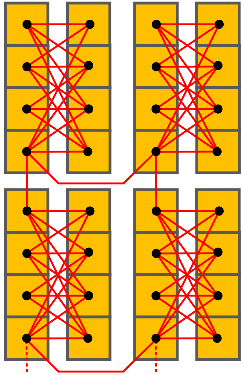
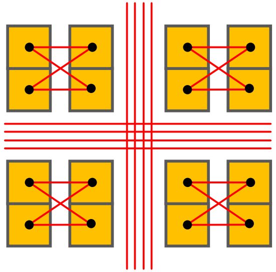
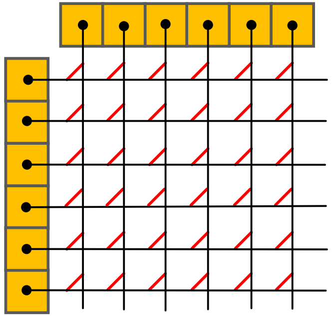
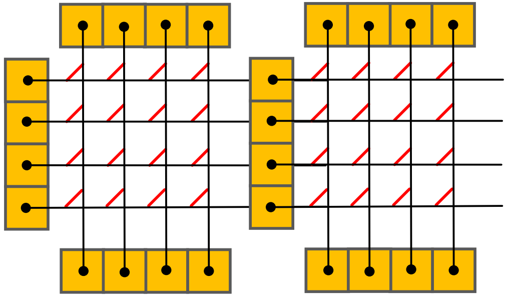
n_i = number of coupled neighbors of i-th cell,
J_{ij} = coupling weight between cells i and j



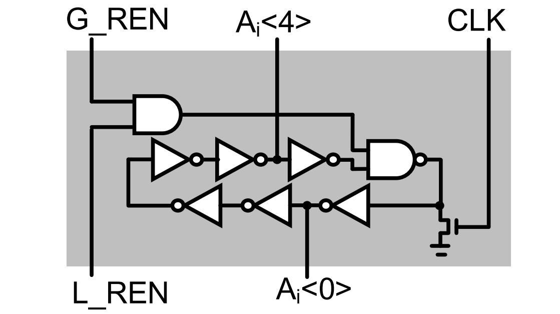
System energy of the Ising computer

- Hexagonal unit cell maximizes the number of neighbors in 2D plane
- Latch based coupling between cells is digitally controlled

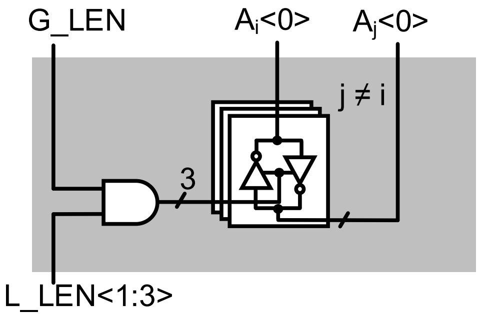
Other Possible Architectures

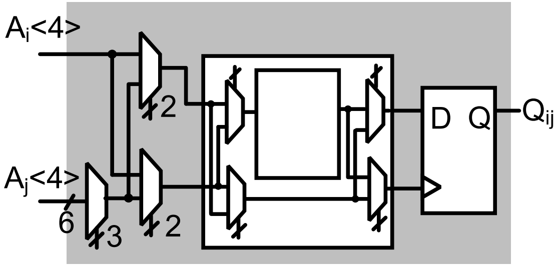
Modular Unit Cell: Circuit Blocks



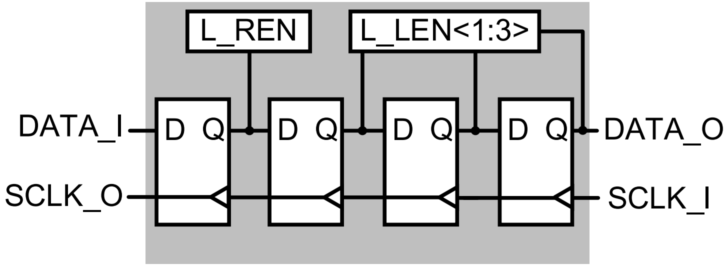
a) ROSC block



b) Latch coupling block



c) Read block

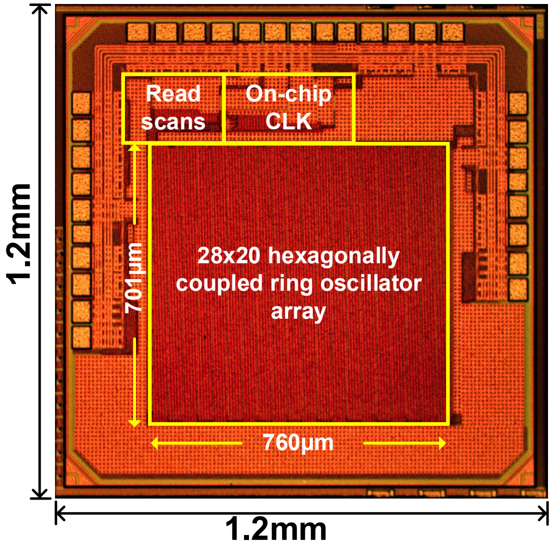


d) Scan block

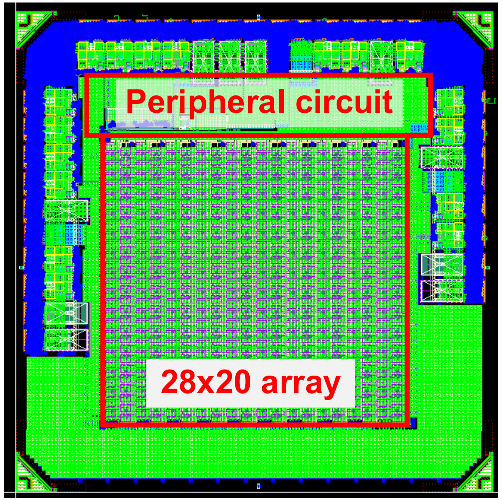
- Read block samples one of the neighboring ROSC
- Scan block programs the graph: four program bits per cell, 2,240 bits for the chip

CICC

Die Photo and Chip Summary



Die photo



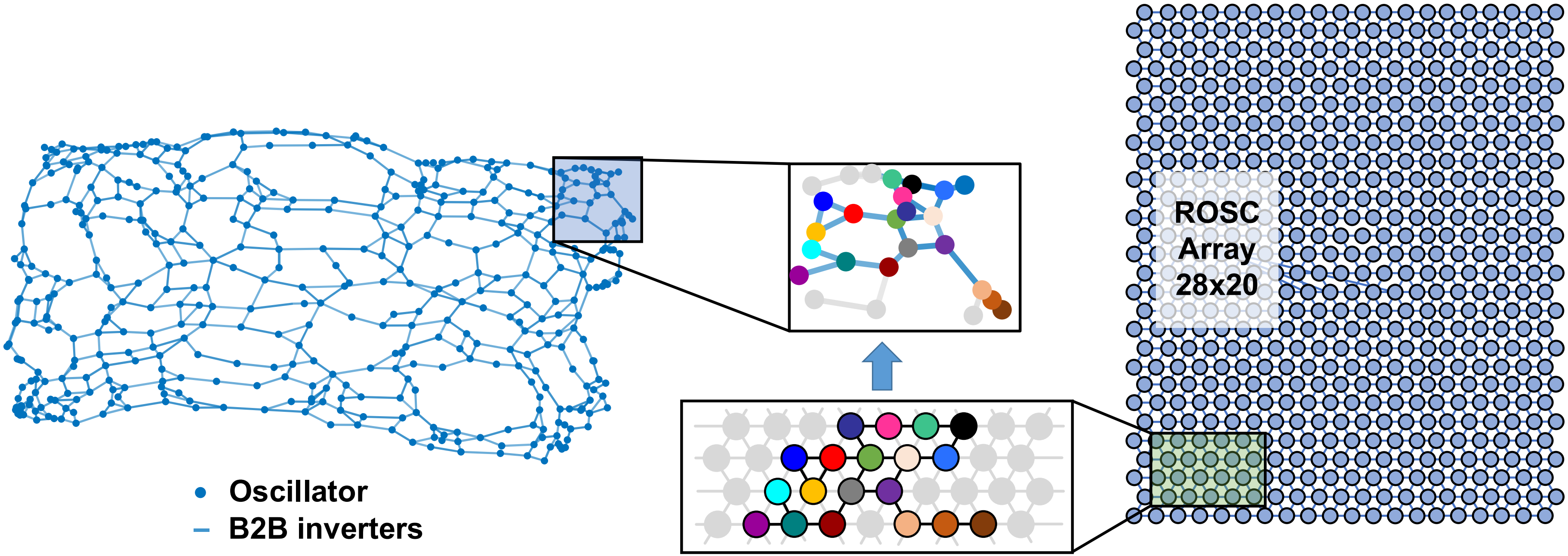
Full chip layout

Application	Combinatorial optimization problems
Process	65nm CMOS
Architecture	ROSC, latch based coupling, self-annealing
Voltage	1.0V
Area	Chip: 1.44mm^2
	Core: 0.53mm^2
	Unit cell: 0.00095mm^2
Peak power	23mW
Power per cell	41µW

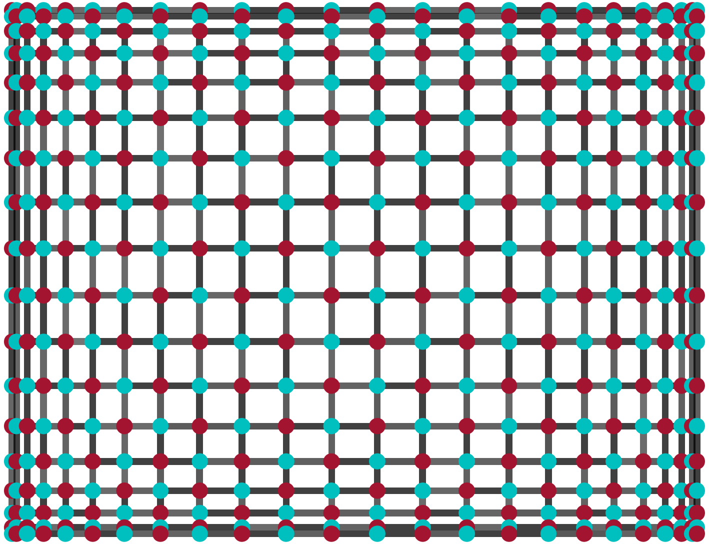
Chip summary

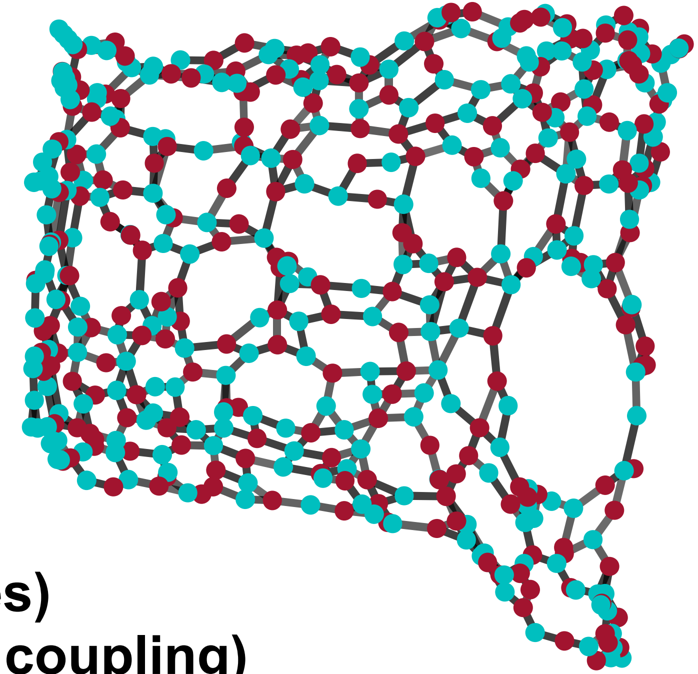
- 28x20=560 coupled oscillators (only limiting factor is chip area)
- Oscillator area < 5% of the full chip area

Embedding Ising Problem to Hardware



Example Problems (Regular versus Random Graphs)

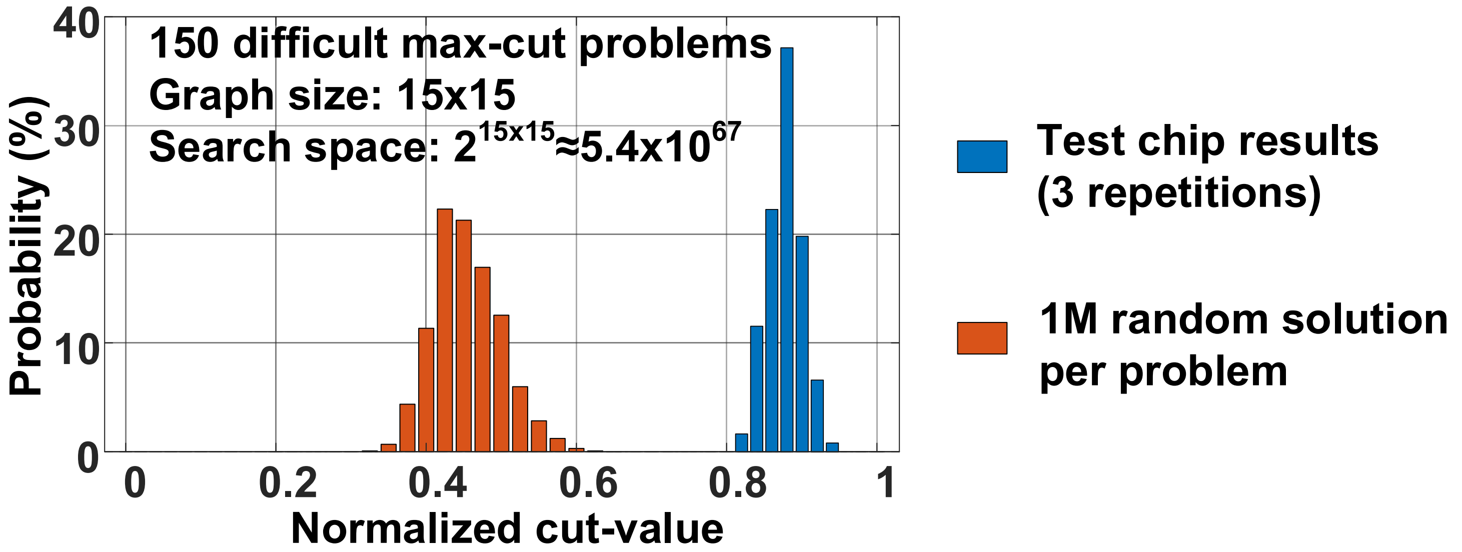




Oscillator (+1 or -1 states)

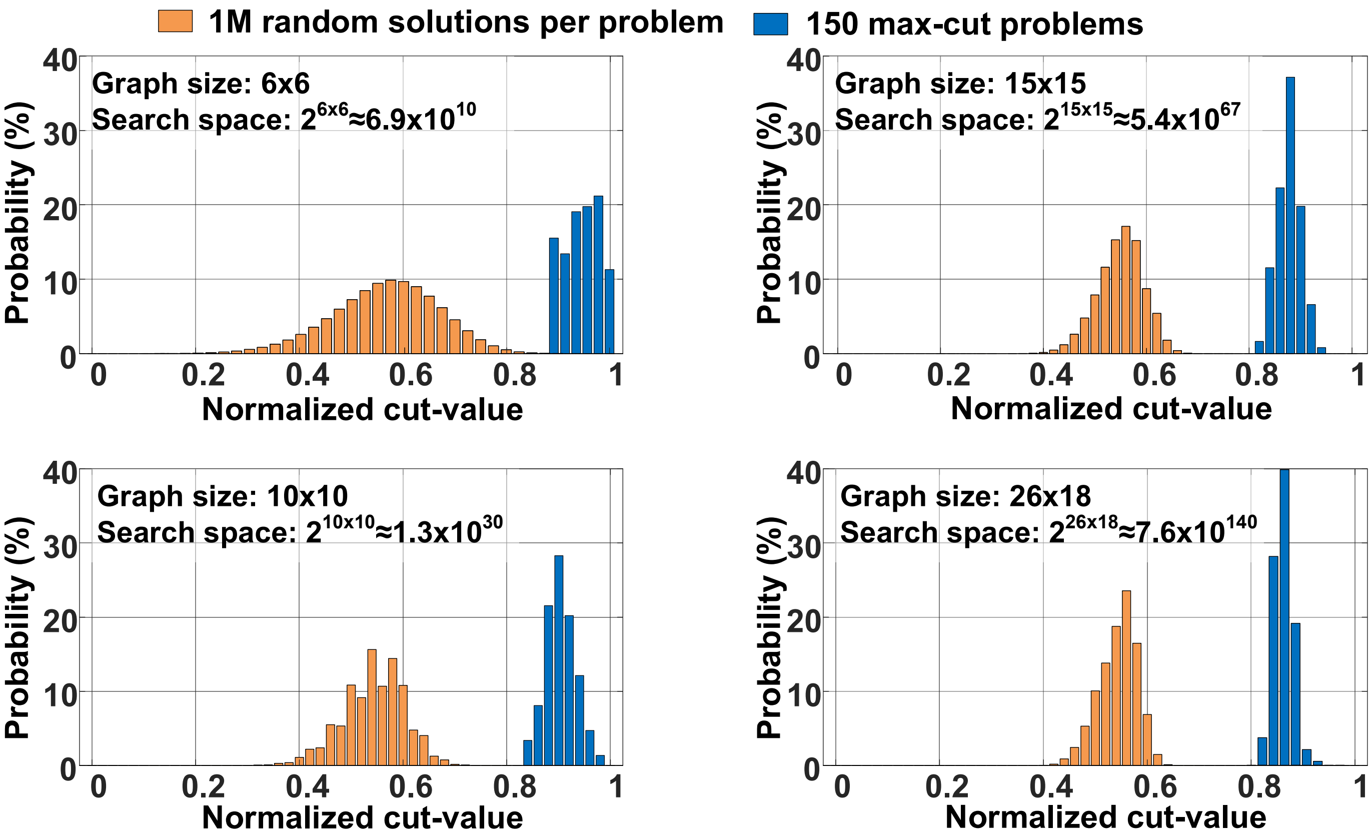
B2B inverters (negative coupling)

Max-cut Results for 15x15 Graphs

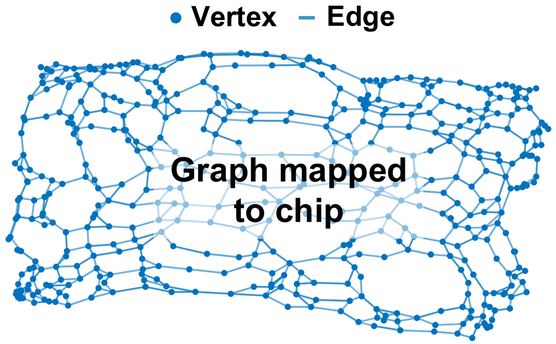


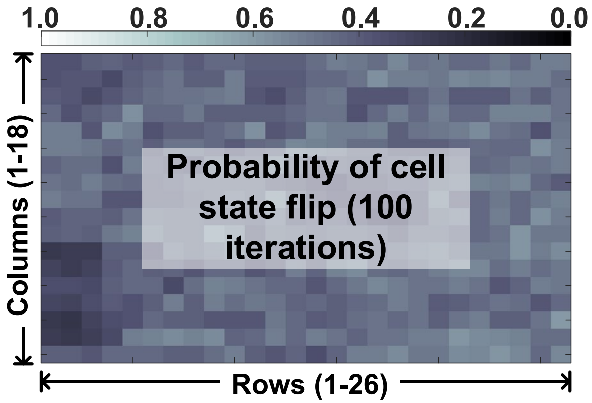
- 150 difficult COPs are mapped and max-cut results are measured for each graph sizes
- Measured results are compared with 1 million randomly sampled solutions from the solution-space for each specific graph.

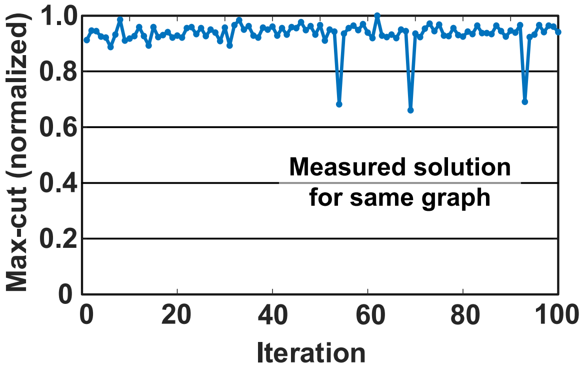
Max-Cut Results for Different Graph Sizes

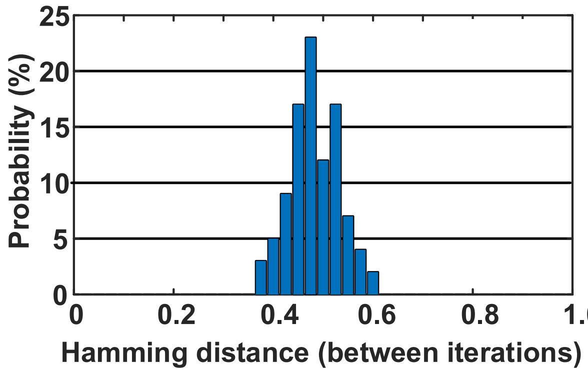


Repeated Experiment for Same Graph



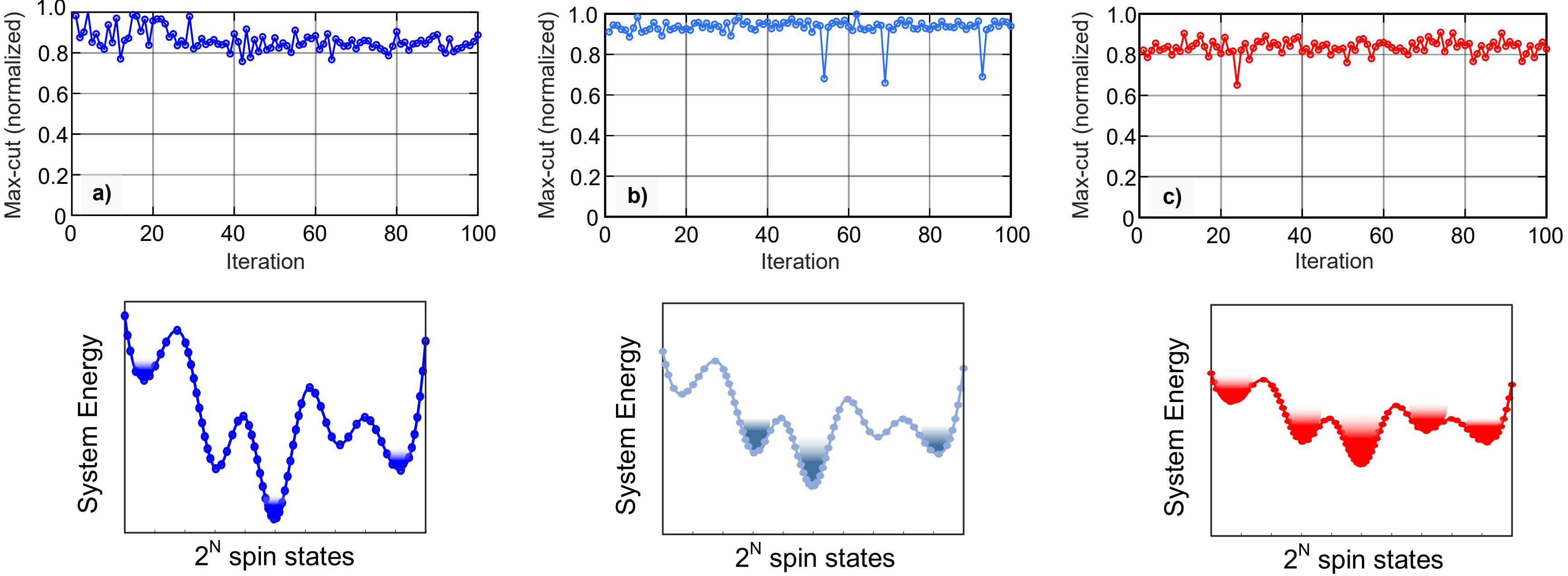






Temperature versus Solution Quality

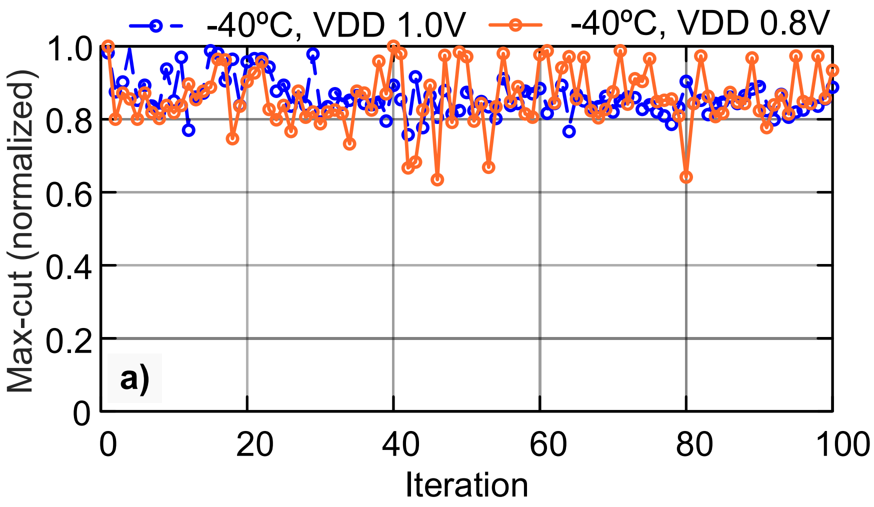
Temperature: -40°C | Temperature: 25°C | Temperature: 90°C

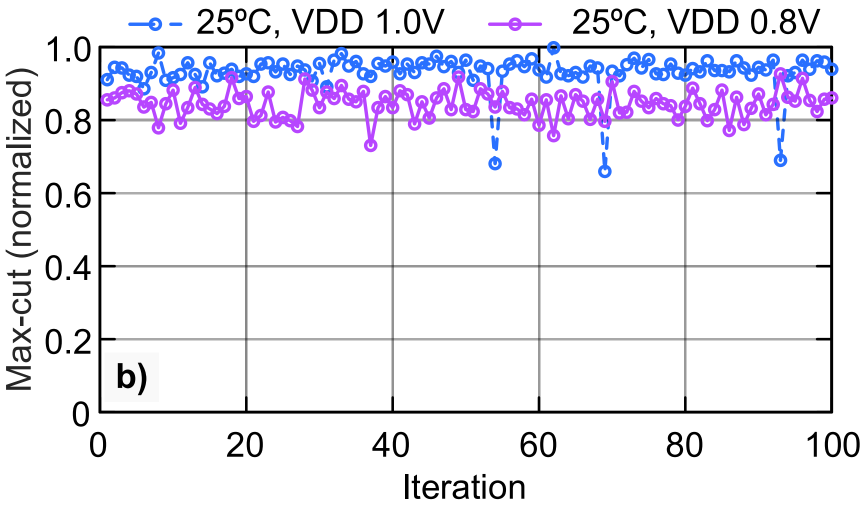


Low temperature:
lower noise, stronger coupling

High temperature:
higher noise, weaker coupling

Supply Voltage versus Solution Quality



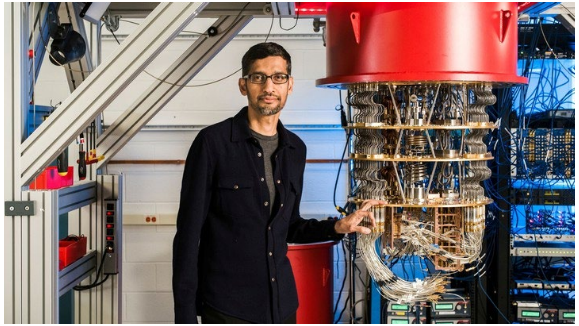


- Lower VDD → higher noise & weaker coupling
- Higher VDD → lower noise & stronger coupling

Outline

- Introduction to Ising Computers
- Current State of the Art
- Case Study: 560 Coupled Oscillator Test Chip
- Commercialization Effort and Outlook
- Summary

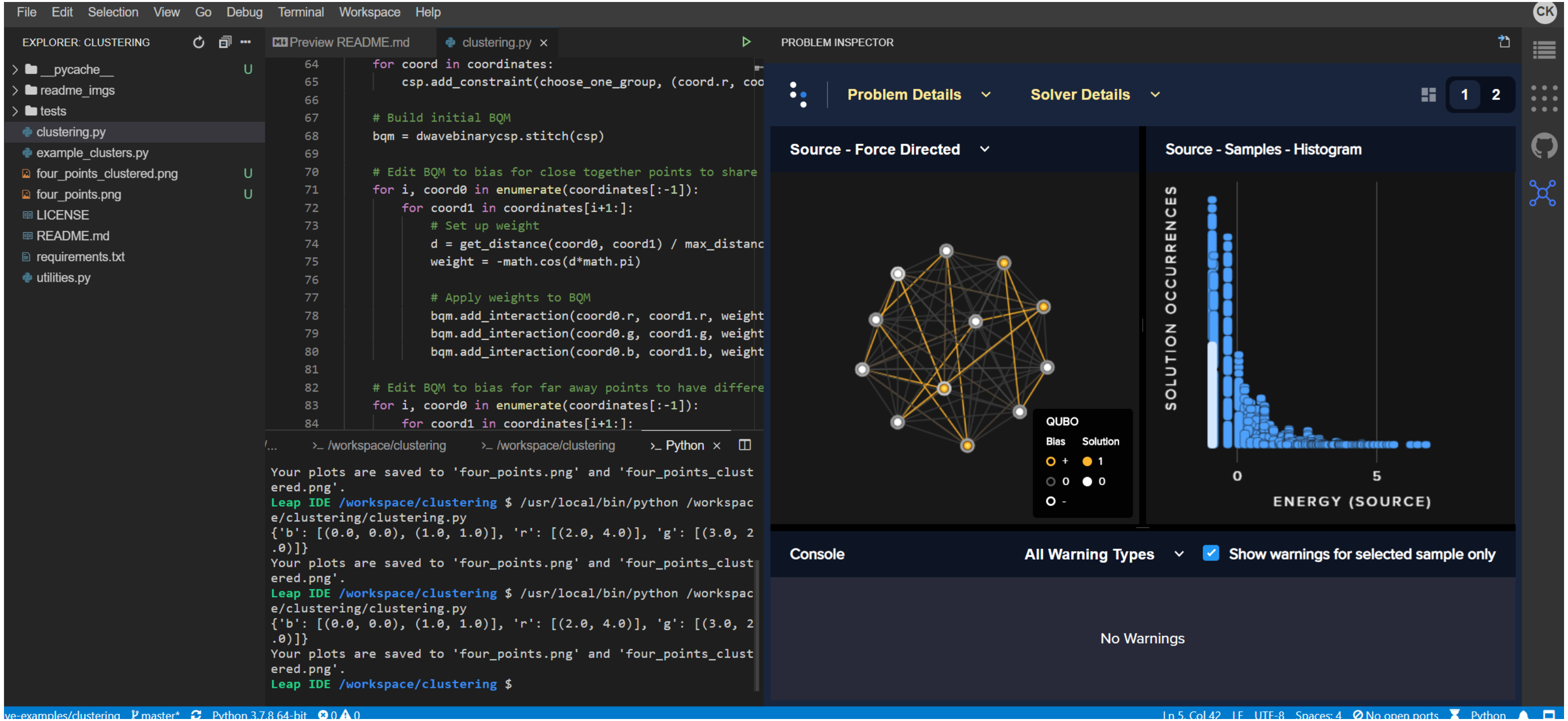
Other Developments: Quantum Computing Startups



Investments:
Dwave >$204M
IonQ > $82M
Rigetti > $198M
PsiQuantum > $215M
IBM, Toshiba, Hitachi, Intel, Google, Microsoft, NASA, LANL, Amazon AWS, Lockheed, …

Challenges:
Kilowatts of cooling power per chip
Large form factor
Limited scalability
Expensive (e.g. $15M/chip)
Immature technology

Dwave Quantum Annealer



AWS Braket

Quantum Processing Units (QPUs)

D-Wave — Advantage_system1.1

Quantum Annealer based on superconducting qubits

Qubits	Status
5760	ONLINE
Region	Next available
us-west-2	AVAILABLE NOW

D-Wave — DW_2000Q_6

Quantum Annealer based on superconducting qubits

Qubits	Status
2048	ONLINE
Region	Next available
us-west-2	AVAILABLE NOW

IonQ

Universal gate-model QPU based on trapped ions

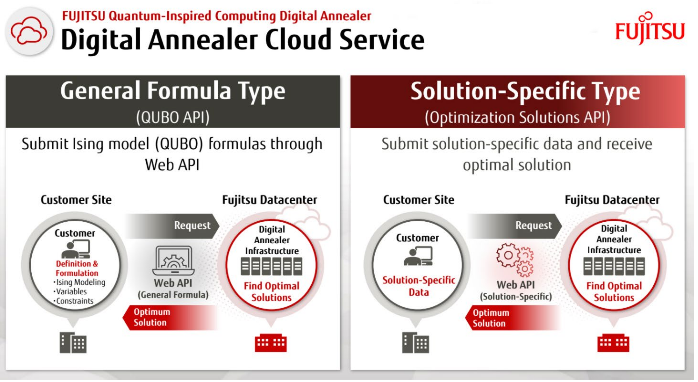
Qubits	Status
11	ONLINE
Region	Next available
us-east-1	08:14:38

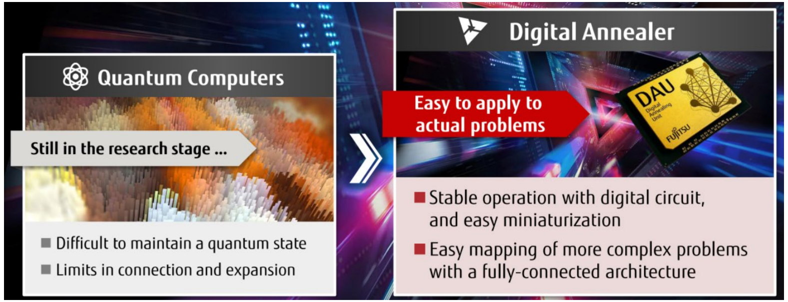
Rigetti — Aspen-8

Universal gate-model QPU based on superconducting qubits

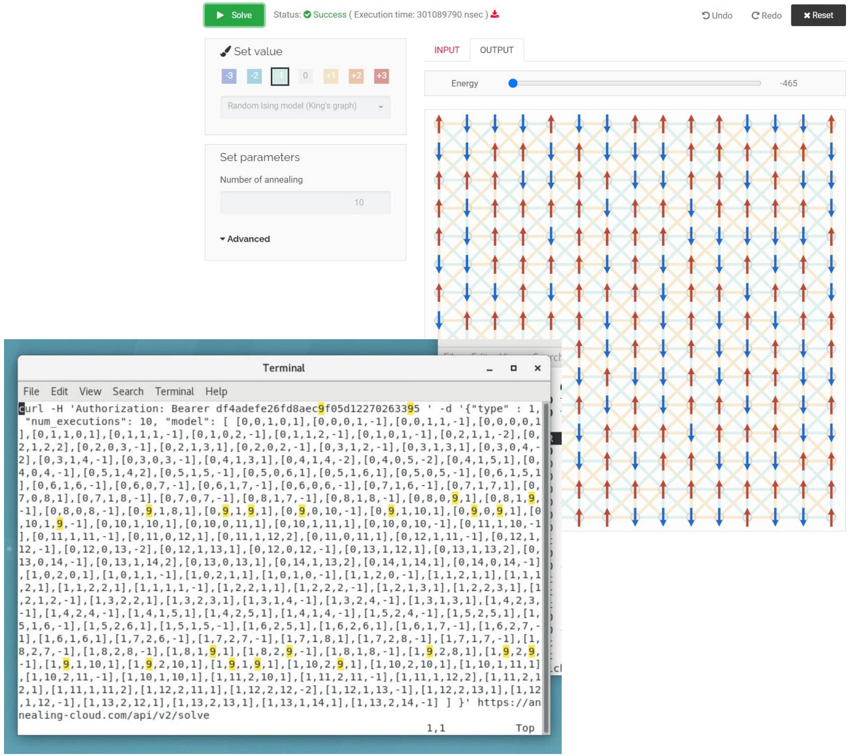
Qubits	Status
31	ONLINE
Region	Next available
us-west-1	10:14:38

Fujitsu and Hitachi's Digital Annealers





www.annealing-cloud.com



Key Takeaways

- NP-hard optimization problems could be the key driver for future computing growth
- A true coupling based integrated CMOS Ising computer was demonstrated in 65nm
  - Probabilistic exploration of various local minima
  - Mapped and solved 1,000 COPs in the chip with an accuracy of 82%-100%
- For oscillator based computing to be a viable approach however, there has to be a clear and significant power-performance-area advantage over
  - Mathematical optimizers (available today)
  - GPU, FPGA, Custom ASICs, digital annealers (available today)
  - Quantum computers


OBRIGADO
gracias
どうも
ARIGATO
hvala
DANK U
takk
MERSI
merci
obrigado
danke schön
köszi
سپاس
PALDIES
muchas gracias
ありがとう
TEŞEKKÜR EDERIM
MOLTE GRAZIE
GO RAIBH MAITH AGAT
謝謝
danke
grazas
THANK YOU
благодаря
GRAZZI
TAK
どうも
THANKS
qujan
TAK
благодаря
asante
muchas gracias
vielen dank
PALDIES
DANK U
OBRIGADO
mesi
grazie
DZIEKI
спасибо
MULTUMESC
danke
TACK
Gràcies
多謝
شكراً
감사합니다
köszi
TEŞEKKÜR EDERIM
muchas gracias
obrigado
NA GODE
NA GODE