A 32Gb/s Digital-Intensive Single-Ended PAM-4 Transceiver for High-Speed Memory Interfaces Featuring a 2-Tap Time-Based Decision Feedback Equalizer and an In-Situ Channel-Loss Monitor

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Outline

• Introduction
• Time Based PAM-4 Decision Feedback Equalizer
• In-situ Channel Loss Monitor
• 65nm Test Chip Results
• Summary
Voltage-based vs. Time-based DFE

DFE: Decision Feedback Equalization

Voltage-based DFE
- Circuit: Current mode logic, Differential
- Pros: Ultra high speed
- Cons: Headroom issues, limited taps, large power consumption

Time-based DFE
- Circuit: Inverter delay line, Single-ended
- Pros: Scalable to large number of taps, low power consumption
- Cons: Moderate speed
Memory Interface Trends

- Single-ended signaling, lower supply voltage
- Data rate higher than 16 Gb/s
- Multi drop memory bus with more reflection

T. Hollis, Solid-State Magazine, 2019

Time-based DFE becoming an attractive alternative
Pulse Amplitude Modulation (PAM)

NRZ

PAM-4

• PAM-4 overtaking NRZ but requires more accurate conversion from voltage signal to time delay signal
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Differential Voltage to Time Converter

### VTC (Prior art)

- Two path delays change with opposite polarity
- Non-linearity cancelled out by subtracting delays

### DVTC (This work)

- DVTC: Differential VTC

\[ \Delta T = T_{RX} - T_{REF} \]

\[ \Delta T = T_{RXP} - T_{RXN} \]

\[ D=0 \]

\[ D=1 \]
Differential Voltage to Time Converter

VTC (Prior art)

DVTC (This work)

• Delay range improves from 42ps to 70ps
NRZ Signal Comparison

Threshold delay generated by VTC in reference delay line
PAM-4 Signal Comparison

- Simple buffer can generate the different threshold delays for PAM-4. Separate DAC circuit not required.
PAM-4 Signal Comparison

- Simple buffer can generate the different threshold delays for PAM-4. Separate DAC circuit not required.
PAM-4 Time-Based Receiver

- Half-rate operation
- 12 delay lines and 6 phase detectors (PD)
PAM-4 Time-Based Receiver

From DVTC, Even
RX_{N,E}, T_{REF,H}, T_{W2X2}, PD, FF
RX_{P,E}, T_{BUF}, T_{W1X1}

From DVTC, Odd
RX_{N,O}, T_{REF,H}, T_{W2X2}, PD, FF
RX_{P,O}, T_{BUF}, T_{W1X1}

V_{11}, RX_{N}, RX_{P}
V_{10}, RX_{N}, RX_{P}
V_{10}, RX_{N}, RX_{P}
V_{01}, RX_{P}, RX_{N}
V_{01}, RX_{P}, RX_{N}
V_{00}, RX_{P}, RX_{N}
PAM-4 Time-Based Receiver
PAM-4 Time-Based Receiver

From DVTC, Even

From DVTC, Odd

PAM-4 Decoder + Eye Monitor

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Test Chip Diagram of PAM-4 Transceiver

- RX: DVTC, PAM-4 TB-DFE, and BER monitor
- TX: PRBS, clock generator, FFE, and driver
- In-situ channel loss monitors on both sides
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Proposed Channel Loss Monitor

- Measure the toggling frequency of comparator output while sweeping reference voltage
• Frequency decreases at higher data rates
• Small discrepancy can be attributed to random digital pattern generated by PRBS (vs. sinusoidal input)
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BER Bathtub and Time-Domain Eye Diagram

65nm GP, 1.2V, 25°C, 32Gb/s, 8GHz

X-axis: Phase (time)
Y-axis: Time offset (time)

Bit Error Rate

-0.3 -0.2 -0.1 0 0.1 0.2 0.3

Phase (UI)

-1E-12 -1E-9 -1E-6 -1E-3 -1E-0

w/o DFE
w/ DFE

w/ DFE

1E-9

1E-6

1E-3

1E-0

1E+3

1E+6

1E+9

1E+12

0 24 48 72 96 120 144 168 192

Time Offset (code)

BER

<10^-9

10^-8

10^-7

10^-6

10^-5

10^-4

10^-3

10^-2

10^-1

<10^-0

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## Die Photo and Feature Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
</tr>
<tr>
<td>Circuit Area</td>
<td>TX: 31x72µm²</td>
</tr>
<tr>
<td></td>
<td>RX: 89x73µm²</td>
</tr>
<tr>
<td>VDD</td>
<td>1.2V</td>
</tr>
<tr>
<td>Data Rate</td>
<td>32 Gb/s</td>
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<tr>
<td>Channel Loss</td>
<td>11.6dB@8GHz</td>
</tr>
<tr>
<td>BER</td>
<td>&lt;10⁻¹²</td>
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<tr>
<td>Power Efficiency</td>
<td>0.97 pJ/b</td>
</tr>
</tbody>
</table>
## Performance Comparison Table

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td><strong>Signaling</strong></td>
<td>Duobinary</td>
<td>PAM-3</td>
<td>Muti-Band</td>
<td>NRZ</td>
<td>PAM-4</td>
</tr>
<tr>
<td><strong>RX Circuit Type</strong></td>
<td>Voltage-Based</td>
<td>Voltage-Based</td>
<td>Voltage-Based</td>
<td>Time-Based</td>
<td>Time-Based</td>
</tr>
<tr>
<td><strong>RX Equalization</strong></td>
<td>1-Tap DFE</td>
<td>1-Tap DFE</td>
<td>Self-Equalization</td>
<td>2-Tap DFE</td>
<td>2-Tap DFE</td>
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<tr>
<td><strong>Data Rate</strong></td>
<td>7 Gb/s</td>
<td>27 Gb/s</td>
<td>10 Gb/s</td>
<td>12.5 Gb/s</td>
<td>32 Gb/s</td>
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<tr>
<td><strong>Technology</strong></td>
<td>65nm</td>
<td>28nm</td>
<td>28nm</td>
<td>65nm</td>
<td>65nm</td>
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<tr>
<td><strong>Voltage</strong></td>
<td>1.05V</td>
<td>0.6V</td>
<td>1.2V</td>
<td>0.8V</td>
<td>1.2V</td>
</tr>
<tr>
<td><strong>Channel Loss</strong></td>
<td><a href="mailto:0.8dB@3.5GHz">0.8dB@3.5GHz</a></td>
<td>20mm</td>
<td>6dB@6GHz</td>
<td><a href="mailto:14dB@6.25GHz">14dB@6.25GHz</a></td>
<td>11.6dB@8GHz</td>
</tr>
<tr>
<td><strong>BER</strong></td>
<td>&lt;1E-12</td>
<td>&lt;1E-12</td>
<td>&lt;1E-12</td>
<td>&lt;1E-12</td>
<td>&lt;1E-12</td>
</tr>
<tr>
<td><strong>TRX Area</strong></td>
<td>0.0333 mm²</td>
<td>0.0135 mm²</td>
<td>0.01 mm²</td>
<td>0.0094 mm²</td>
<td>0.009 mm²</td>
</tr>
<tr>
<td><strong>TRX Power Efficiency</strong></td>
<td>0.56 pJ/b</td>
<td>1.03 pJ/b</td>
<td>0.95 pJ/b</td>
<td>0.49 pJ/b</td>
<td>0.97 pJ/b</td>
</tr>
</tbody>
</table>

Summary

• Digital-intensive PAM-4 time-based DFE
• Differential voltage-to-time converter with enhanced linearity and dynamic range
• In-situ channel loss monitor