22.4 A 32Gb/s Digital-Intensive Single-Ended PAM-4 Transceiver for High-Speed Memory Interfaces Featuring a 2-Tap Time-Based Decision Feedback Equalizer and an In-Situ Channel-Loss Monitor

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Single-ended transceivers that can deliver high-data rates at reduced supply voltages are required to meet the ever-growing demands of future memory interfaces. The performance of conventional non-return-to-zero (NRZ) links is usually limited by inter-symbol-interference (ISI) noise caused by high channel losses. Alternative schemes such as duobinary [1], three or four level pulse amplitude modulation (PAM-3, PAM-4) [2], and multi-band signaling [3] were proposed to increase bandwidth efficiency. In particular, PAM-4 signaling utilizes four signal levels to send 2b per unit interval, at the expense of complex TX and RX circuits resulting in higher power consumption and larger chip area. While this approach has been gaining popularity for ultra-high speed (>50Gb/s) links, a more compact implementation is needed for memory interface applications. In this paper, we propose a digital-intensive PAM-4 receiver targeted at memory interfaces; time-based circuits are used for the decision feedback equalization (DFE). Unlike traditional current-mode logic, time-based circuits can be realized using inverters and programmable loads, making them ideally-suited for low-voltage energy-efficient memory interfaces.

Figure 22.4.1(left) shows the block diagram of the full transceiver system. The PAM-4 TX consists of a pseudo random bit sequence (PRBS) generator for testing purposes, a 3-tap half-rate feed forward equalizer (FFE) and parallel voltage-mode drivers. The PAM-4 RX includes a differential voltage-to-time converter (DVTC), a 2-tap time-based decision feedback equalizer (TB-DFE), a PAM-4 decoder and an on-chip bit error rate (BER) monitor. In-situ channel loss monitors were implemented on both the TX and RX sides. The detailed implementation of the 3-tap FFE and output combiner are shown in Fig. 22.4.1(right). The 8Gb/s bit stream is fed to the half-rate FFE for signal pre-emphasis.

Linearity and dynamic range are two important considerations in PAM-4 receiver designs because of the multi-level signal levels. In particular, accurate mapping of the four voltage levels to the corresponding time delays is a critical requirement for TB-DFE. Two main types of VTCs have been used in previous works [4]-[5]. [4] utilizes the clock-to-q delay of a voltage comparator biased in metastable condition. The offset voltage of the metastable voltage comparator is tuned by adjusting the source degeneration resistance. In [5], a current starved inverter stage is used where the pull-up delay is controlled by the input voltage. The VTC design in [4] is more complex than that in [5] but can achieve a higher voltage-to-time sensitivity. Both VTCs suffer from linearity issues. To achieve high sensitivity, good linearity, and robust operation, we propose the DVTC circuit in Fig. 22.4.2(upper, right) where the incoming analog voltage Vin is connected to the PMOS header of the upper inverter as well as the NMOS footer of the lower inverter. As illustrated in the timing diagram, RX_P delay and RX_N delay have opposite polarities due to the same V_{in} voltage controlling the pull-up and pull-down delays of the two paths. For instance, when the data is high, the RX_P delay increases while the RX_N delay decreases. This unique configuration expands the delay range from 42 to 70ps as shown in the simulation results in Fig. 22.4.2(bottom, right). Non-linearity in the two delay paths are cancelled out, enabling good linearity over the entire voltage range, from VSS to VDD.

Figure 22.4.3 shows the implementation of the fully time-based PAM-4 DFE along with the signal waveforms for each delay stage. Differential output signals RX_N and RX_P from the odd and even DVTCs are fed to the time-based DFE block. The delay difference between RX_N and RX_P contains the signal information. The four delay levels corresponding to voltage levels V_{00}, V_{01}, V_{10}, and V_{11} must be compared with three threshold delays $T_{REF,H}$, $T_{REF,M}$, and $T_{REF,L}$. This operation is performed by the three delay chain blocks denoted H, M, and L. Each block contains two separate delay paths for RX_N and RX_P signals, respectively. The first buffer stage performs the delay comparison while the second buffer stage performs the 2-tap DFE operation. The length of the delay chain was reduced by implementing the 6-bit DFE weights w1 and w2 in the upper and lower paths, respectively. To support half-rate operation, a total of 6 delay chain blocks with 12 delay paths and 6 phase detectors (PDs) are implemented in our design. A notable advantage of our proposed time-based implementation is the absence of any DAC circuits for generating reference voltages $V_{TH,H}$, $V_{TH,M}$, and $V_{TH,L}$. These analog voltages are required in conventional voltage-based PAM-4 designs to detect the different voltage levels. In our time-based implementation, simple programmable delay stages are used in lieu of DACs which significantly reduces the design complexity and circuit area. The timing waveforms in Fig. 22.4.3(bottom) show how the delay signals are manifested in each delay stage. Signals RX_N and RX_P have different relative delays depending on the four signal levels. These delays are compared with different reference delays in the first delay stage. ISI noise is cancelled out in the second delay stage and the delay polarity is sampled by a PD circuit. The results generated by the PD are decoded by a PAM-4 decoder and the BER is measured using an on-chip monitor circuit.

S-parameter is the de-facto measure of channel loss but its measurement requires an extensive test setup including a high frequency sinusoidal signal source. In this work, we designed an in-situ monitor that can indirectly measure the channel loss by sensing the signal swings of the TX and RX signals for a random bit sequence. The monitor circuit detects the TX and RX signal levels by comparing them with a known reference voltage $V_{REF.}$ By sweeping the V_{REF} and measuring the average toggling frequency of the comparator output using a divider circuit, we can extract the signal swing information without an extensive setup. Figure 22.4.4 shows how the signal swings are extracted from the measured frequency versus reference voltage data. We also introduce a channel loss parameter T_{21} which is basically the ratio between the TX and RX signal swings. The area and power consumption of the proposed channel loss monitor are negligible.

A PAM-4 test chip featuring the aforementioned techniques was implemented in a 65nm GP process. Figure 22.4.5(upper row) shows the data from the in-situ channel loss monitor. The average frequency of the TX and RX comparator outputs reach the same level at 1GHz due to the relatively small loss. As the frequency increases to 7GHz or higher, the RX comparator frequency saturates early due to the severe channel loss while the TX comparator frequency continues to rise. From the frequency versus voltage plot, we calculated the loss parameter defined in Fig. 22.4.4 and compared the results with S-parameter values obtained from electromagnetic simulations. The small discrepancy can be attributed to the non-sinusoidal random bit stream used for the channel characterization. Error rate of the PAM-4 link was measured using an on-chip BER monitor. The bathtub curves in Fig. 22.4.5 (lower left) shows TB-DFE enabling an operating window with a BER less than 10^{-12}. A time-domain BER eye-diagram is shown in Fig. 22.4.5 (lower right) down to BER rates of $<10^{-9}$. Figure 22.4.6 compares the proposed transceiver with relevant previous works. The proposed design has a competitive performance while offering the unique benefits of a time-based design. Figure 22.4.7 shows the die photo and feature summary of the 65nm chip. When operating at a data rate of 32Gb/s, the PAM-4 transceiver achieves an energy-efficiency of 0.97pJ/b. The circuit area of the TX and RX blocks are 31×72 μm^2 and 89×73 μm^2, respectively.

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[3] W. Cho et al., "A 38mW 40Gb/s 4-Lane Tri-Band PAM-4 / 16-QAM Transceiver in 28nm CMOS for High-Speed Memory Interface," *ISSCC*, pp. 184-185, Feb. 2016.
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[5] P. Chiu et al., "A 65-nm 10-Gb/s 10-mm On-Chip Serial Link Featuring a Digital-Intensive Time-Based Decision Feedback Equalizer," *JSSC,* vol. 53, no. 4, pp. 1203-1213, April 2018.

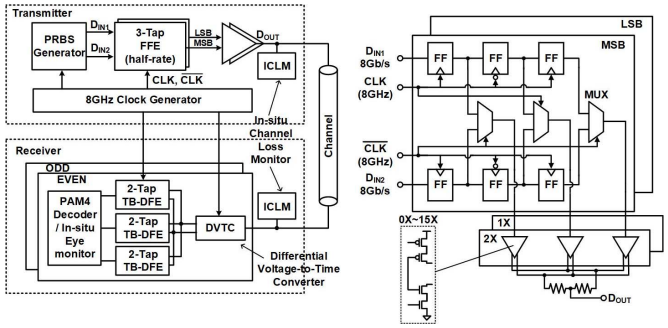


Figure 22.4.1: (Left) Block diagram of the proposed PAM-4 transceiver. (Right) Implementation of 3-tap FFE and voltage mode driver.

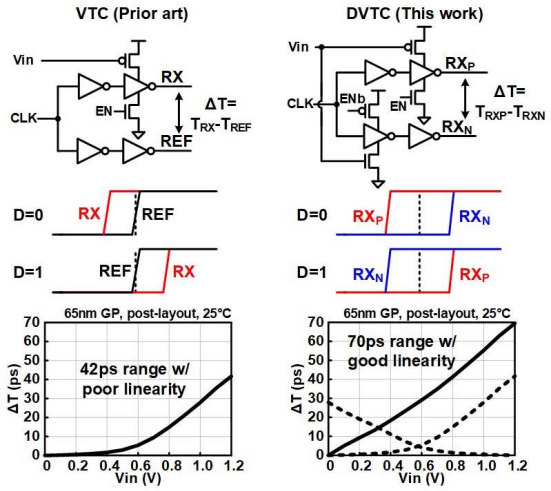


Figure 22.4.2: Schematic, operating principle and timing diagram of the inverter-based VTC [5] and proposed DVTC. Post-layout simulation result show that the linearity and dynamic range are significantly improved.

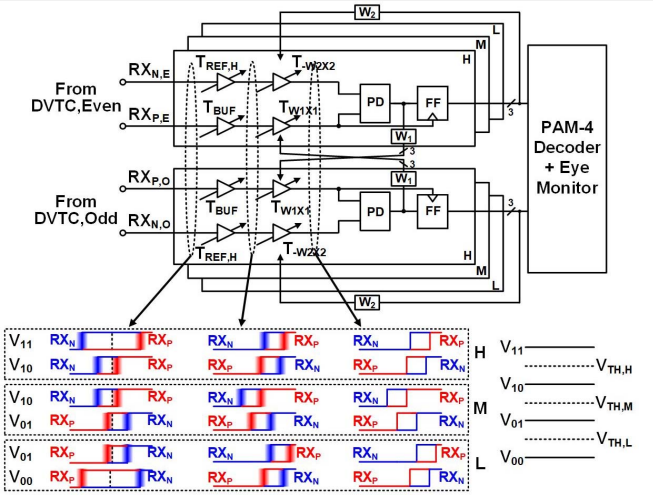


Figure 22.4.3: Block diagram of proposed time-based PAM-4 DFE. The timing diagram illustrates how the delay difference is manifested after each delay stage pair for the four PAM-4 signal levels.

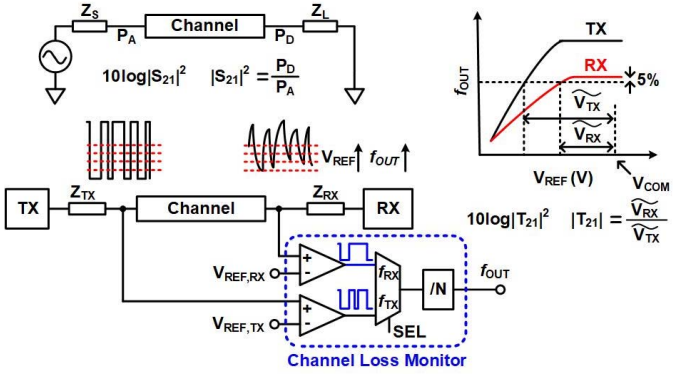


Figure 22.4.4: Proposed in-situ channel loss monitor and methodology for extracting channel loss parameter from the monitor output.

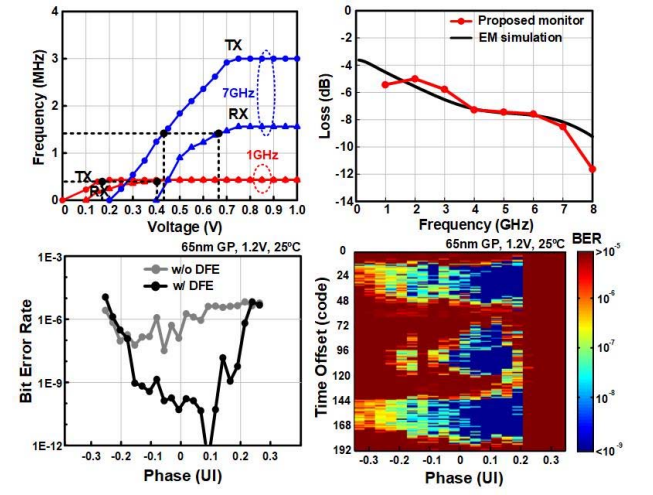
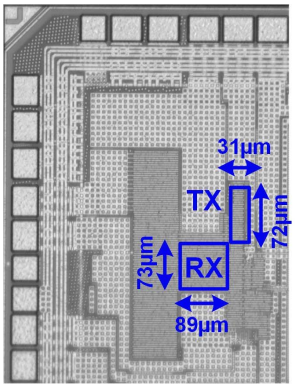


Figure 22.4.5: (Upper) Channel loss monitor data and reconstructed channel characteristics. (Lower) Bathtub curves with and without DFE for BER<10^{-12}, and time-domain BER eye-diagram.

	JSSC'14 [1]	ISSCC'19 [2]	ISSCC'16 [3]	JSSC'18 [4]	This work
Signaling	Duobinary	PAM-3	Muti-Band	NRZ	PAM-4
Single/Differential	Single-Ended	Single-Ended	Differential	Single-Ended	Single-Ended
RX Circuit Type	Voltage-Based	Voltage-Based	Voltage-Based	Time-Based	Time-Based
RX Equalization	1-Tap DFE	1-Tap DFE	Self-Equalization	2-Tap DFE	2-Tap DFE
Data Rate	7 Gb/s	27 Gb/s	10 Gb/s	12.5 Gb/s	32 Gb/s
Technology	65nm	28nm	28nm	65nm	65nm
Voltage	1.05V	0.6V	1.2V	0.8V	1.2V
Channel Loss	0.8dB@3.5GHz	20mm	6dB@6GHz	14dB@6.25GHz	11.6dB@8GHz
BER	<10E-12	<10E-12	<10E-12	<10E-12	<10E-12
TRX Area	0.0333 mm^2	0.0135 mm^2	0.01 mm^2	0.0094 mm^2	0.009 mm^2
TRX Power Efficiency	0.56 pJ/b	1.03 pJ/b	0.95 pJ/b	0.49 pJ/b	0.97 pJ/b

Figure 22.4.6: Performance comparison with previous work.



Technology	65nm CMOS
Circuit Area	TX: 31x72µm^2
	RX: 89x73µm^2
VDD	1.2V
Data Rate	32 Gb/s
Channel Loss	11.6dB@8GHz
BER	<10^{-12}
Power Efficiency	0.97 pJ/b

Figure 22.4.7: Chip microphotograph and feature summary.

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