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[Invited] Characterization and Mitigation of EM Effects in Advanced Nodes

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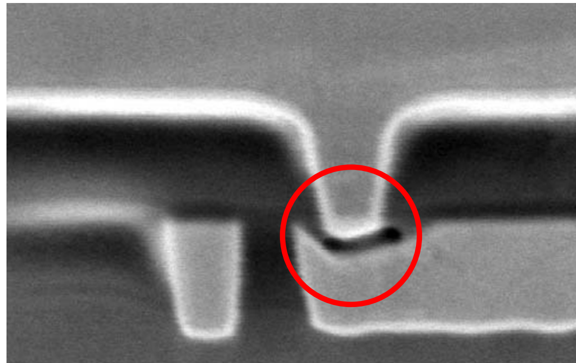
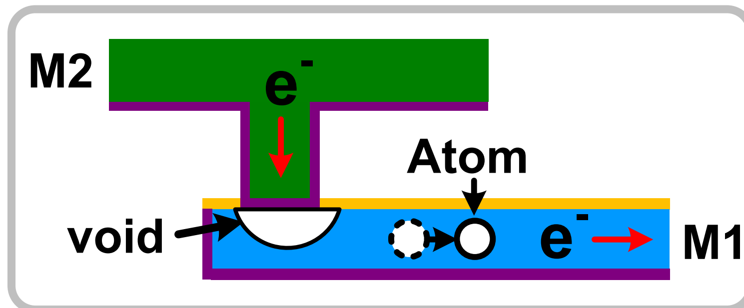
[1]Now with Maxim Integrated, [2]Now with Intel

Collaborators: Cisco, TSMC, Mentor Graphics, and Intel

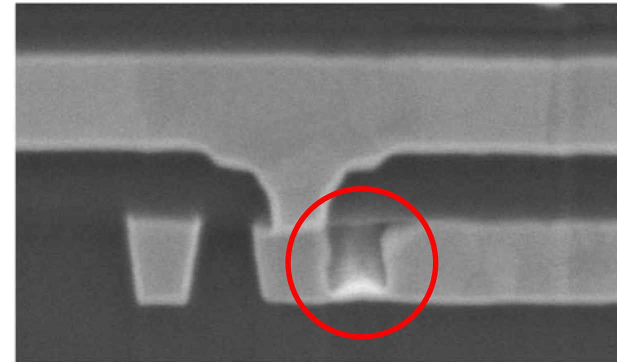
Electromigration In Interconnects

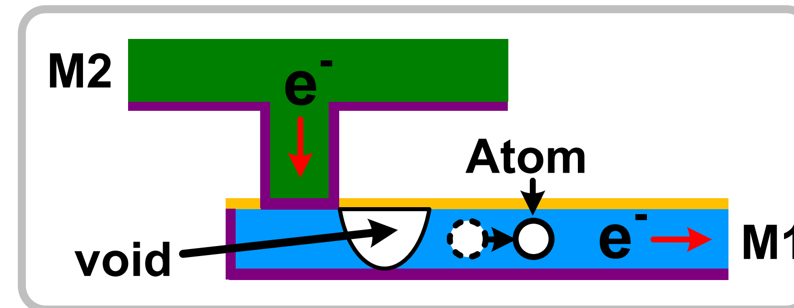
Abrupt failure





Progressive failure

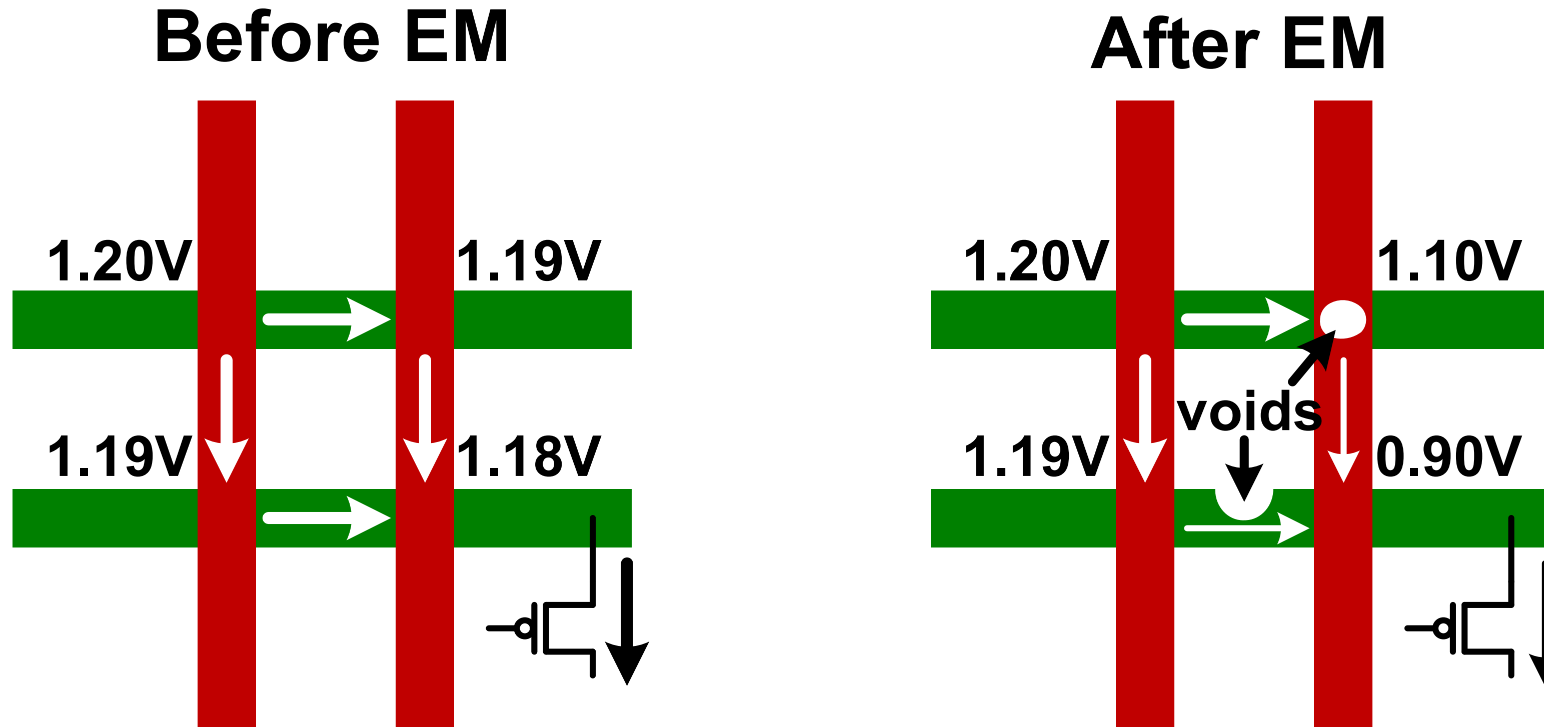




A.S. Oates, et al., TDMR, 2009

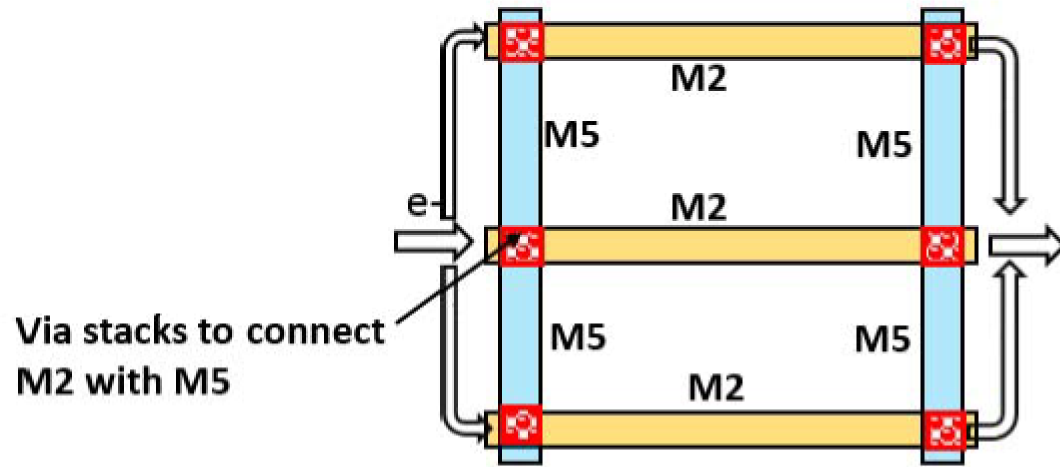
- EM depends on current density, temperature, and mechanical stress
- Impact: IR drop in power grids, increased delay in signal wires

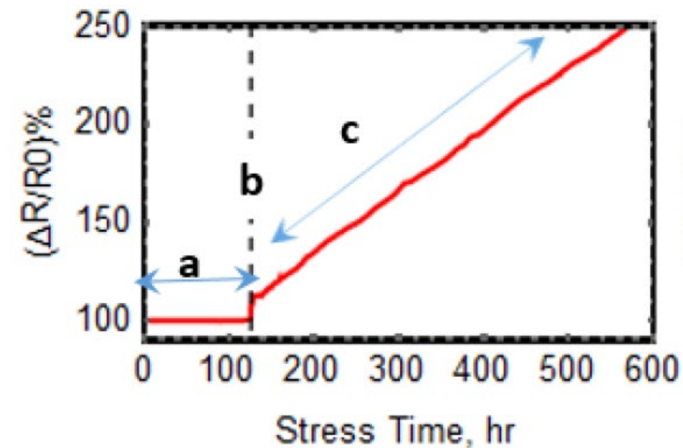
Power Grid EM Characterization Challenges



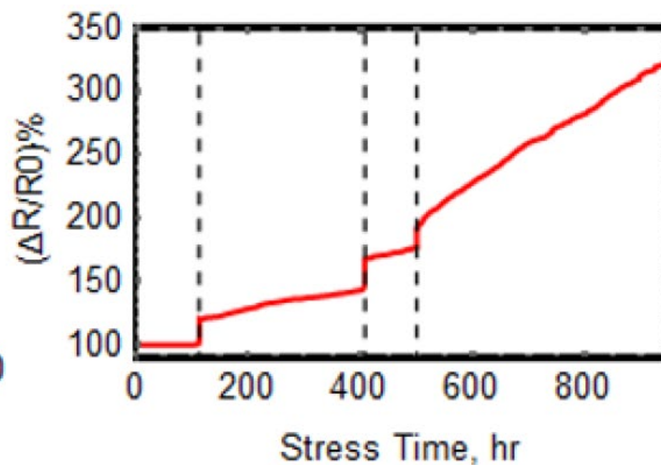
- High stress temperature (>300˚C) → active load will be damaged
- Large amount of data required for statistical analysis → long test time
- Too many sample points → large # of IO pads

Prior Art: Power Grid EM Test Structure





a) Single link EM structure

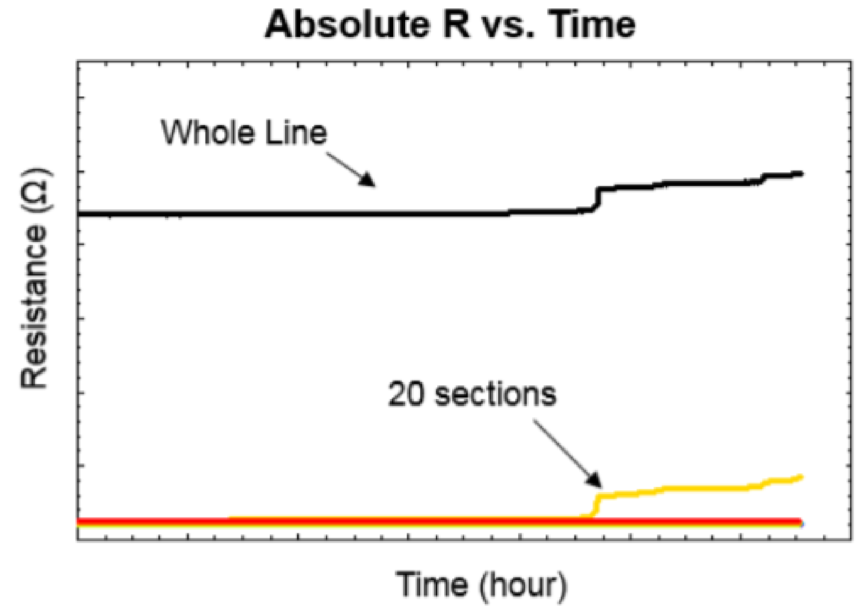


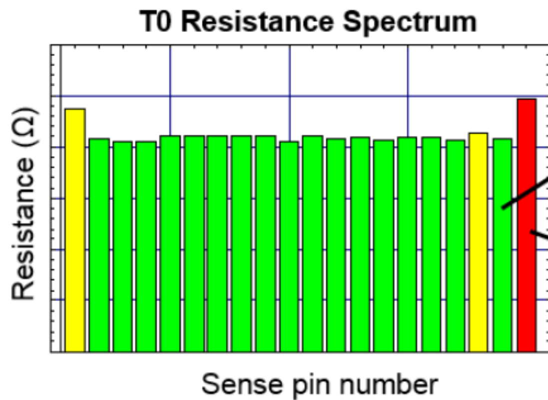
b) Power grid like EM structure (Type II)

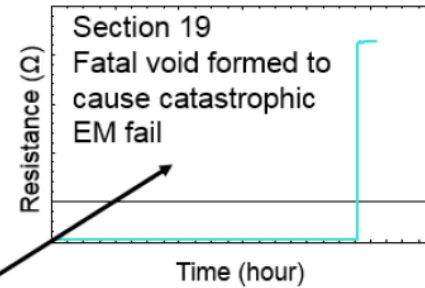
B. Li, IRPS 2018 (IBM)

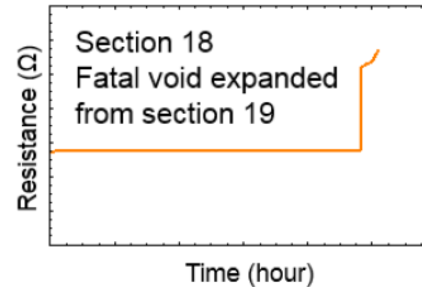
- Total resistance of 3x2 50µm long test structure stressed at 325ºC with constant current
- Key observations: Faster failure compared to single-link, multiple resistance jumps, different growth rates

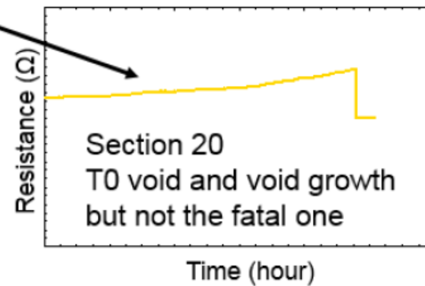
Prior Art: Voltage Tapping Technique

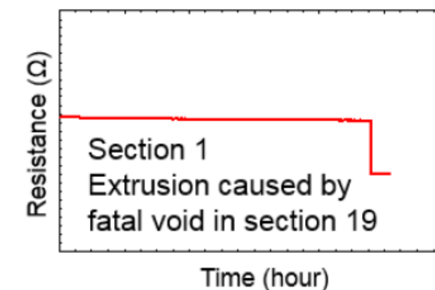








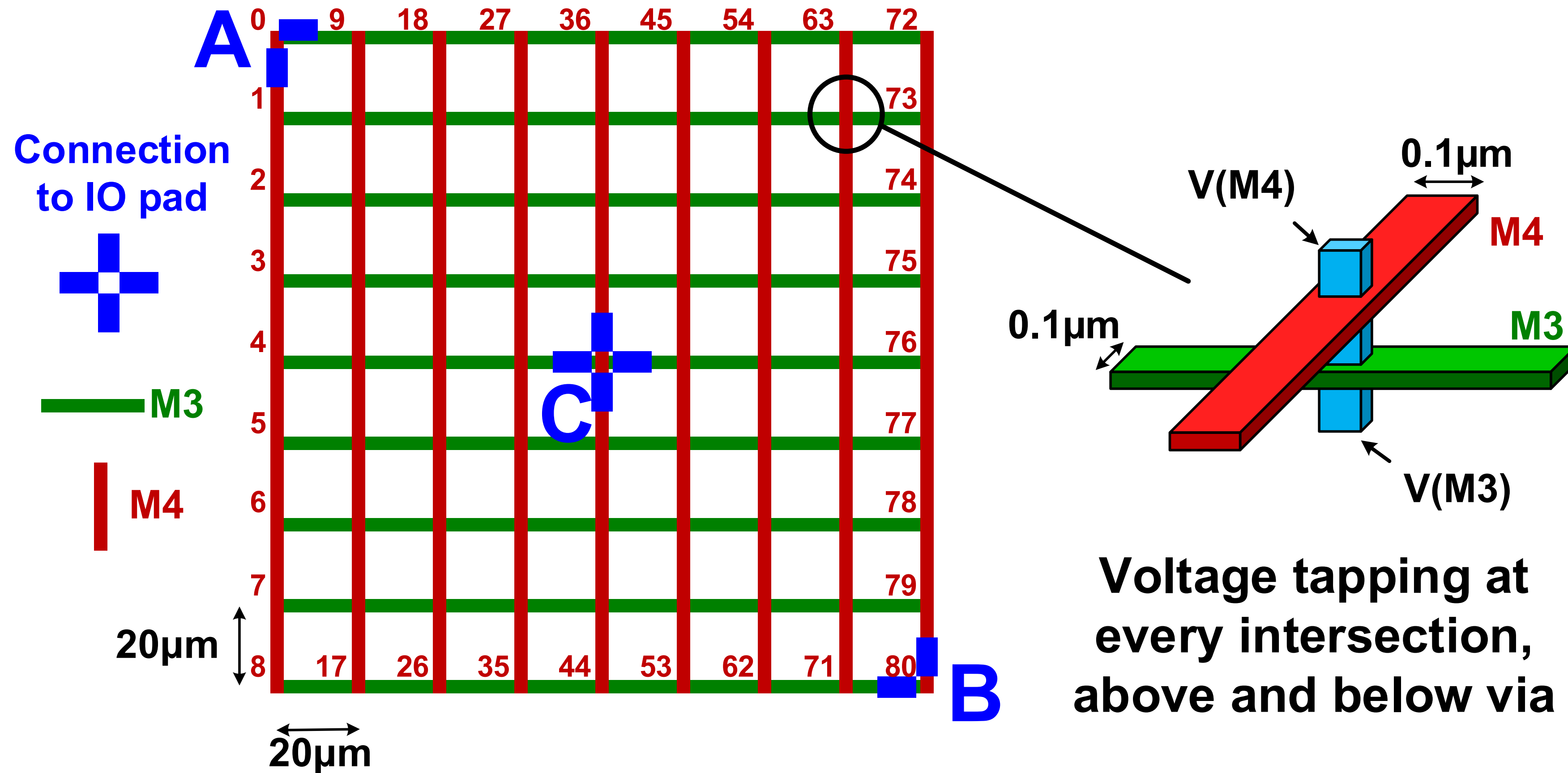




- Effect of individual voids or extrusions can be measured accurately

F. Chen, IRPS 2015 (IBM)

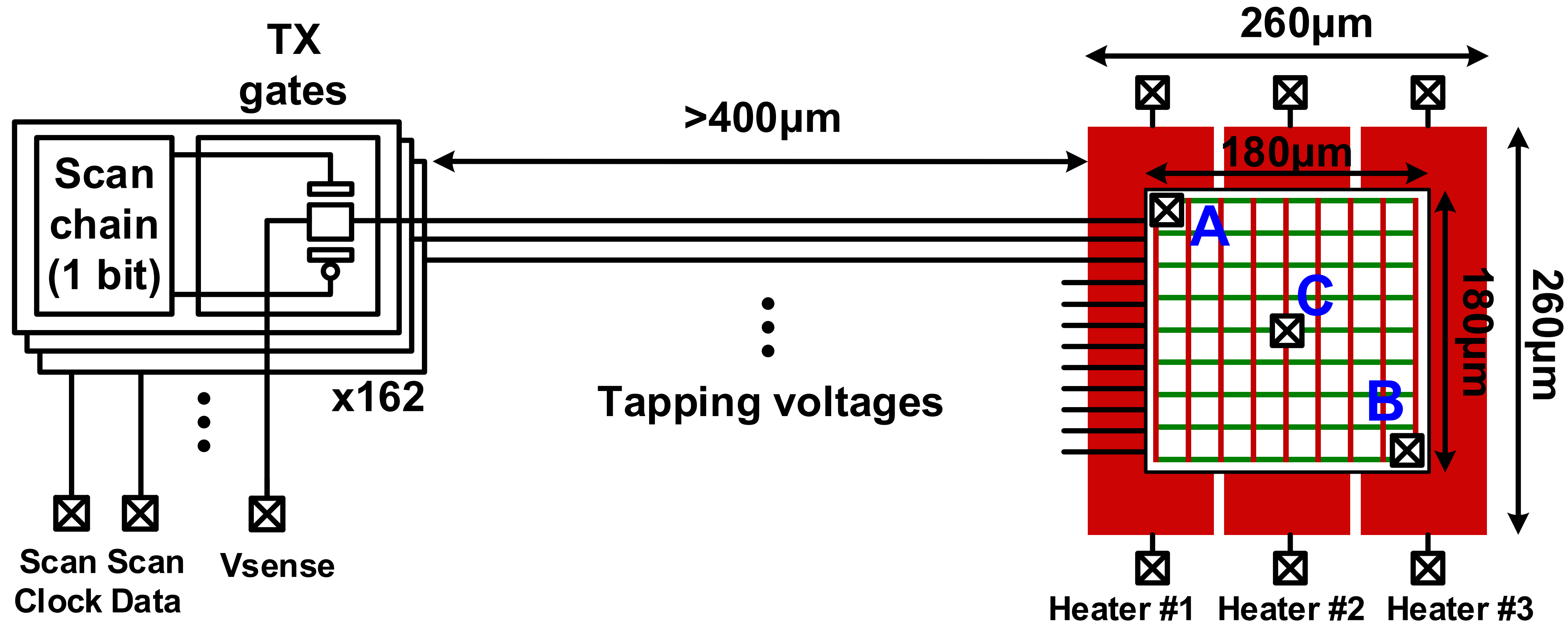
Our Work: 9x9 Power Grid EM Test Structure



- M4-M3 “pseudo” power grid with three pad connections(A,B,C)
- Voltage tapping through top and bottom vias
- Strong connection to IO pads using multiple vias and wide wires

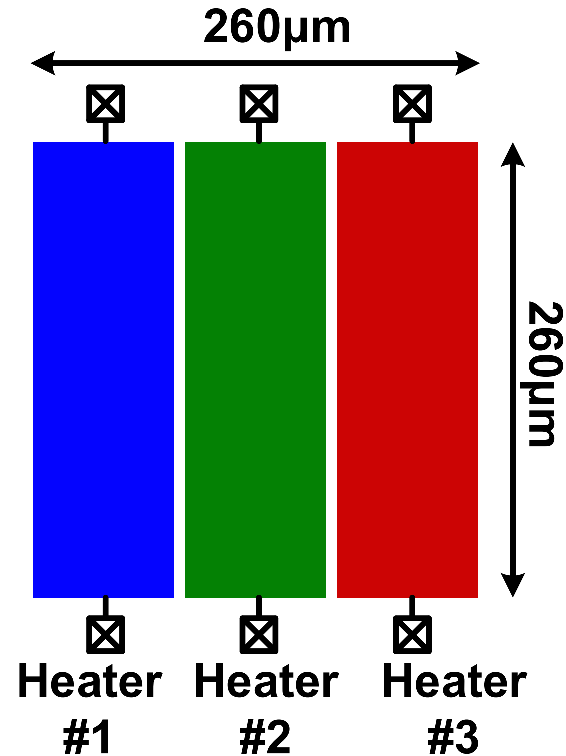
C. Zhou, C. Kim, VLSI Technology Symposium 2018, TDMR 2020

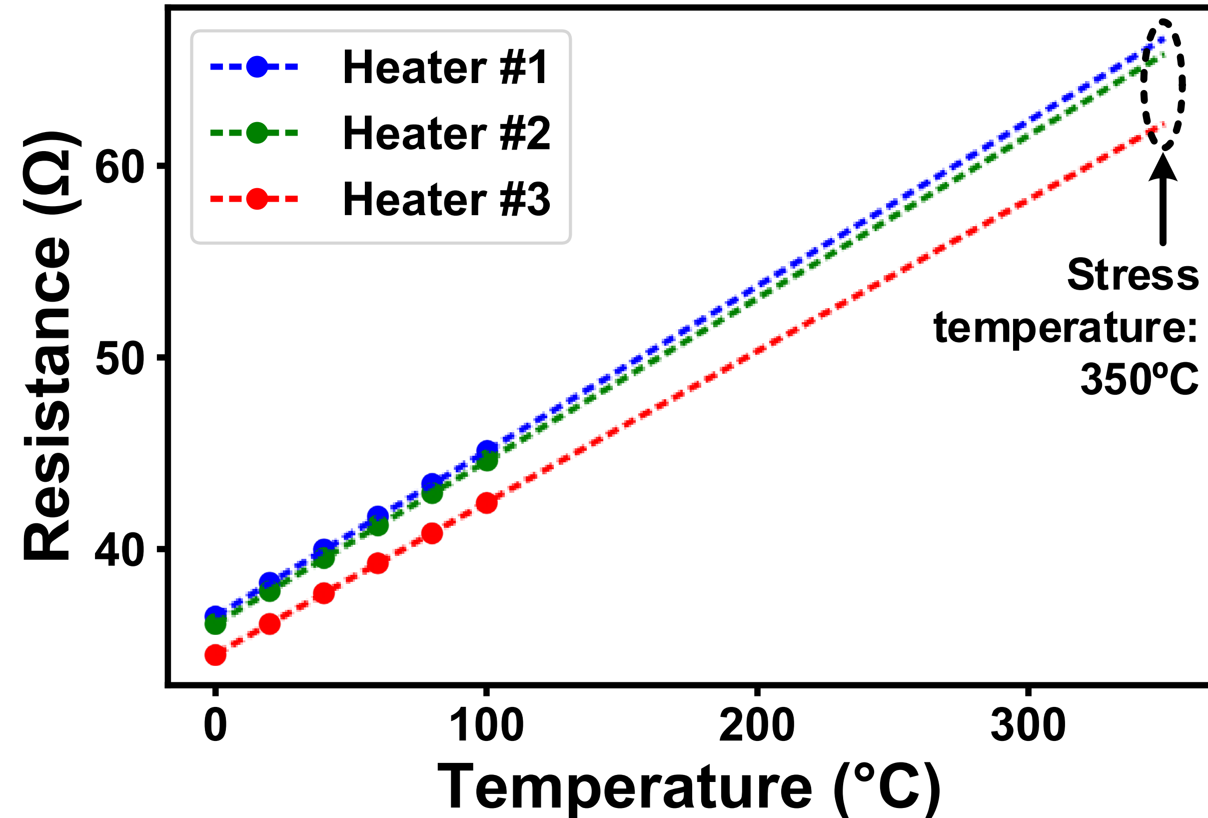
65nm EM Test Chip Diagram



- IO device based transmission gates used for voltage monitoring
- Circuits >400µm away from heaters to protect from high temp.

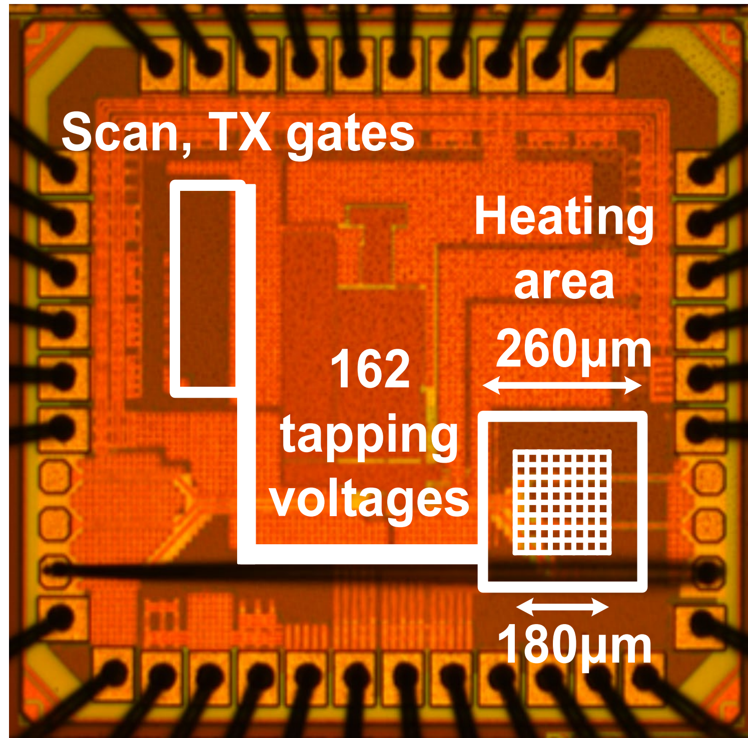
On-chip Heater Temperature Coefficient of Resistance (TCR)

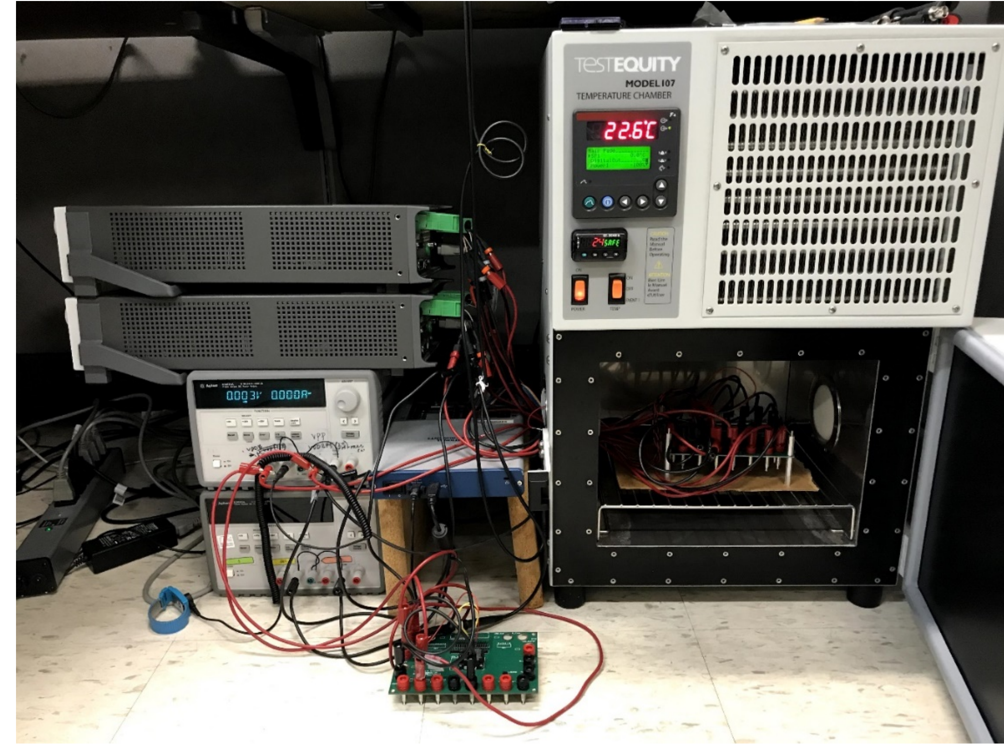




- Poly resistor based on-chip heaters enables (1) fast and accurate temperature control and (2) on-chip control circuits
- Three heater stripes for individual temperature control
- Excellent linearity thanks to four terminal Kelvin measurements

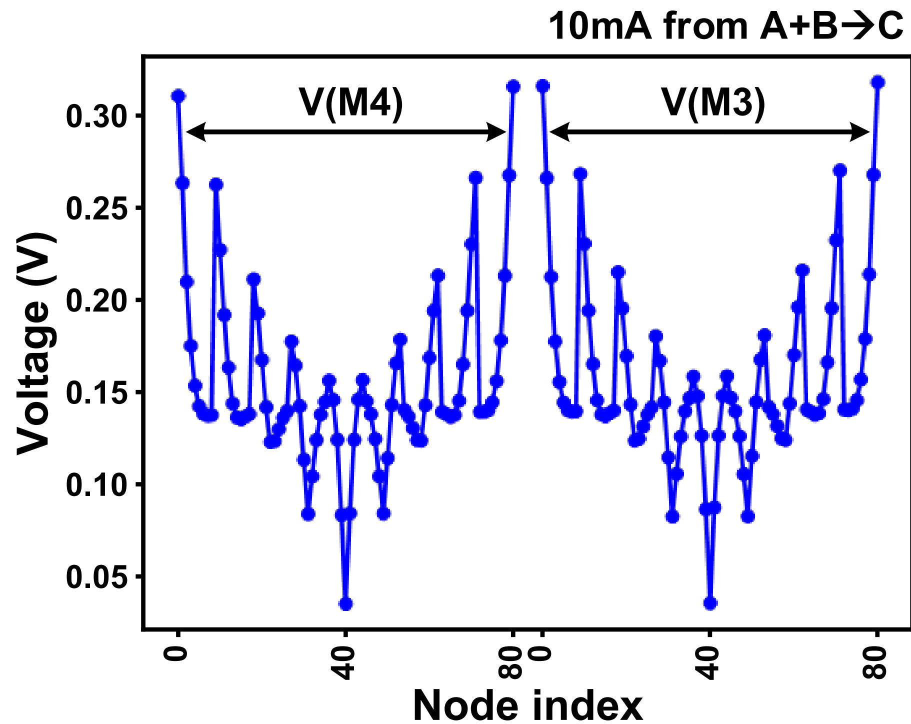
Die Photo and Test Setup

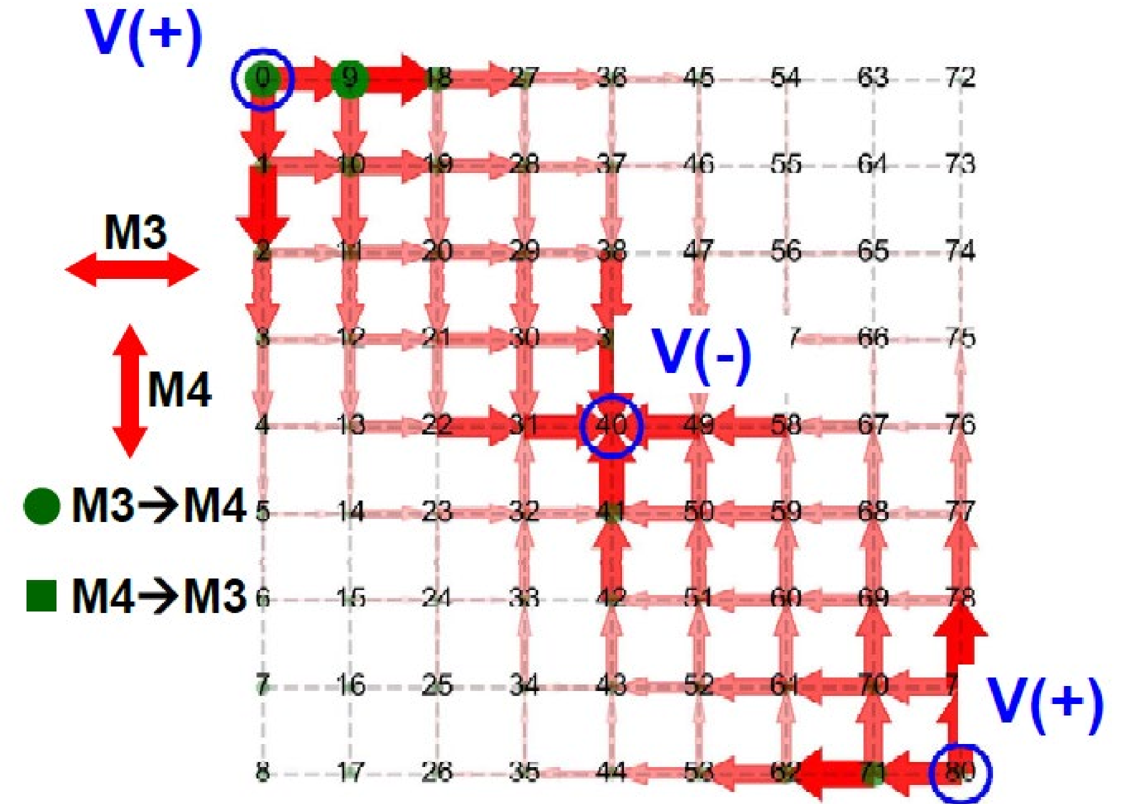




- Temperature control setup
  - Measure heater temperature coefficient of resistance (TCR) before EM test
  - Ambient temperature set to 0 °C to keep control circuits cool during test

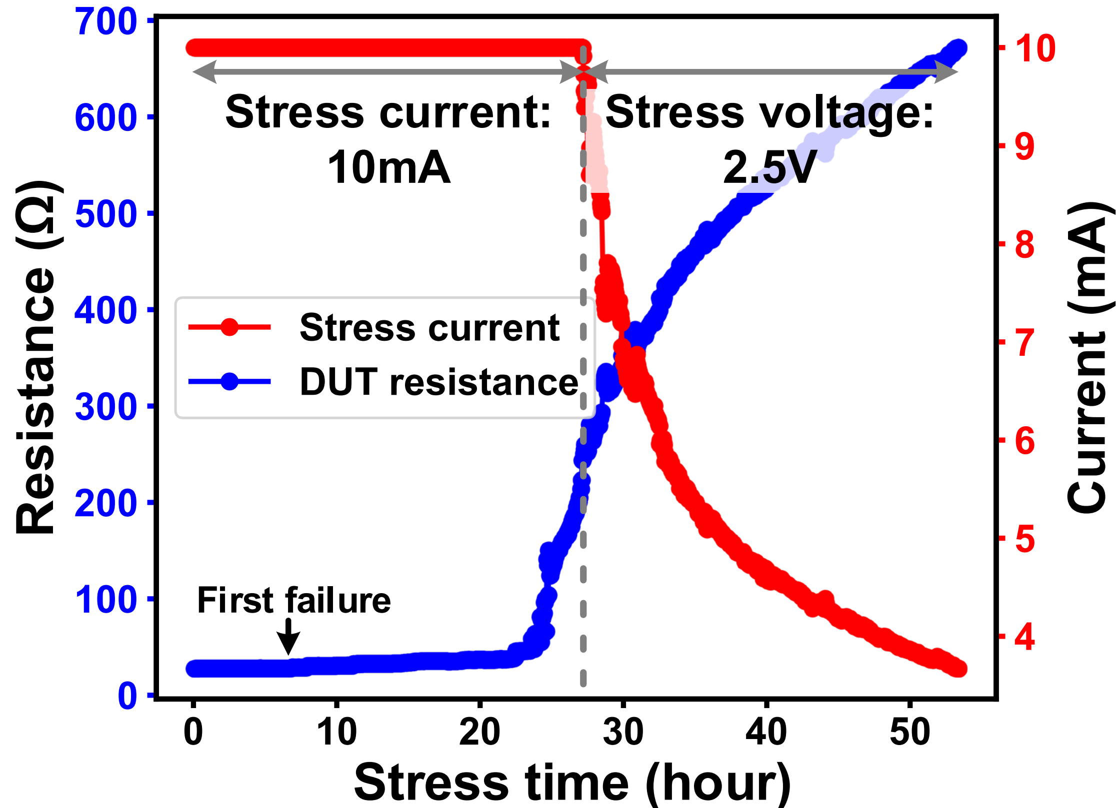
Voltage Drop Map of Fresh Chip

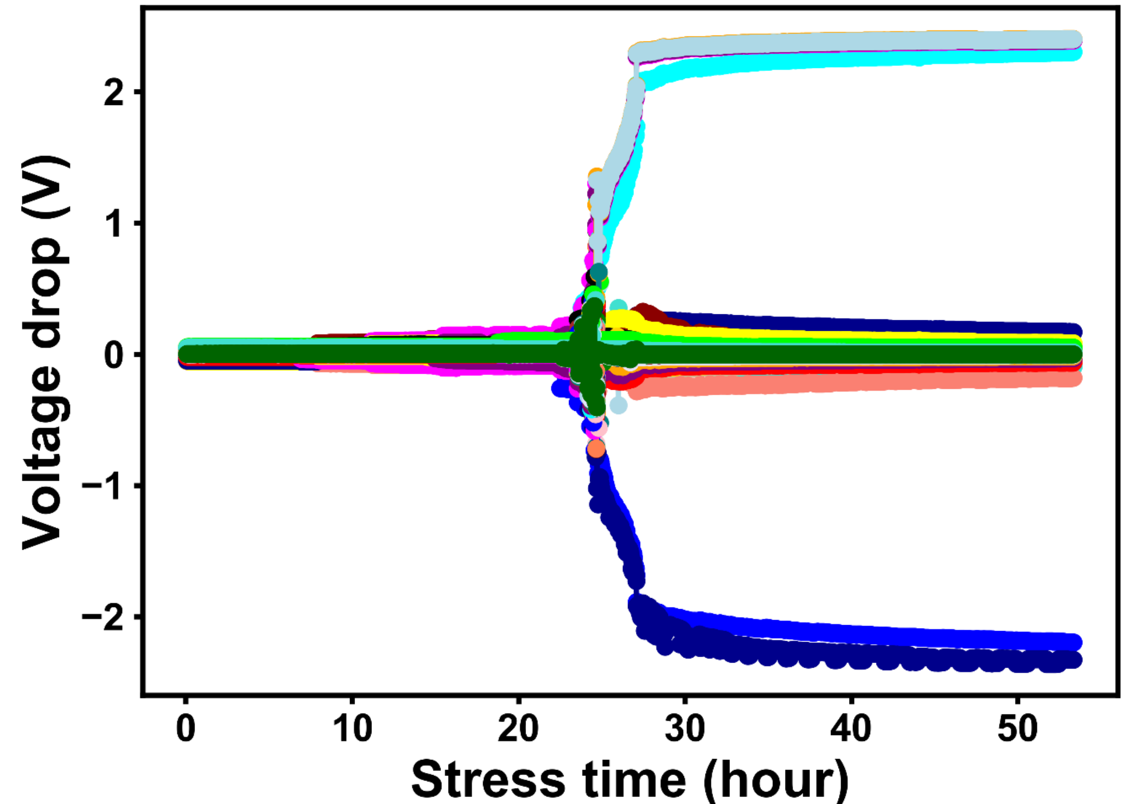




- 162 node voltage samples → voltage drop across entire power grid
- For a fresh grid, the size of the arrow and marker represents the current density (with the exception of nodes near V(+) and V(-))
- Current density highest near IO pad connection points A, B, C

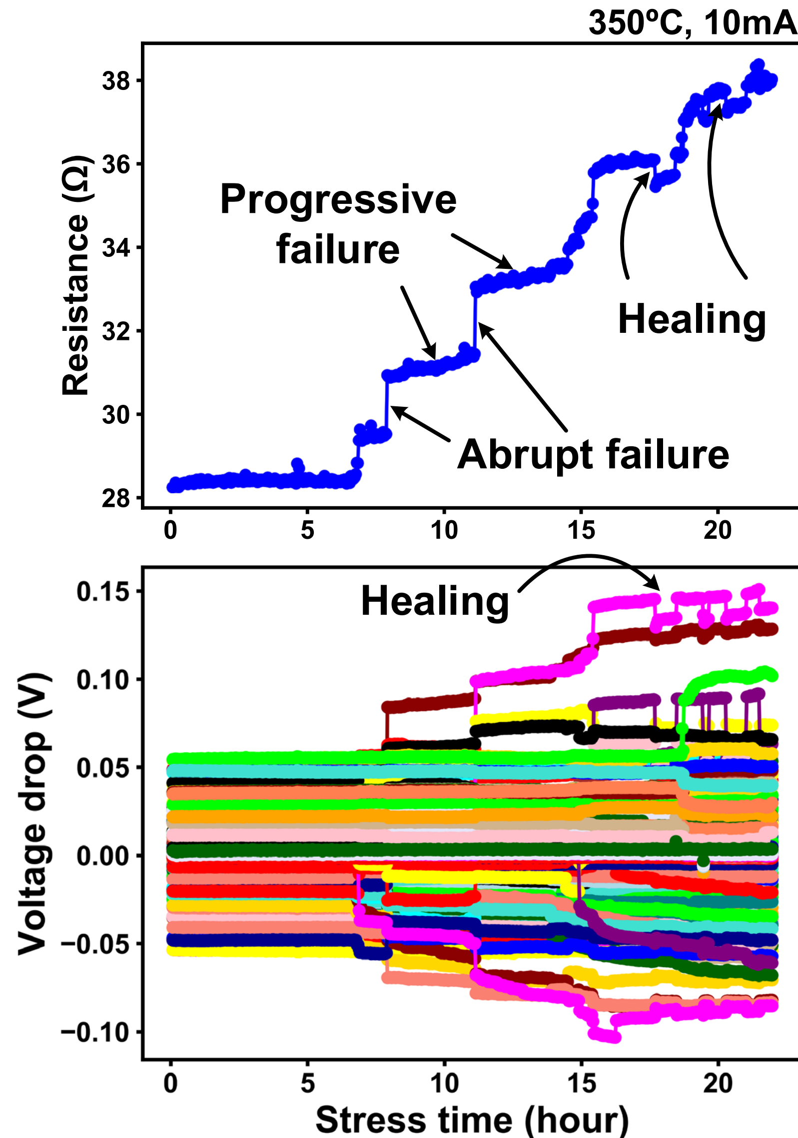
Total Power Grid Resistance and Voltage Drop Traces





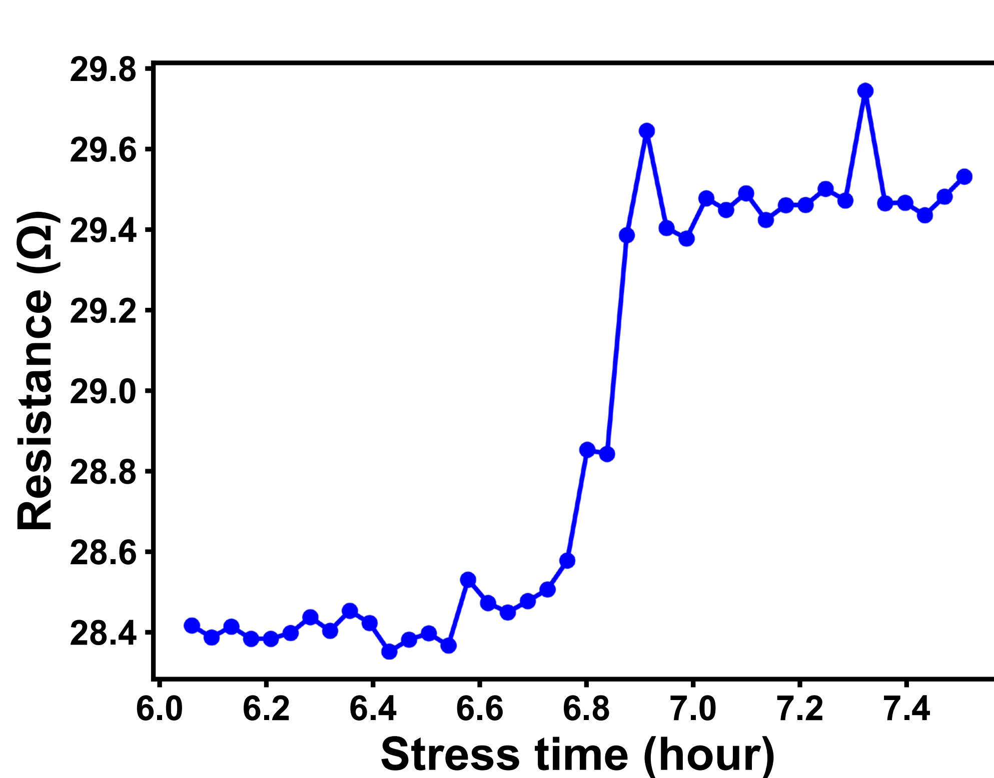
- Stress mode: constant current mode → constant voltage mode
- Due to voltage compliance limit of source meter

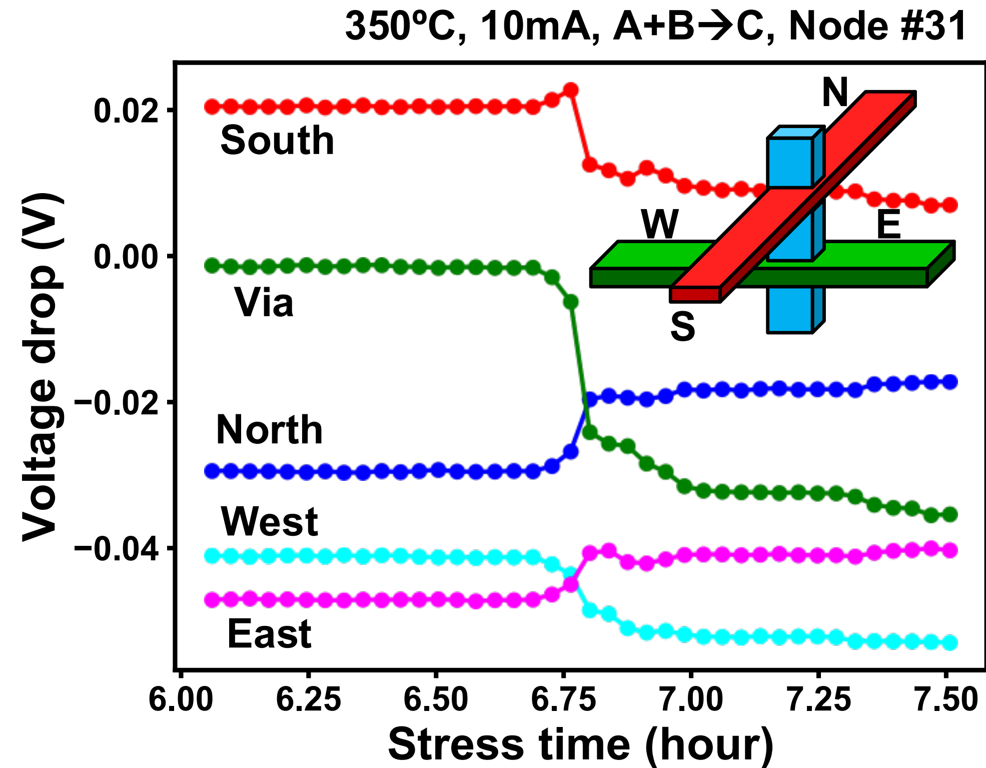
Failure Modes and Healing

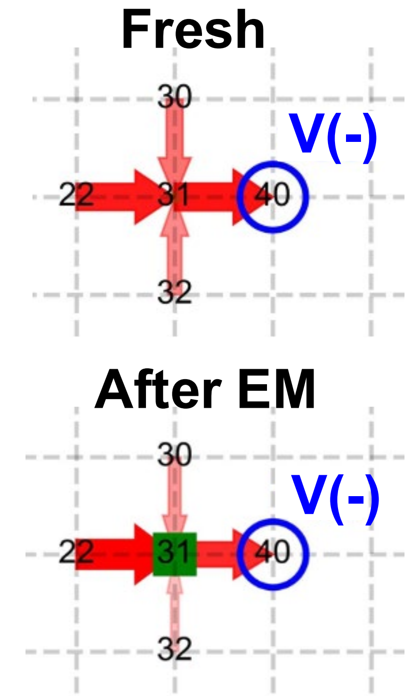


- Both abrupt and progressive failures observed
- Temporary healing observed
  - Electrical stress (forward)
  - Mechanical stress (backward)
- Voltage jumps are due to either EM in the wire itself (large jumps) or increased current due to EM in neighboring wires/vias (small jumps)

EM Failure Location Analysis

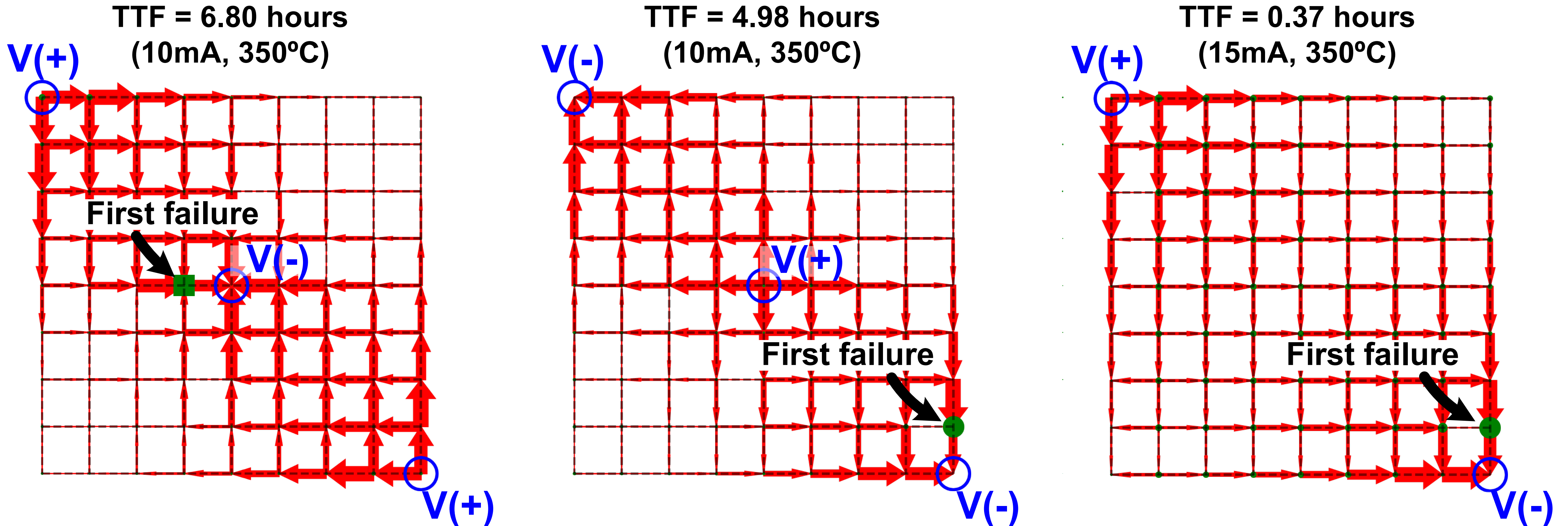






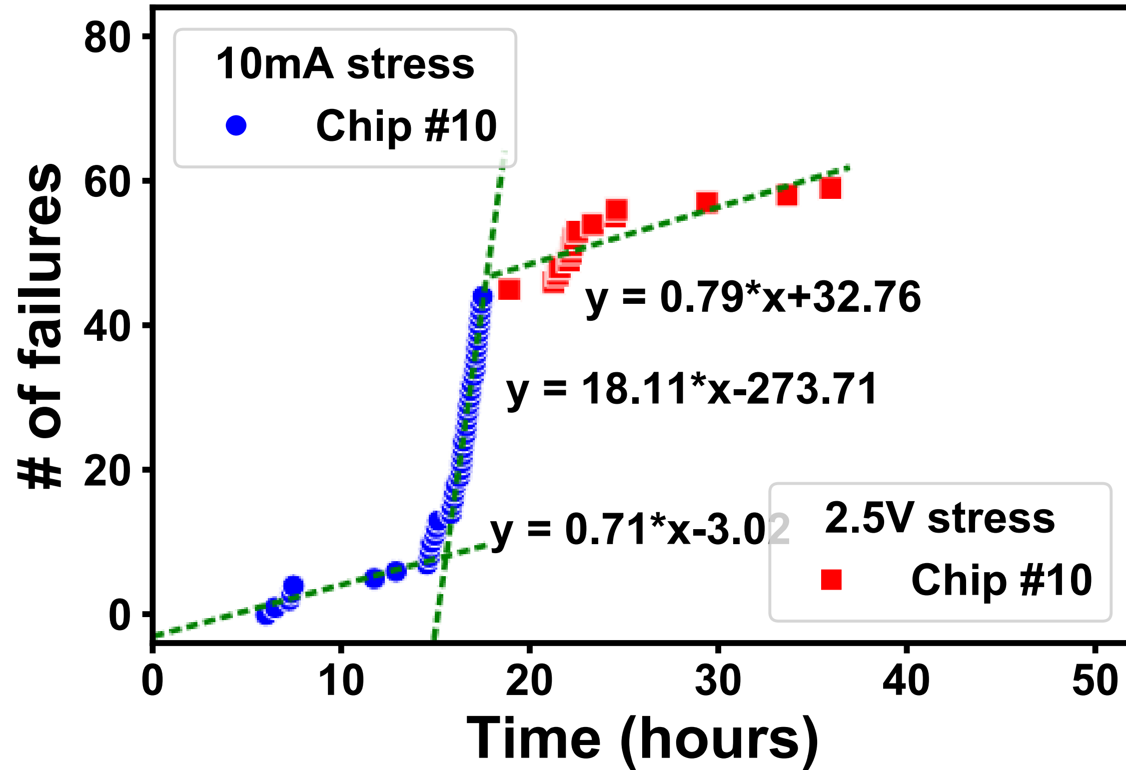
- Branch with largest voltage shift likely to be failure location
- Resistance shift not instantaneous (i.e. gradually changes over several minutes → longer timescale under nominal condition)

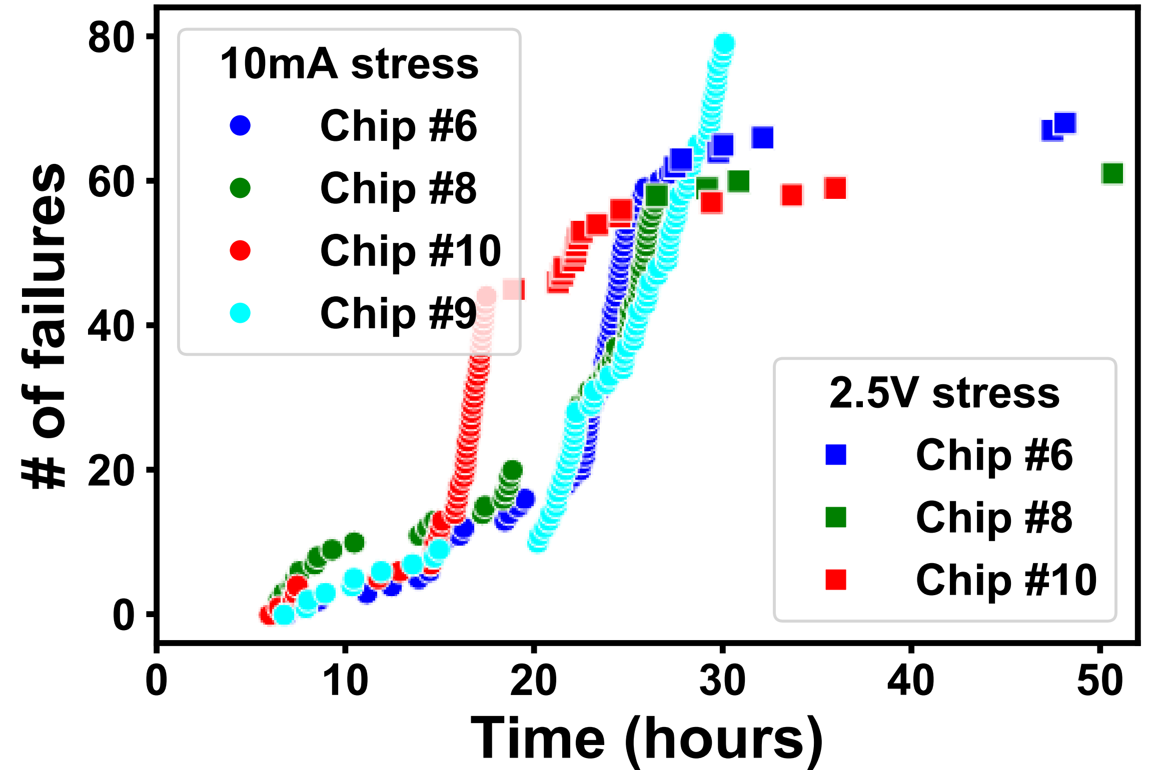
First EM Failure Location



- Three current stress modes applied to multiple chips
- First failure located near negative voltage terminal due to EM tensile stress

EM Failure Rates



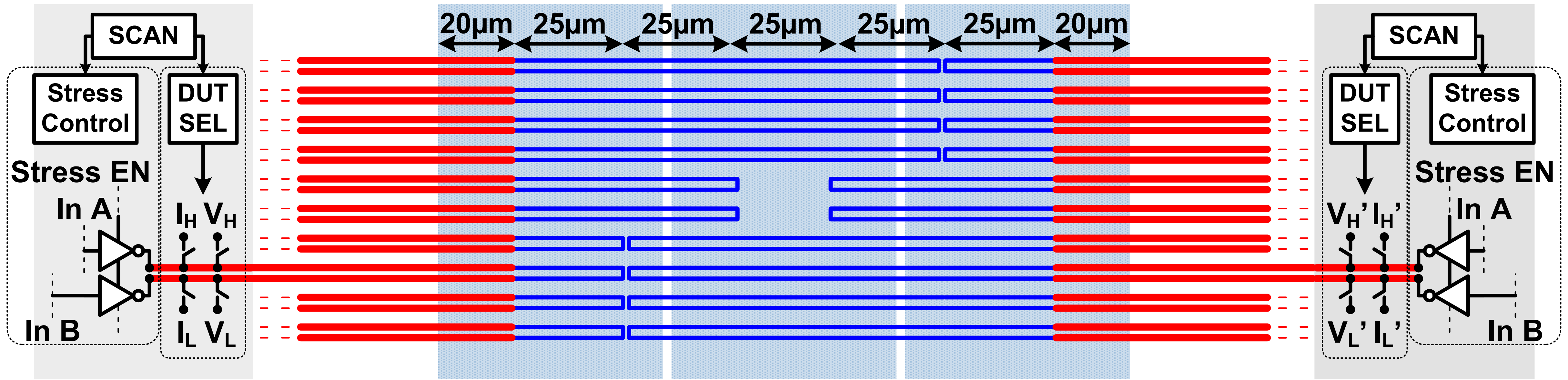


- Constant current stress: failure rate increased rapidly due to increasing current density in alternative paths
- Constant voltage stress: failure rate decreases due to decreasing total current

Part 1 Summary

- Voltage tapping technique used to track EM induced voltage drop inside a “pseudo” 9x9 power grid
- Early failures occur near the negative voltage terminal
- Failure rate rapidly increases after the first few failures due to higher current density in alternative paths
- Healing was easily observed which may be due to redundant current paths of power grid
- Data useful for calibrating EM models and prediction tools

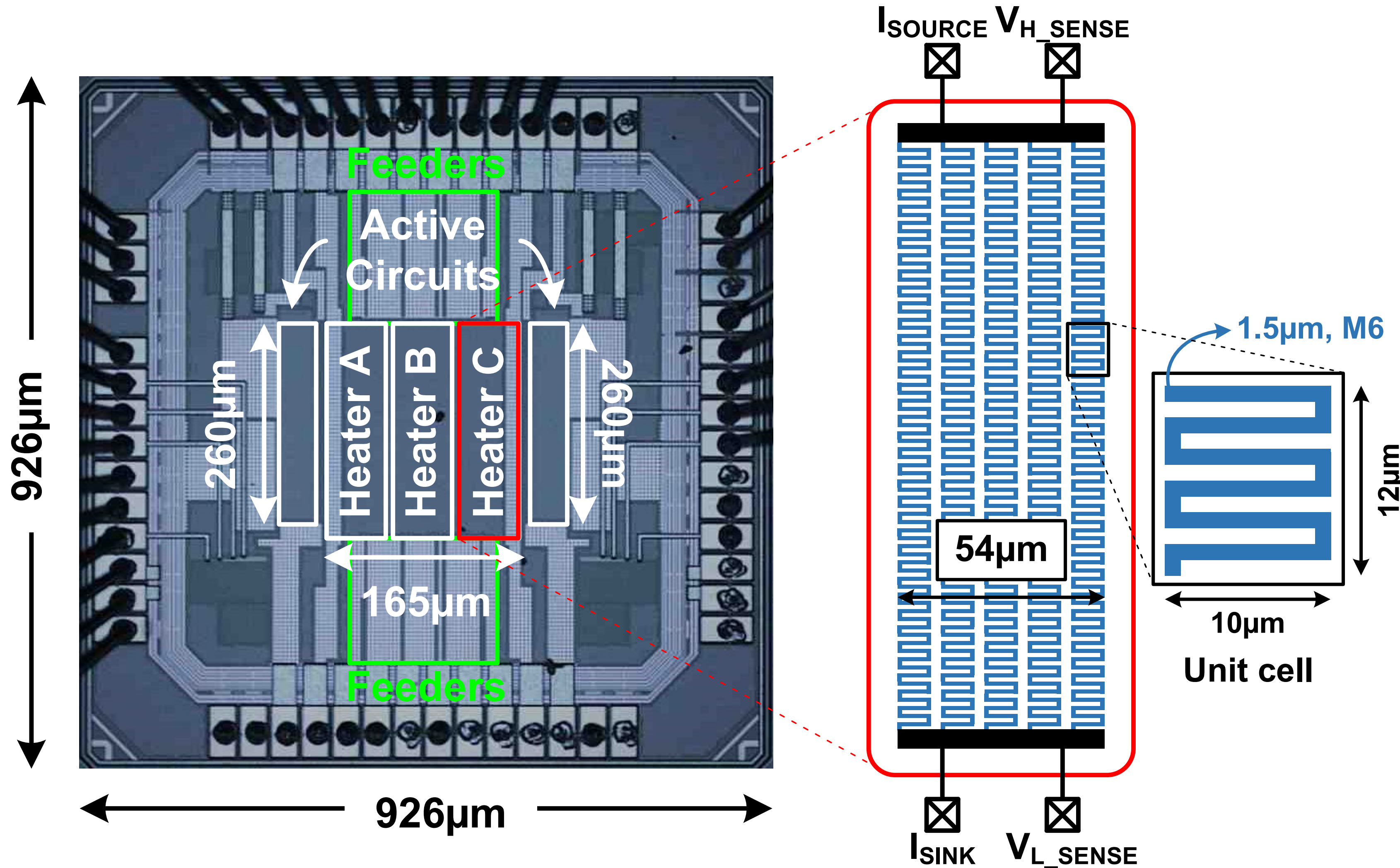
16nm Test Vehicle For EM Characterization



- Wide feeders to minimize IR drop
- Folded to maximize area utilization
- Parallel stress capability
- 4 terminal Kelvin sensing
- IO device switches to minimize leakage

N. Pande, et al., IEDM 2019

16nm Die Photo and On-Chip Heater Design

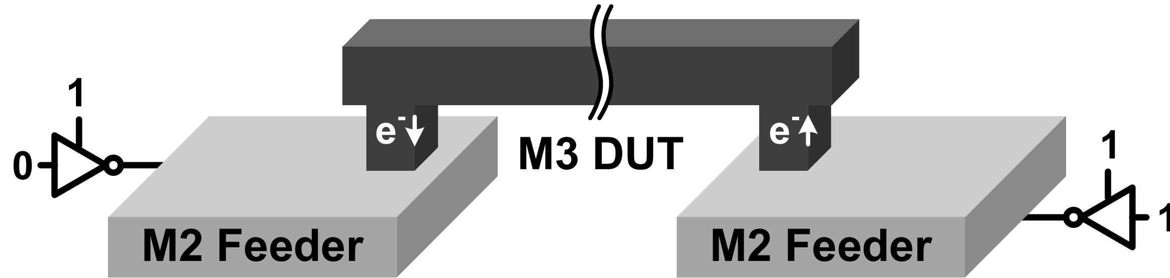


- Snake shaped metal heaters
- 4-wire sensing to accurately track temperature in heating area

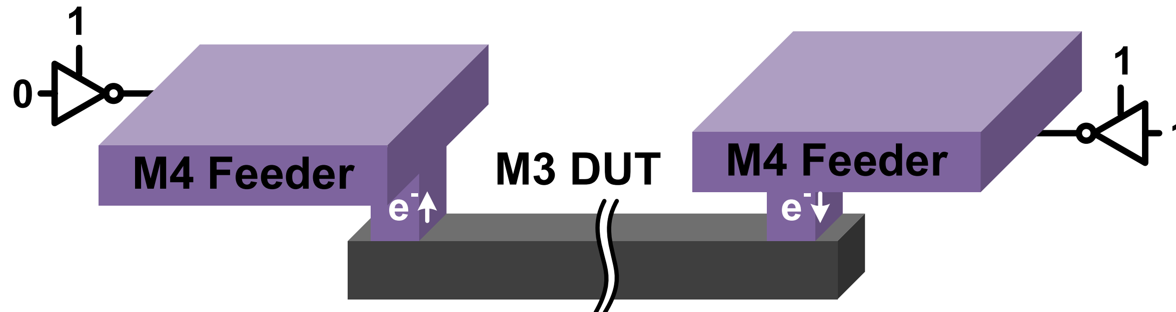
N. Pande, et al., IEDM 2019

Test Structures

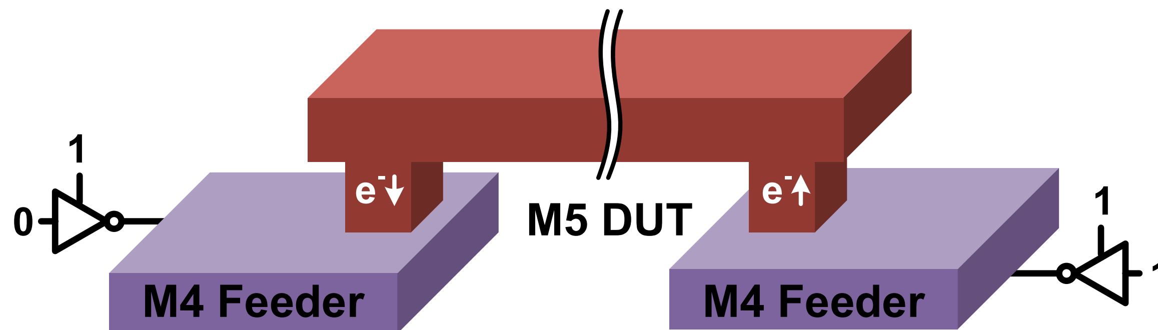
Feeder length = 70µm in all cases



M3 DUT + M2 Feeder
- 50µm, 100µm, 200µm

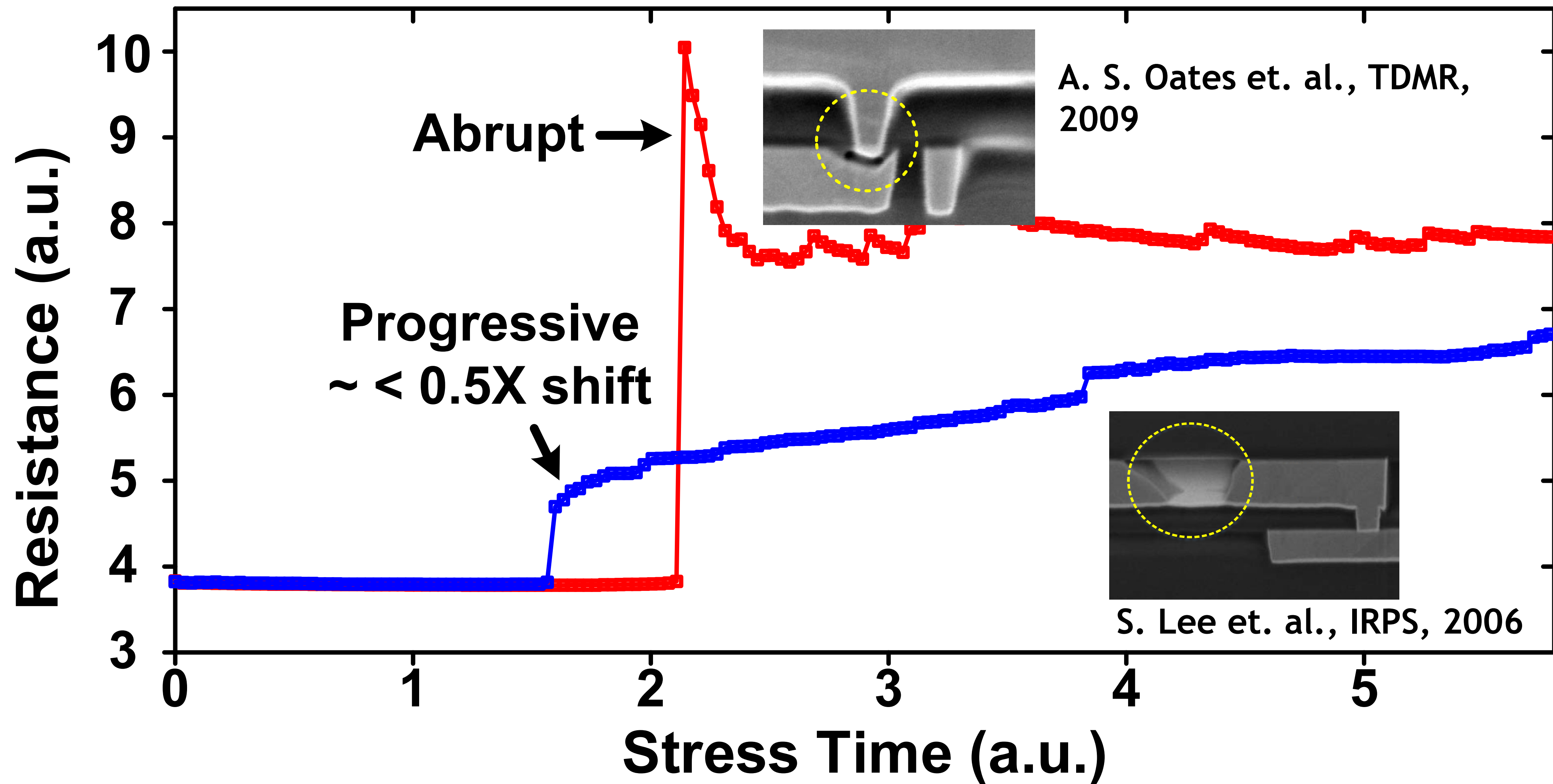


M3 DUT + M4 Feeder
- 50µm, 100µm, 200µm

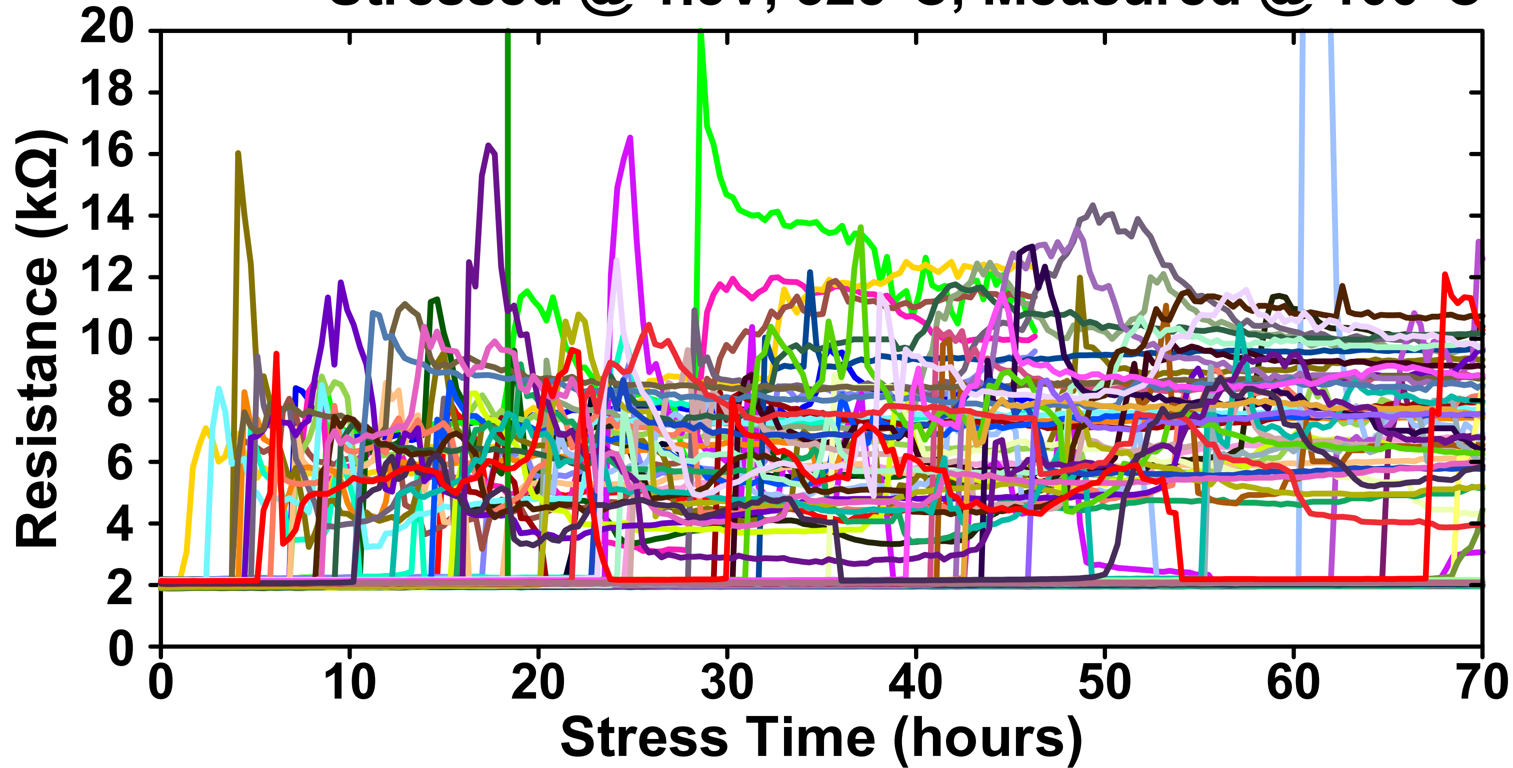


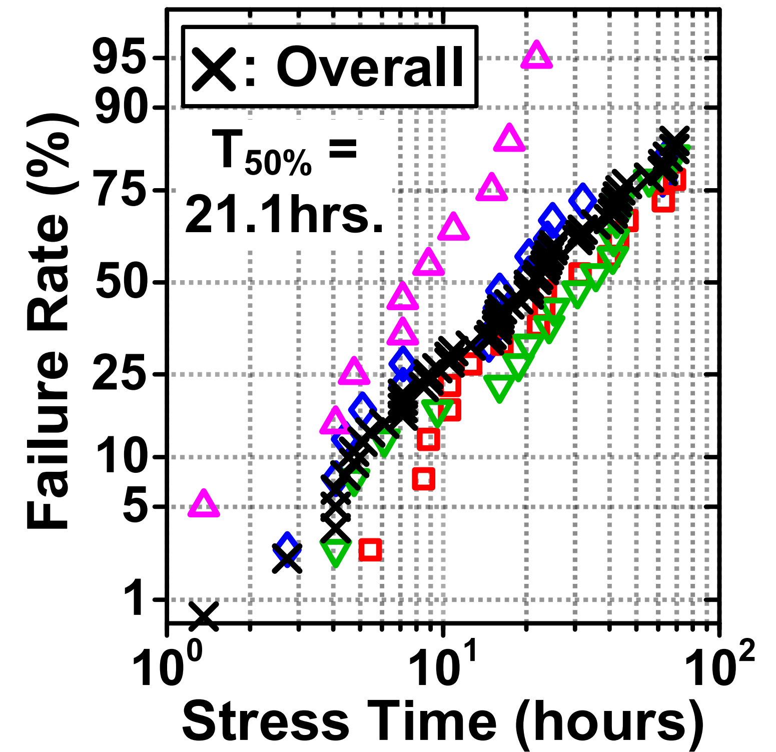
M5 DUT + M4 Feeder
- 50µm, 100µm, 200µm

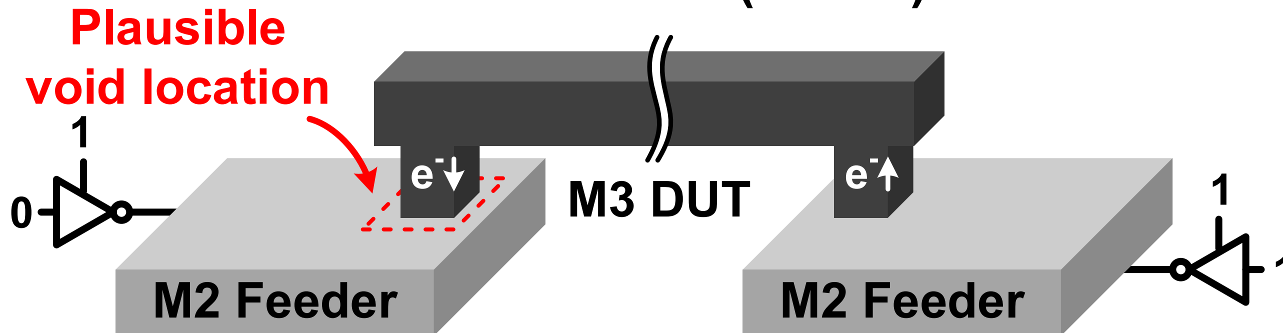
Failure Types In This Work



M3 DUT (50μm, M2 Feeder)

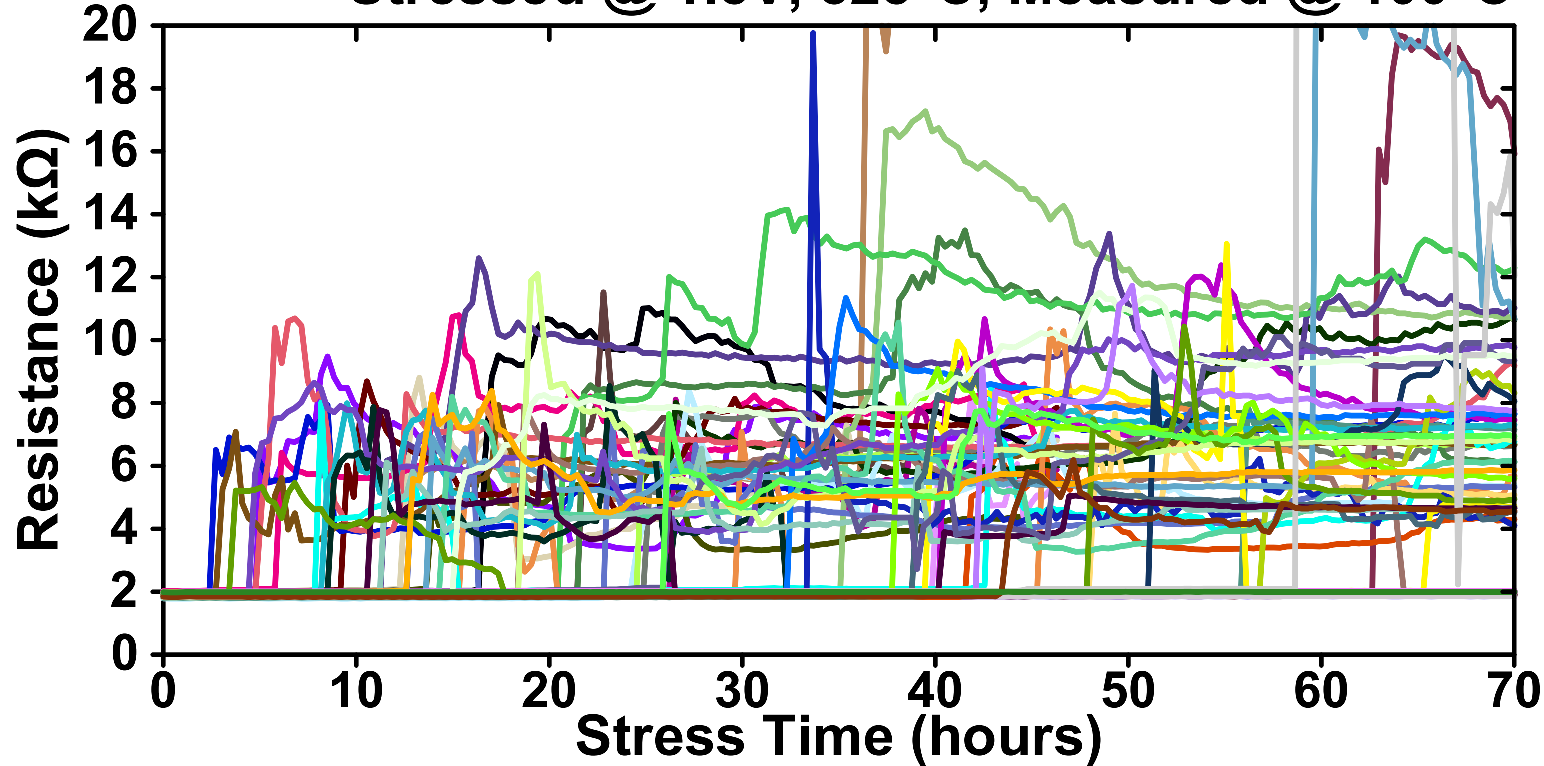


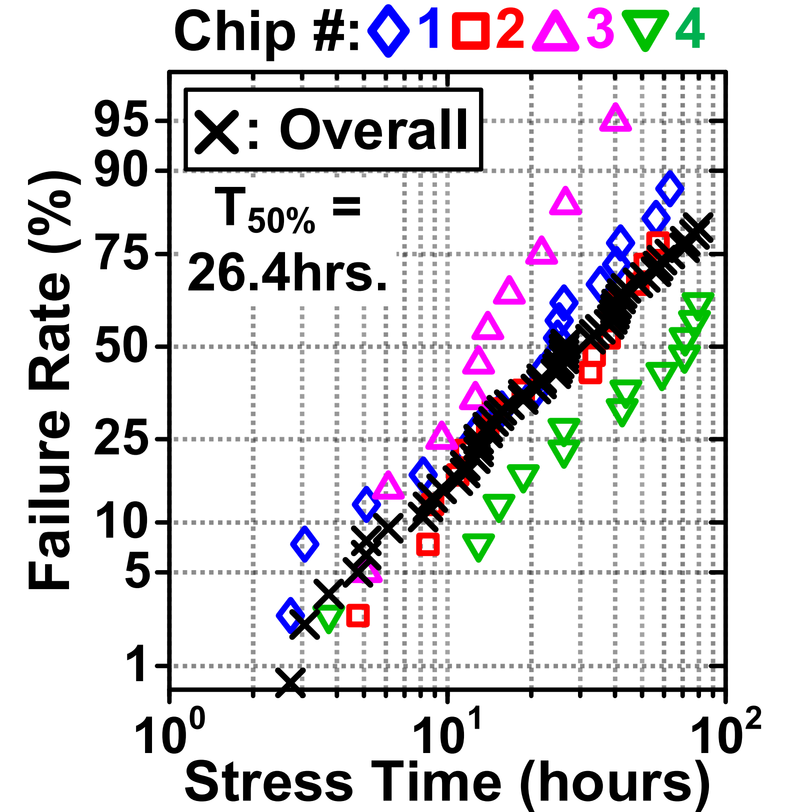


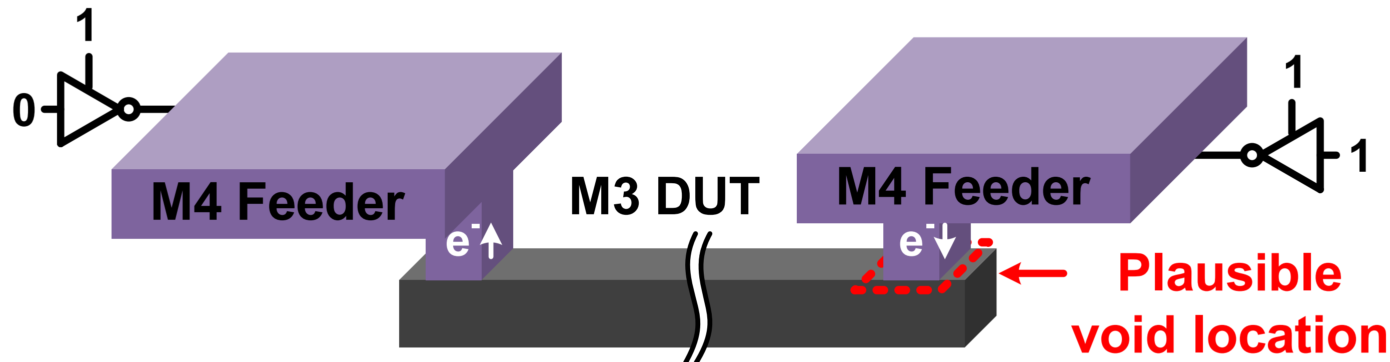


- Predominantly abrupt resistance increases, attributed to voids formed beneath the via

M3 DUT (50μm, M4 Feeder)

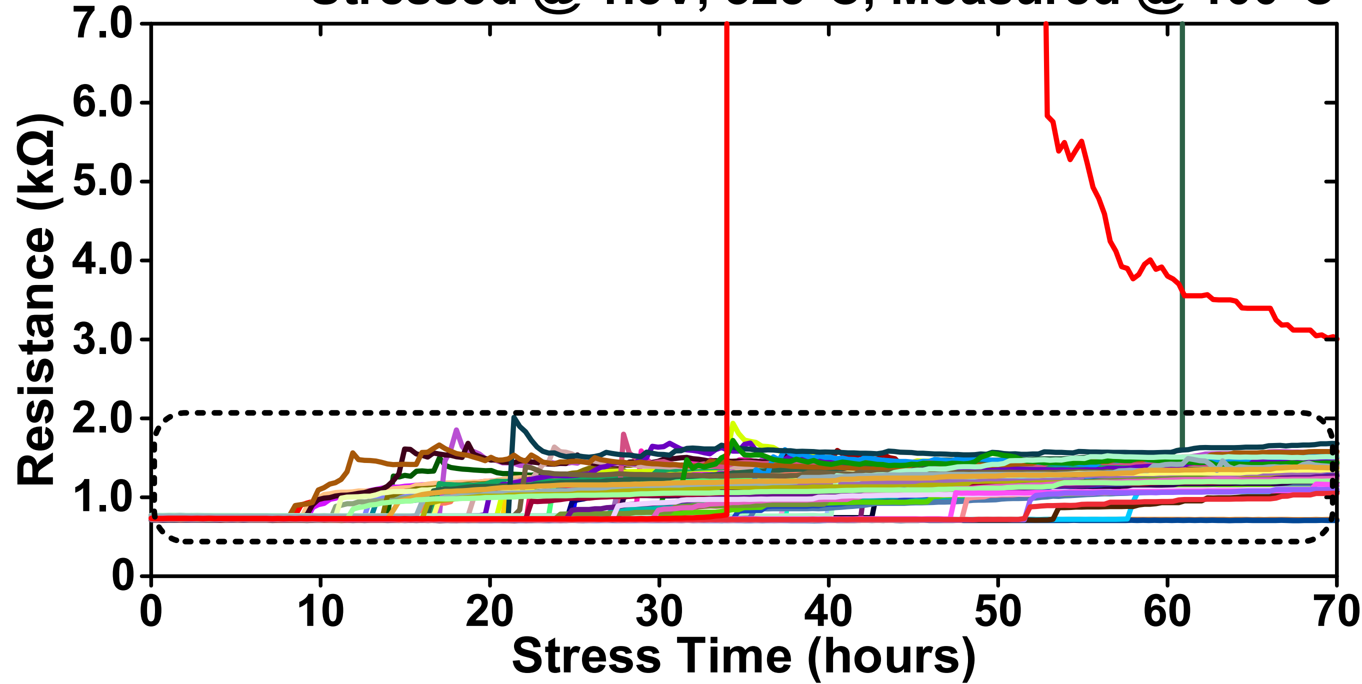


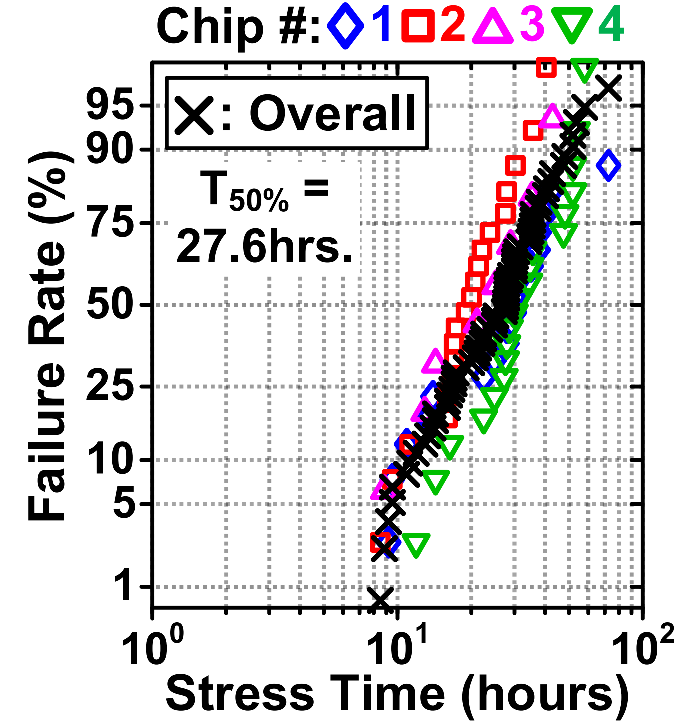


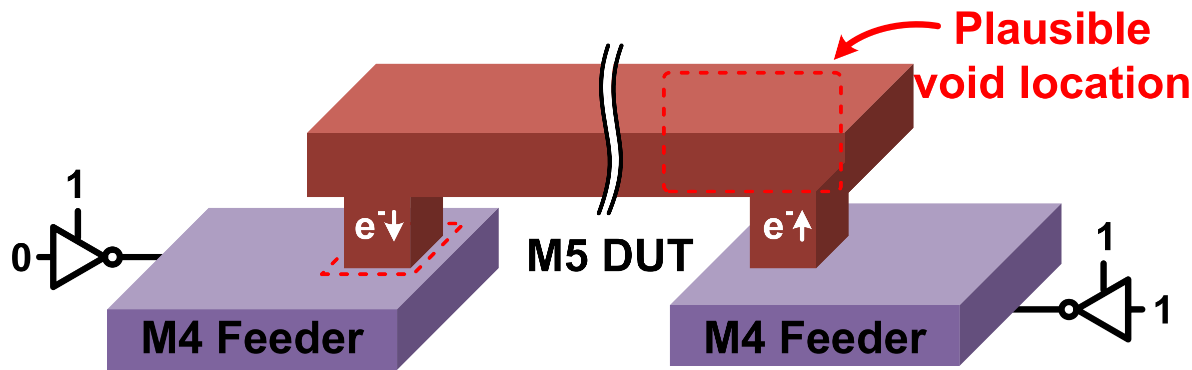


- Similar behavior with abrupt resistance shifts but longer MTTF

M5 DUT (50μm, M4 Feeder)

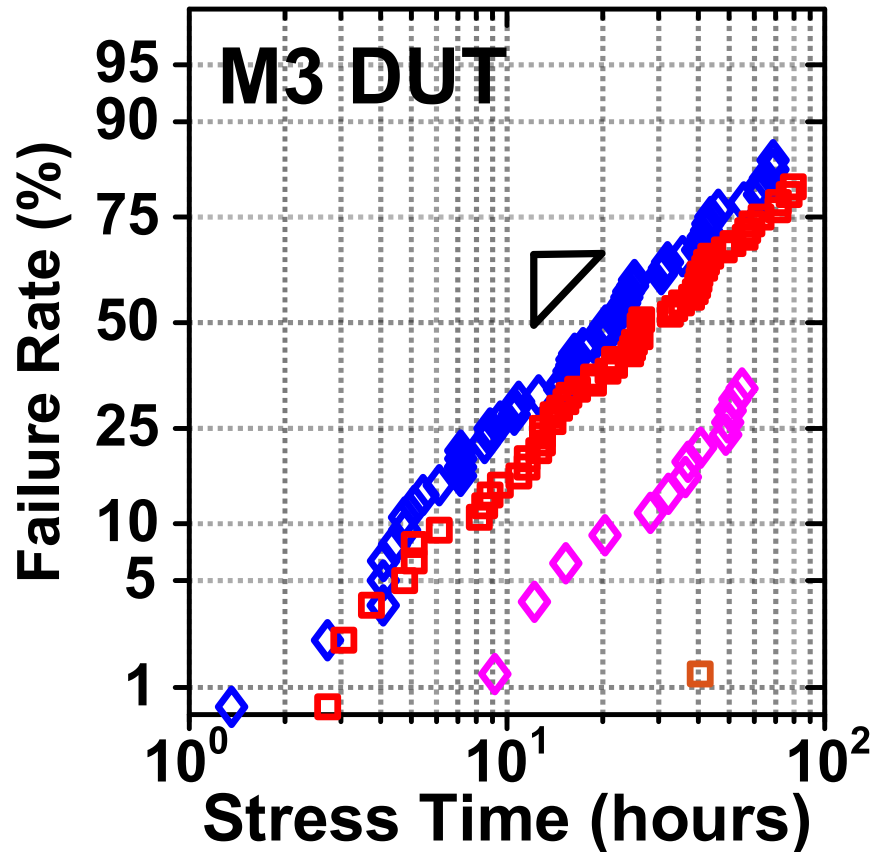


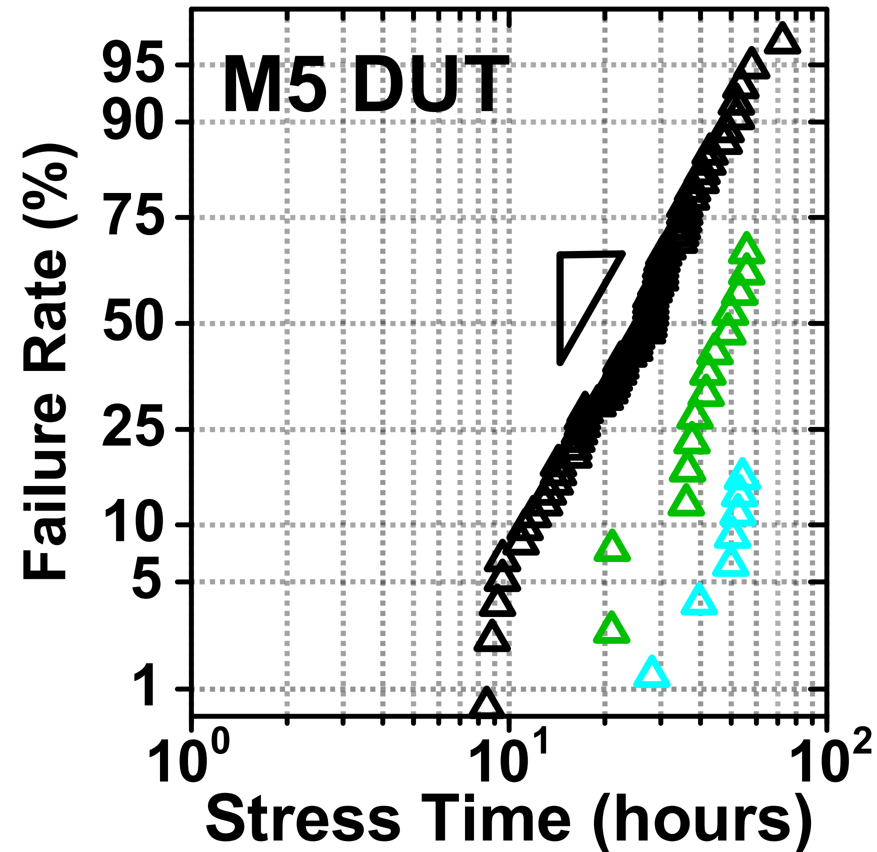




- Predominant failures of progressive type, despite identical J_{STRESS}

Abrupt vs. Progressive EM Distributions





Part 2 Summary

- Array-based EM test vehicle featuring on-chip heaters, parallel stress and Kelvin sensing capabilities demonstrated in 16nm FinFET
- EM trends analyzed for various wire structures
  - Abrupt failures in M3 DUTs, progressive failures in M5 DUTs
  - Wire width affects abrupt failure lifetime (possible bamboo effect in narrow wires)