[Invited] Characterization and Mitigation of EM Effects in Advanced Nodes

Chris H. Kim

Students: Nakul Pande, Yonghyeon Yi, Chen Zhou\textsuperscript{1}, Xiaofei Wang\textsuperscript{2}

University of Minnesota

chriskim@umn.edu, chriskim.umn.edu

\textsuperscript{1}Now with Maxim Integrated, \textsuperscript{2}Now with Intel

Collaborators: Cisco, TSMC, Mentor Graphics, and Intel
Electromigration In Interconnects

- EM depends on current density, temperature, and mechanical stress
- Impact: IR drop in power grids, increased delay in signal wires

A.S. Oates, et al., TDMR, 2009
Power Grid EM Characterization Challenges

• High stress temperature (>300°C) $\rightarrow$ active load will be damaged
• Large amount of data required for statistical analysis $\rightarrow$ long test time
• Too many sample points $\rightarrow$ large # of IO pads
Prior Art: Power Grid EM Test Structure

• Total resistance of 3x2 50μm long test structure stressed at 325°C with constant current

• Key observations: Faster failure compared to single-link, multiple resistance jumps, different growth rates

B. Li, IRPS 2018 (IBM)
Prior Art: Voltage Tapping Technique

- Effect of individual voids or extrusions can be measured accurately

F. Chen, IRPS 2015 (IBM)
Our Work: 9x9 Power Grid EM Test Structure

- M4-M3 “pseudo” power grid with three pad connections (A, B, C)
- Voltage tapping through top and bottom vias
- Strong connection to IO pads using multiple vias and wide wires

C. Zhou, C. Kim, VLSI Technology Symposium 2018, TDMR 2020
IO device based transmission gates used for voltage monitoring
- Circuits >400μm away from heaters to protect from high temp.
Poly resistor based on-chip heaters enables (1) fast and accurate temperature control and (2) on-chip control circuits.

- Three heater stripes for individual temperature control
- Excellent linearity thanks to four terminal Kelvin measurements

Stress temperature: 350°C
Die Photo and Test Setup

- Temperature control setup
  - Measure heater temperature coefficient of resistance (TCR) before EM test
  - Ambient temperature set to 0 °C to keep control circuits cool during test
162 node voltage samples → voltage drop across entire power grid

For a fresh grid, the size of the arrow and marker represents the current density (with the exception of nodes near V(+) and V(-))

Current density highest near IO pad connection points A, B, C
Total Power Grid Resistance and Voltage Drop Traces

- Stress mode: constant current mode $\rightarrow$ constant voltage mode
- Due to voltage compliance limit of source meter
Failure Modes and Healing

- Both abrupt and progressive failures observed
- Temporary healing observed
  - Electrical stress (forward)
  - Mechanical stress (backward)
- Voltage jumps are due to either EM in the wire itself (large jumps) or increased current due to EM in neighboring wires/vias (small jumps)
EM Failure Location Analysis

- Branch with largest voltage shift likely to be failure location.
- Resistance shift not instantaneous (i.e. gradually changes over several minutes → longer timescale under nominal condition.)
First EM Failure Location

- Three current stress modes applied to multiple chips
- First failure located near negative voltage terminal due to EM tensile stress

TTF = 6.80 hours  
(10mA, 350ºC)

TTF = 4.98 hours  
(10mA, 350ºC)

TTF = 0.37 hours  
(15mA, 350ºC)
EM Failure Rates

- Constant current stress: failure rate increased rapidly due to increasing current density in alternative paths
- Constant voltage stress: failure rate decreases due to decreasing total current
Part 1 Summary

- Voltage tapping technique used to track EM induced voltage drop inside a “pseudo” 9x9 power grid
- Early failures occur near the negative voltage terminal
- Failure rate rapidly increases after the first few failures due to higher current density in alternative paths
- Healing was easily observed which may be due to redundant current paths of power grid
- Data useful for calibrating EM models and prediction tools
16nm Test Vehicle For EM Characterization

- Wide feeders to minimize IR drop
- Folded to maximize area utilization
- Parallel stress capability
- 4 terminal Kelvin sensing
- IO device switches to minimize leakage

N. Pande, et al., IEDM 2019
16nm Die Photo and On-Chip Heater Design

- Snake shaped metal heaters
- 4-wire sensing to accurately track temperature in heating area

N. Pande, et al., IEDM 2019
Test Structures

Feeder length = 70µm in all cases

- **M3 DUT + M2 Feeder**
  - 50µm, 100µm, 200µm

- **M3 DUT + M4 Feeder**
  - 50µm, 100µm, 200µm

- **M5 DUT + M4 Feeder**
  - 50µm, 100µm, 200µm
Failure Types In This Work

![Graph showing resistance vs stress time with labels 'Abrupt' and 'Progressive' with respective data points and images. The graph indicates an abrupt shift of resistance with stress time and a progressive shift with stress time. The data is referenced to A. S. Oates et al., TDMR, 2009, and S. Lee et al., IRPS, 2006.]
M3 DUT (50µm, M2 Feeder)

Stressed @ 1.5V, 325°C, Measured @ 100°C

- Predominantly abrupt resistance increases, attributed to voids formed beneath the via

\[ T_{50\%} = 21.1 \text{hrs.} \]
M3 DUT (50µm, M4 Feeder)

Stressed @ 1.5V, 325°C, Measured @ 100°C

![Graph showing resistance over stress time for M3 DUT and M4 Feeder.]  

- Similar behavior with abrupt resistance shifts but longer MTTF
**M5 DUT (50µm, M4 Feeder)**

Stressed @ 1.5V, 325°C, Measured @ 100°C

- Resistance (kΩ) vs. Stress Time (hours)
- Failure Rate (%) vs. Stress Time (hours)

- Predominant failures of progressive type, despite identical $J_{\text{STRESS}}$

Plausible void location in M5 DUT (50µm, M4 Feeder)
Abrupt vs. Progressive EM Distributions

M3 DUT

M5 DUT

Failure Rate (%)

Stress Time (hours)

M3 (50µm, M2)  M3 (100µm, M2)
M3 (50µm, M4)  M3 (200µm, M4)

M5 (50µm, M4)  M5 (100µm, M4)
M5 (200µm, M4)

Stress Time (hours)

$10^0$  $10^1$  $10^2$
$10^0$  $10^1$  $10^2$
Part 2 Summary

• Array-based EM test vehicle featuring on-chip heaters, parallel stress and Kelvin sensing capabilities demonstrated in 16nm FinFET
• EM trends analyzed for various wire structures
  • Abrupt failures in M3 DUTs, progressive failures in M5 DUTs
  • Wire width affects abrupt failure lifetime (possible bamboo effect in narrow wires)