Analysis of Neutron-Induced Multibit-Upset Clusters in a 14-nm Flip-Flop Array

Saurabh Kumar, Minki Cho, Luke Everson, Qianying Tang, Pascal Meinerzhagen, Andres Malavasi, Dan Lake, Carlos Tokunaga, Muhammad Khellah, James Tschanz, Vivek De, and Chris H. Kim

***Abstract*— We report a detailed analysis of neutron-induced multibit-upset (MBU) clusters measured from flip-flop arrays implemented in a 14-nm trigate CMOS. Depending on the strike location, charge collection efficiency, and circuit topology, the MBU clusters are characterized in terms of size and span, and a qualitative first-order analysis has been presented. A novel MBU analysis framework has been demonstrated that uses a weighted sliding window to characterize MBU clusters efficiently and accurately with minimal double-counting or mischaracterization of cluster size. To further explain the relative MBU cross sections, the unique MBU patterns extracted from measured data have been studied and analyzed to find layout dependencies. The results show the strong correlation between the internode proximity and MBUs. The analysis shows a higher soft error rate (SER) cross section for smaller MBU cluster size and smaller span while the bigger clusters have lower contribution toward overall MBU SER.**

***Index Terms*— FinFET, multibit upset (MBU), radiation effects, reliability, soft error.**

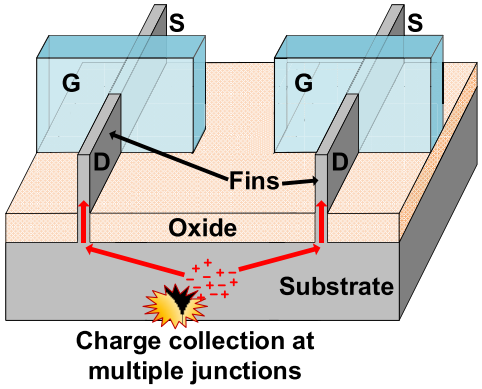

Fig. 1. Closer proximity of device junctions in FinFET transistors facilitates charge collection at multiple junctions, and thereby, increasing the MBU induction probability.

I. Introduction

THE continuous process scaling in integrated circuits has resulted in increased on-chip transistor density, and hence, more number of sensitive nodes [1]–[3] that has been a contributing factor toward higher radiation-induced soft error rate (SER) at the chip level. Moreover, with scaling, the inter-junction proximity is getting closer which further lowers in case of FinFET devices due to the elevated source–drain structures and lower fin-to-fin distance. This facilitates charge collection by multiple junctions due to a single radiation strike that may result in a higher probability of multibit-upset (MBU) induction. Hence, even though the devices have become more resilient to soft errors with scaling, the chip-level SER remains a critical reliability issue and MBU contribution in overall SER has shown to increase [5]–[9]. Fig. 1 illustrates the MBU induction in FinFETs, where charge injected by a single strike gets collected by multiple junctions, inducing an MBU error. As the device density increases, a single strike can inject a large enough charge that can drift/diffuse to more than one junction (due to lower junction-to-junction proximity) and induce multiple upsets leading to MBU. In memory circuits such as SRAM, accurate knowledge of MBU impact is crucial [10], [11] to determine various mitigation technique choices such as degree of column interleaving and selection of error correction codes (ECC). Much of the research on MBU is, therefore, focused on the characterization of soft error in SRAM arrays [12]–[14].

The above-mentioned techniques, however, cannot be directly applied to flip-flop and latch circuits that are distributed throughout processors and SoCs due to relatively larger area overhead and higher latency. Moreover, the existing techniques such as parity check or triple-modular redundancy (TMR) [15], [16] can be unreliable when multiple bits are affected. In TMR designs, circuits are replicated thrice to ensure correct output even if one of these fails by taking the majority vote. Similarly, in parity check, the parity bit keeps track of the number of 0's/1's in the register and reports an error if an upset gets induced in the register file. However, if multiple registers are physically placed in close proximity (a common scenario in register array groups in general-purpose processor architectures), chances of MBU induction increases which can result in an undetected error.

As shown in Fig. 2(a), in case of bit-wise TMR registers, MBUs can be corrected in two possible scenarios: 1) if the MBU is induced in a single register affecting multiple bits or

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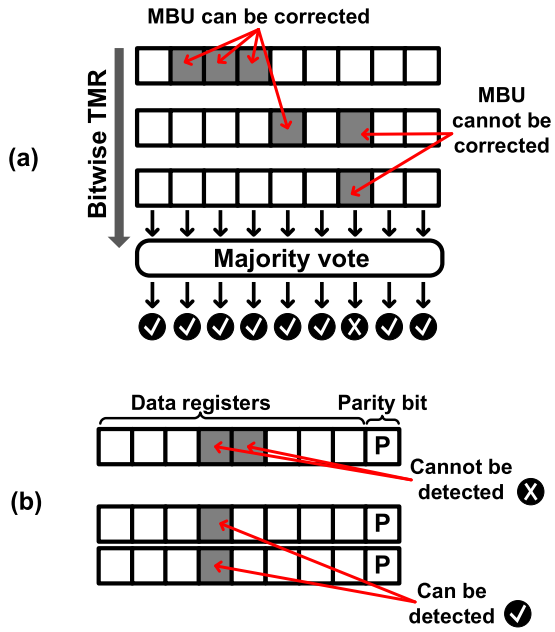


Fig. 2. (a) MBU in bit-wise TMR unit. MBU occurring in the same bit location of different register results in failure. (b) Parity check-based error detection fails in case of MBU in the same register.

2) if the MBU affects multiple bits in two or more registers, each at a different bit location. However, in case the errors occur in multiple registers at the same bit location, TMR fails. Similarly, in the parity check, MBUs affecting single bits in multiple registers can be detected while errors in the same register can go undetected, as shown in Fig. 2(b). These limitations make MBUs a concern in the processor design, especially in reliability-critical applications. Hence, an experimental study of flip-flop MBU is required to accurately assess the vulnerability of these structures to soft errors and to develop efficient mitigation strategies.

To our knowledge, this paper is the first attempt to characterize and provide a qualitative analysis of flip-flop single-bit upset (SBU) and MBU in the FinFET process technology. Most of the prior works have focused on comparative studies of the overall SER cross sections for different flip-flop topologies [17]–[20]. Dense flip-flop-based arrays are implemented in a 14-nm trigate CMOS and irradiated under neutron beam at the Los Alamos National Laboratory (LANL) to collect the statistical data for soft error analysis. MBU clusters with a wide range of size and span are extracted from the spatial maps of flip-flop arrays using a software tool. This allows the study of different MBU patterns individually to better understand the dependencies that lead to their occurrences in the arrays, depending on the strike location and proximity to sensitive nodes. Based on the flip-flop circuit topology, a qualitative analysis is presented to explain different MBU patterns observed in the data.

II. 14-nm Flip-Flop Array

Fig. 3 shows the flip-flop array circuit design and implementation. We leveraged the embedded scan chain in our previous back-sampling chain (BSC) array [21] to characterize and study neutron-induced MBUs in flip-flops. While the BSC

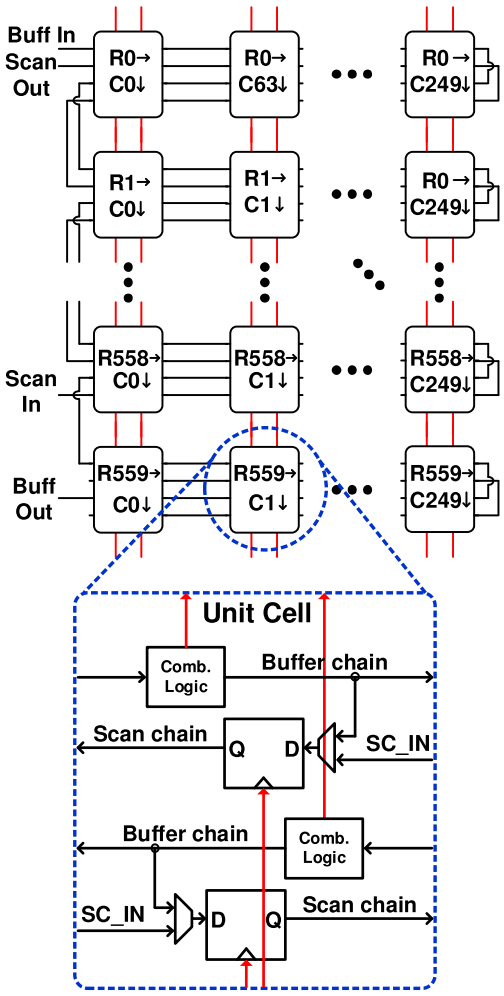


Fig. 3. Flip-flop array design implemented using a uniform and regular unit cell layout. The array served as the target circuit to capture radiation strikes for SBU/MBU induction. Each unit cell consists of two sets of flip-flops forming a part of the scan chain, each running in the opposite direction.

design was intended to study width and amplitude of single-event transient (SET) pulses, in this experiment, we use only the flip-flops in the array to study SBU and MBUs. Each BSC array consists of 560 × 250 flip-flops implemented using a unit cell-based layout. Each unit cell is tiled in both horizontal and vertical directions allowing 2-D scaling of the array. The scan chain and clock are routed in opposite directions to avoid any hold time violations. BSC array can be configured in two modes (test and scan). Initially, in scan mode, all flops are initialized with 1's before the test by selecting SC_IN as the flop input. Once the initialized array is set to test mode where buffer output is connected to the flop input and it is statically held to 0.

This unit cell-based implementation facilitated uniform layout implementation and enabled a scalable design without compromising on characterization accuracy. Master–slave D-type flip-flops with single clock input were implemented in the array, as shown in Fig. 4 (top). During irradiation tests, both clock and data inputs were statically held to logic low, resulting in the slave stage of the flop operating in hold mode while the master stage was transparent. In this mode, the slave stage is, therefore, susceptible to radiation strikes on the cross-

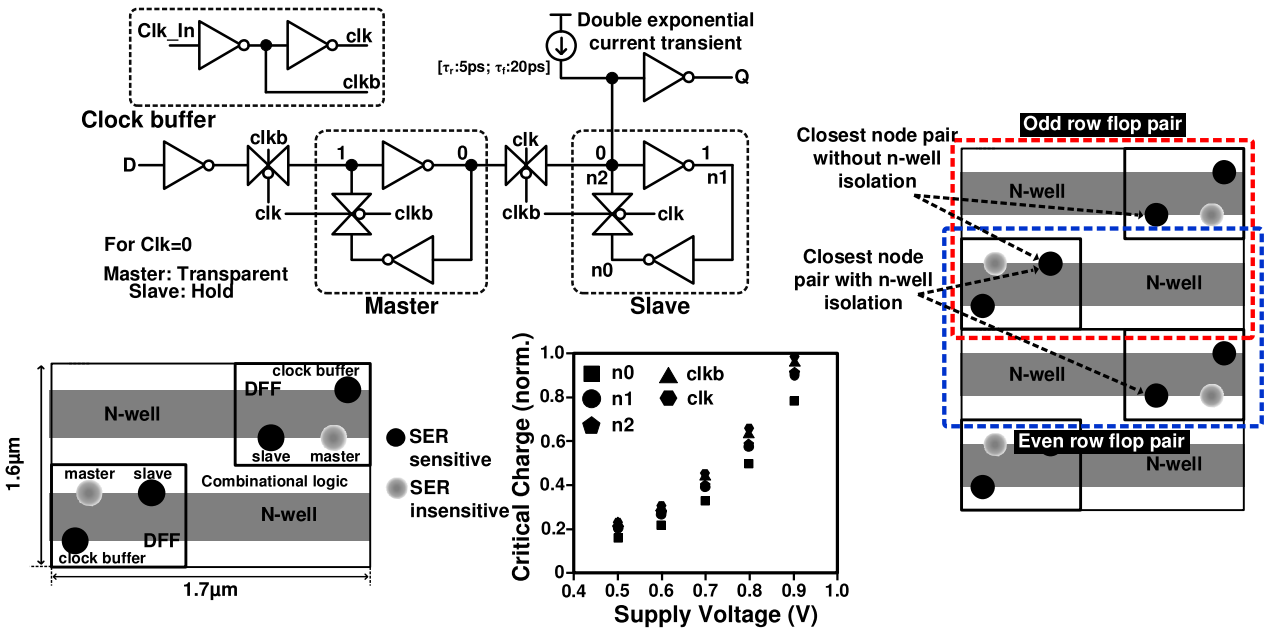


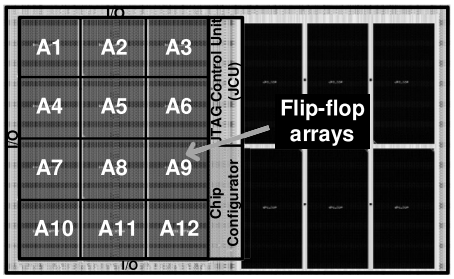
Fig. 4. Circuit design of the implemented master–slave flip-flop with slave and clock buffer nodes susceptible to radiation strikes (during irradiation: $D = 0$ and Clk_In $= 0$) (top). Simplified unit cell layout includes two flip-flops and combinational logic with two n-well rows (bottom). Two vertically stacked unit cells showing odd/even row flop that are discerned by n-well isolations. Critical charge (Q_{crit}) simulations show similar strike sensitivities for both clock and slave stage nodes across different supply voltages.

coupled inverter loop which could cause the stored data to flip. In addition, a strike on the clock buffer nodes could also induce an SET pulse which could result in an incorrect sampling of 0, thereby flipping the stored data bit. The master node, being transparent, cannot affect stored data and hence can be ignored in the analysis. This resulted in four sensitive nodes in each unit cell, as shown in Fig. 4.

The location of n-wells also plays a role in determining the susceptibility of nodes toward MBU. Uemura *et al.* [22], [23] and Furuta *et al.* [24] have shown that n-wells tend to create isolations that attenuate charge diffusion across the well region, thereby reducing the MBU probability for nodes that are located across the well. In the test chip layout, n-wells run in the horizontal direction [Fig. 4 (bottom)], and the n-well effect has been captured in terms of MBU contribution by specific nodes that have closer proximity but are located across the well. In the case of odd flop pairs, the closest sensitive nodes do not have n-well isolations between them as shown in the vertical stack of two unit cells (Fig. 4). While in case of even pair flops, the closest sensitive node pair has two n-well isolations and relatively larger internode distance. More details can be found in the measured results and analysis section. Please note that the sensitive node pair in this paper refers to the sensitive drain regions of the nodes that are susceptible to charge collection and error induction. To keep the discussion simple and analysis easy to understand, sensitive nodes (with sensitive drain regions) have been shown throughout. To simulate the SER sensitivity for all susceptible nodes, a current source modeling a double-exponential transient pulse (with $\tau_{\text{r}} = 5$ ps and $\tau_{\text{f}} = 20$ ps) for charge injection was used to estimate critical charge (Q_{crit}) [25], [26], where Q_{crit} is defined as the minimum amount of charge that is required for logic flip at the given node (in case of slave stage nodes) or the amount of charge required to induce an SET which can result in incorrect sampling and a data flip (in case of clock buffer nodes). Fig. 4 (bottom) illustrates various sensitive nodes that are susceptible to radiation strikes which include the clk and clkb nodes in the clock buffer and $n0$, $n1$, and $n2$ nodes in the slave stage. The simulation results in Fig. 4 show that the critical charge values for each of these nodes are very close to each other. For a supply voltage of 0.7 V, simulations show that the average normalized Q_{crit} for any one node in the slave stage is 0.36 units while that of the nodes in the clock buffer is 0.41 units. Moreover, this difference gets smaller as the VDD scales down, making all nodes equally sensitive toward strikes. Hence, it is important to include clock buffer nodes as well as slave stage nodes in the analysis.

III. Neutron Irradiation Test Setup

The 90 test chips were irradiated in parallel at LANL under accelerated neutron beam for five effective days. Fig. 5 shows the test chip specifications depicting 12 identical flip-flop arrays implemented in each chip. Irradiation tests were performed at multiple supply voltages ranging from 0.7 to 0.4 V. This enabled analysis of MBU dependence on the supply voltage. To ensure minimal error in the scan circuitry, the supply voltage of the scan chain was fixed to a higher value of 1.1 V. During the irradiation phase, the supply voltage was scaled to the desired value, and the chips were irradiated under the beam to allow error induction. Afterward, scan out was performed at a higher voltage to collect the SER data. During measurements, in order to compensate for intermittent beam current fluctuations, appropriate scaling was used to linearly scale failure in time rates with respect to the associated beam current value.



Technology	14nm, 9-metal layer, tri-gate HKMG CMOS
Die area	3.7mm x 2.2mm
Core voltage	<0.7V
Scan voltage	1.1V
Array dimension	250x560x12 = 1.7 million flop stages

Fig. 5. Implemented 14-nm test chip layout and feature summary.

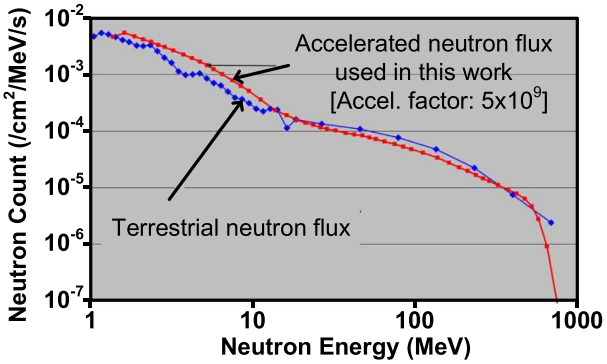


Fig. 6. Accelerated neutron beam energy profile at LANL facility. The spallation neutron beam profile closely follows the terrestrial neutron spectrum with an acceleration factor associated with it to speed up irradiation tests.

Fig. 6 shows the neutron beam flux versus energy profile used for the irradiation tests. The neutron beam energy spanned from 1.38 to 750 MeV. Neutron beam used in our irradiation tests closely matched energy profile of terrestrial neutron exposure (after accounting for the acceleration factor) which helped in emulation of real-world neutron exposure in an accelerated environment. The average neutron beam flux was 4.2×10^4 particles/cm^2/s.

IV. Analysis Framework

Fig. 7 shows the multicell upset (MCU) cluster analysis framework developed to characterize MCU cross sections. The goal of this analysis is to process the spatial map of scan-out data (denoting the position of each flipped bit in the flip-flop array) and determines the size (number of adjacent flipped bits) and span (center-to-center distance between farthest upset cells) of each MBU cluster. When determining cluster size and span, the highest weight (priority) is assigned to clusters with more flipped bits and smaller cluster span, since these are more likely to be induced by a single strike. In this paper, the cluster window dimension (which defined the largest MBU cluster size) is 4×4. This decision was made based on the measured data analysis where most of the clusters detected were within this range. A sliding 4×4 window scans the entire array map

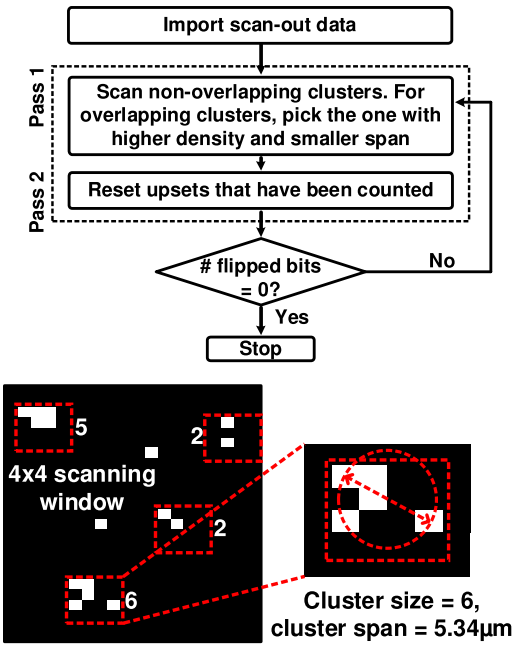


Fig. 7. MBU cluster extraction framework using the weighted sliding window approach. The proposed framework gives priority to clusters with the largest size and smallest span. (These clusters have highest induction probability.)

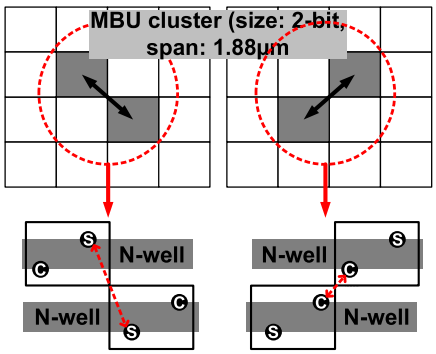


Fig. 8. MBU clusters with the same size and span but different orientations may result in different internode distances for SER sensitive nodes. This requires a close analysis of different MBU patterns.

and picks up all nonoverlapping MBU clusters. In the case of overlapping clusters, priority is given to the cluster with a higher weight (larger size and/or smaller span). All bits are reset to the default value of 1 after the corresponding clusters are accounted for, and the scan is repeated to detect remaining clusters. This iterative priority-based approach ensures that no flipped bit in any cluster is counted multiple times, and the use of a priority-based sliding window avoids the possibility of dividing a single MBU cluster and instead of counting it as two smaller clusters since it looks for the largest and densest clusters across the map and account of those first. The scan-out interval was limited appropriately such that the probability of multiple strikes at the same location is minimized; thus ensuring that MBU clusters are sparse in space.

Although the above methodology enables an efficient and accurate quantitative analysis of MBU clusters as a function of supply voltage, span and size, a closer analysis of MBU patterns, and their orientations in the layout are required

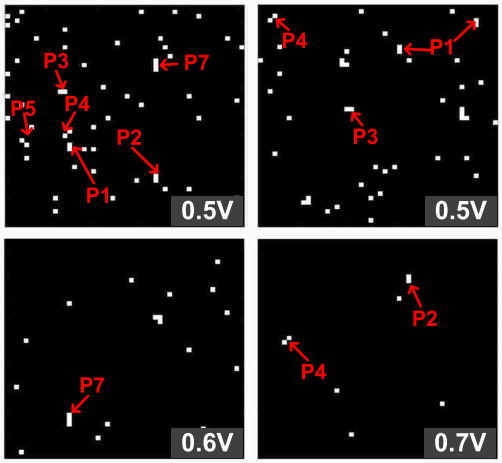


Fig. 9. Unique patterns (P1–P7) in spatial maps from different supply voltages showing MBUs induced during neutron irradiation test.

to gain additional insight into their induction and probable mechanisms that influence these behaviors. For instance, for a given span and size, there can be multiple cluster orientations, as shown in Fig. 8 which are not captured by the MBU cluster analysis (Fig. 7). These different orientations of upset cells within the cluster also correspond to different internode distances. In order to get a better photograph, the more detailed analysis is carried out, in which unique patterns pertaining to MBUs are extracted from the span maps and analyzed.

Fig. 9 depicts various MBU patterns found in the spatial maps. During the test, each array was initialized to all 1's, and data were scanned out after a fixed exposure time. Spatial maps were generated from the data resembling actual array bits with their locations preserved. The induced MBUs range from 1- (SBU) to 2-, 3-, and 4-bit patterns. Each of these patterns corresponds to unique node groups formed in a specific orientation within the array. Seven distinct MBU patterns were identified corresponding to distinct orientations based on the actual layout implementation, as shown in Fig. 10. The illustration also shows relative node locations for the corresponding MBU pattern in the layout. The dotted arrows are suggestive in nature showing the possible node combinations that have relatively higher MBU induction probability as compared to other node combinations for a given pattern. "S" represents the slave stage nodes, and "C" represents the clock buffer nodes. Since simulations in Fig. 4 show similar SER sensitivities for the slave stage as well as clock buffer nodes, it is critical to consider both nodes in the analysis. For simplicity, only 2–3-bit MBU patterns are shown (although measured data show up to 4-bit MBU induction). P1–P5 represent 2-bit MBUs and P6 and P7 represent 3-bit MBUs with the following features.

1) *P1(P2):* Induced when any combination of slave or clock nodes in the odd(even) row vertical flop pair are involved.
2) *P3:* Induced when the sensitive node pairs in horizontal flop orientation are involved.
3) *P4(P5)*: Induced when the sensitive node pairs in diagonal flops with left (right) orientation are involved.
4) *P6(P7):* Induced when the three consecutive nodes in horizontal (vertical) flop orientation are involved.

V. Measured Results and Analysis

Fig. 11 shows the spatial upset map from one flip-flop array in a single chip for 0.5-, 0.6-, and 0.7-V supply voltages. To ensure that the probability of consecutive SBUs being interpreted as an MBU is low, we used data collected at supply voltages of 0.5 V and higher. In addition, timestamping was used with higher read-out frequency for lower voltage data to ensure that in a single scan-out map, all upsets were temporally close. This further reduced the probability of consecutive SBUs being induced by multiple strikes in a short time period. As shown in Fig. 11, the bit flips are illustrated by white dots in an otherwise black (denoting logic 1) map. The sparsely located flips indicate a relatively lower number of errors in each scan-out cycle, thereby ensuring a low probability of consecutive SBUs.

As shown in Fig. 7, the MBU clusters are extracted using a 4×4 window. The basic assumption here is that the cluster formed by a single particle strike, in most cases, spans up to four cells in both x- and y-directions. This hypothesis has also been confirmed by the measured data. Fig. 12 shows the MBU cluster cross section plotted against the cluster span for 2-, 3-, and 4-bit MBU clusters induced during the neutron irradiation tests. The plots shown here are for 0.5- and 0.6-V supply voltages. The SER cross section on the y-axis has been normalized to that of SBU which correspond to clusters containing single flipped bit.

The plots in Fig. 12 show a nearly exponential trend of SER cross section with respect to cluster span. With an increase in the intercell distance, the induction probability for MBUs reduces, resulting in a drop in cross section. Moreover, the trend lines for different cluster sizes for a given supply voltage depict lower cross section with an increase in the number of upset cells within the cluster. This can be attributed to the charge-sharing phenomena, in which more overall charge is required to induce errors in a larger number of cells, resulting in higher Q_{crit} and hence lower cross section. The spherical charge cloud that originates at the strike location travels in all directions via drift (in case the strike is closer to the depletion region) or diffusion (in case the charge induced is located far from any depletion region of the device junction). The charge magnitude drops exponentially as a function of distance which makes the error induction probability low for nodes far from the strike location. This may be the contributing factor toward a sharp decline in cross section with increasing span.

Comparing the results from 0.5- and 0.6-V supply voltages, we can see that for the same span, reduction in VDD results in a higher cross section due to the increase in Q_{crit} for cells operating at a higher voltage. Moreover, the relative span for same-size clusters at 0.6 V is shorter as compared to the 0.5-V supply voltage. This can be attributed to the fact that at a lower voltage, Q_{crit} for each sensitive node is lower which results in less charge required for each node to flip. At low voltages, therefore, the diffused charge is able to impact

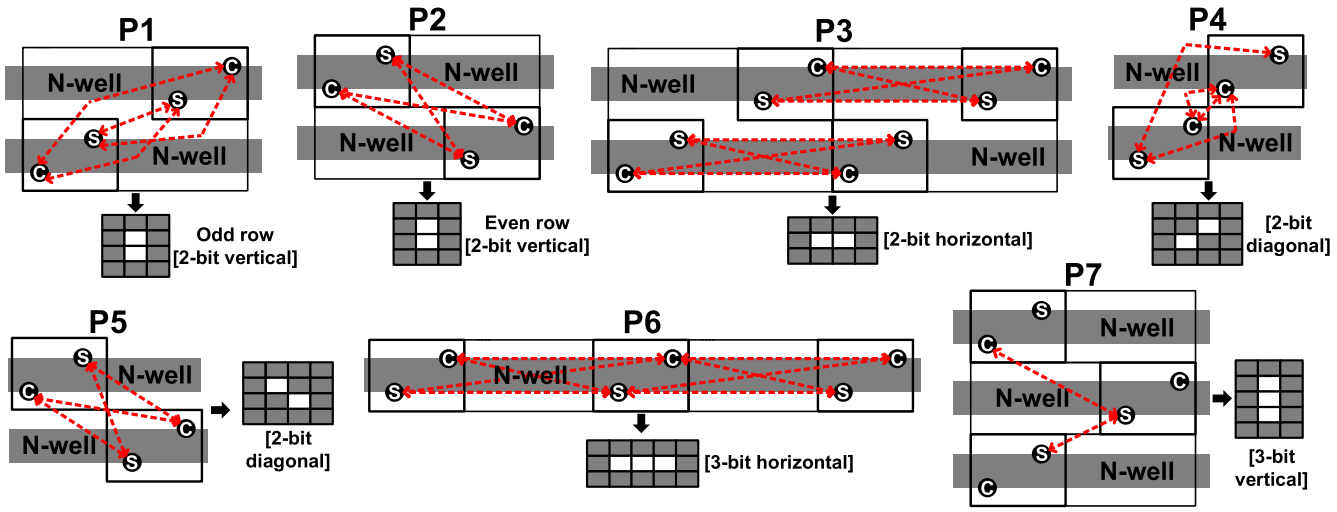


Fig. 10. Different sensitive node combinations that may induce possible MBU patterns and their corresponding scan-out patterns observed in the irradiation data. Seven unique patterns were extracted and analyzed based on the internode proximity and their relative locations.

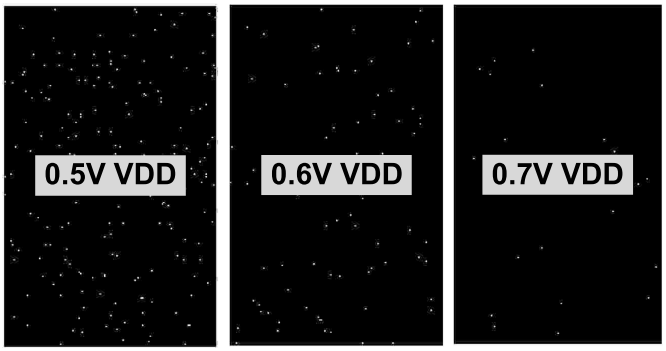


Fig. 11. Spatial maps showing measured SBU/MBU errors in single flip-flop array at different supply voltages. Maps with sparse errors ensure the minimal probability of overlapping/consecutive SBUs mistaken as single MBU.

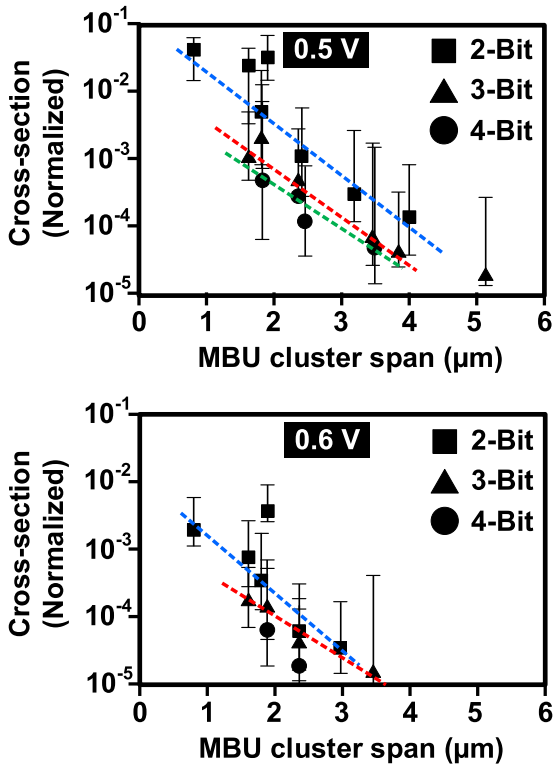


Fig. 12. SER cross section plotted against the MBU cluster span for different MBU cluster sizes at 0.5- and 0.6-V supply voltage. Trends show an exponential decrement in SER cross section with an increase in span and supply voltage.

nodes over a larger distance. The results in Fig. 12 demonstrate the probability of MBU clusters of varying sizes and spans since induction probability is proportional to the SER cross section. Another point to note is that with lower voltage, MBU contribution in overall SER goes up which is critical for circuits operating at near-threshold voltages (NTVs).

Fig. 13 shows the SER cross section measured from neutron irradiation for various MBU patterns at three different VDDs. With lower VDD, the critical charge drops, making circuits more sensitive to radiation strikes. This can be seen from the exponential increase in cross section as VDD scales from 0.7 down to 0.5 V. In Fig. 13, a 4-bit MBU distribution is also shown in addition to the seven patterns and one additional 3-bit pattern (3B-L). A 3B-L refers to the L-shaped 3-bit MBU that consists of 2-bit vertical and 1-bit horizontal flop combination or vice-versa. A 4B-V, 4B-H, and 4B-R refer to 4-bit MBU corresponding to vertical, horizontal, and square-shaped flop groups, respectively.

P1 and P4 MBU types have high-SER cross sections. This can be attributed to two reasons: 1) sensitive nodes are at closest proximity and 2) there is no n-well isolation between the closest sensitive node pairs. In the case of P1, the closest slave stage node pair has their nMOS devices without a well isolation as can be seen from Fig. 10. Similarly, in P4, the closest clock buffer node pairs have nMOS devices without a well isolation, thereby increasing chances of charge sharing and collection. In P2 and P5, the closest sensitive node pairs have relatively higher distance with n-well isolations between their pMOS and nMOS devices, which hinder charge diffusion and hence contributes to lower SER cross section. P3 and P6 are MBU patterns with the horizontal orientation. Here, the

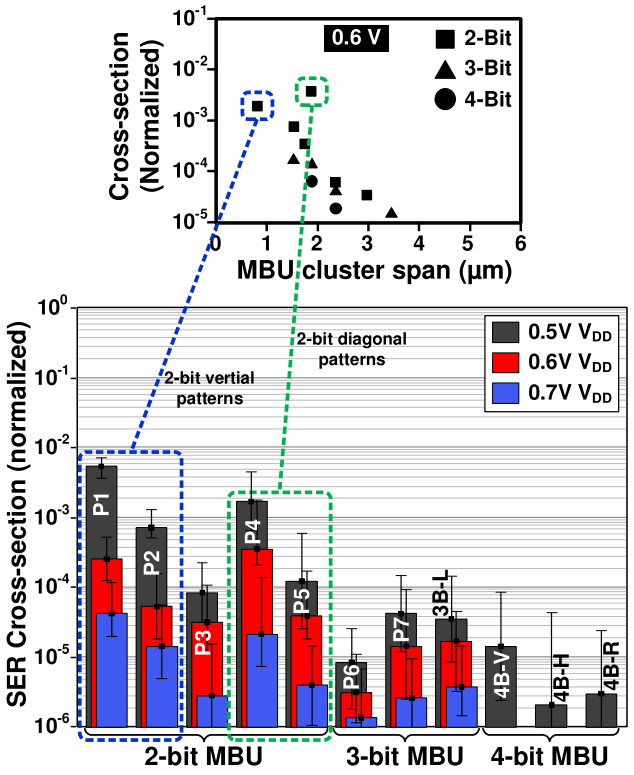


Fig. 13. Measured SER cross section for various MBU patterns at 0.5, 0.6, and 0.7 V.

distance between nodes is higher, resulting in lower cross section. Comparing P4 and P5 for slave stage nodes, P4 pattern has n-well isolations but has a higher contribution toward overall SER. A probable cause for this result may be the clock buffer nodes in P4 that have the closest proximity with no n-well isolation. P6 and P7 correspond to the 3-bit MBUs and hence have a lower contribution. A 3B-L pattern corresponding to 3-bit L-shaped MBU has higher contribution toward SER as compared to P6 (3-bit horizontal) since it consists of possible patterns with 2-bit vertical and 1-bit horizontal flop groups which have relatively smaller internode distance. The 4-bit MBUs are only observed for 0.5 V due to lower critical charge requirement. In the case of 4-bit MBUs, the vertical pattern shows a higher cross section as compared to horizontal due to the smaller relative distance between sensitive nodes.

The results from MBU cluster plots in Fig. 12 can now be seen in a better light with more detailed MBU pattern results presented in Fig. 13. For instance, the larger span should have a lower cross section (since charge drops with distance from the strike location). However, we can see from Fig. 13 that there is a data point with a higher cross section and higher span. This can be explained by the 2-bit MBU cross sections for the diagonally oriented patterns. Since the clock buffer nodes in P4 pattern have the closest proximity as compared to all other 2-bit patterns, its induction probability is higher resulting in higher cross section. Hence, the information regarding MBU patterns and their corresponding cross sections provide a deeper insight into the layout dependencies impacting MBU induction probability.

VI. Conclusion

In this paper, we report detailed SBU/MBU data from a flip-flop array implemented in a 14-nm technology for neutron irradiation tests. A more efficient and accurate MBU cluster analysis approach based on a weighted sliding window scan is proposed that accurately captures the count of various MBU cluster sizes. The results show an exponential drop in SER cross section as the cluster span increases which essentially indicates a steep drop in charge magnitude as it diffuses from the strike location. Moreover, the larger-sized clusters exhibit a smaller cross section which may be due to charge sharing among multiple nodes during charge collection.

In order to get deeper insights into the layout/circuit dependencies impacting MBU induction, the distinct MBU pattern analysis based on internode proximity for SER sensitive nodes has been proposed. More than seven unique MBU patterns pertaining to 2-, 3-, and 4-bit errors are extracted from the measured data, and a qualitative analysis is presented based on MBU dependence on the relative distance between sensitive nodes. Measured data shows higher MBU cross section for sensitive nodes that are in closer proximity as compared to distant nodes, giving important insights into the SER dependencies based on the physical layout and n-well orientations. Results shown in this paper are critical for circuit designs and may serve as a guide for layout implementation by carefully placing sensitive nodes to obtain higher SER resilience without incurring large overheads.

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