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Electromigration Effects in Power Grids Characterized from a 65 nm Test Chip

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***Abstract*—A 65 nm test chip to study electromigration (EM) events in integrated circuit power grids was taped-out and successfully tested. A 9×9 grid was implemented using M3 and M4 metal layers which was stressed under constant current and constant voltage modes. On-chip poly heaters were employed to raise the DUT temperature to 350 °C without damaging the peripheral circuitry and chip package. A bank of transmission gates based on IO transistors were used to tap out the M3 and M4 voltages at each intersection point of the power grid. Using the test structure, we could directly observe for the first time, the voltage drop map across the entire power grid. Subtle changes on the monitored voltage map uncovered mechanical stress dependent failure locations as well as self-healing due to redundant current paths. The EM failure rate and order of failure locations were also analyzed.**

***Index Terms*—Electromigration, power grid, EM healing, failure location, voltage tapping, on-chip heater, circuit based characterization.**

I. Introduction

ELECTROMIGRATION (EM) is the primary backend of line reliability issue caused by the continuous flow of electrons which results in a metal void within the interconnect. Depending on the type of circuit affected by EM, it has different effects. For example, if it occurs in a signal wire, the propagation delay of the signal may increase or the signal level may be degraded. If it occurs inside a power grid, EM can worsen the IR drop noise in the VDD and GND voltages. Fig. 1 shows a simplified diagram of node voltages in a power grid before and after EM failures. In fresh state, the VDD level is 1.18V which is close to the ideal 1.2V nominal voltage. After EM failures occur in the via and wire segment, the VDD level drops to 0.90V which may cause timing errors. EM effects in a single wire or a chain of wires have been studied extensively [1] [2]. Resistance shift is typically used as the indicator of EM failure. These studies mainly focus on how EM lifetime is affected by physical structure, temperature, current density, current frequency and duty cycle. In contrast, EM studies in power grid structures have been seldom reported due to the complexity of measurement, although several mathematic modeling works have been presented recently [3]–[5]. In [6], a 3×2 test structure was implemented to study EM effects in power grids. Here, the total resistance of the test structure was monitored to determine the time to failure, while the failure location was pinpointed using a scanning electron microscope image.

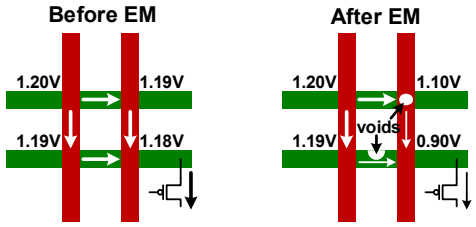

Fig. 1. IR drop increased due to EM failure or power grid.

Due to redundant current paths in a power grid, it is imperative to understand how the voltages at different points in a power grid change with EM voids. This is different from single wire measurements where the time to failure is determined simply based on a fixed shift (e.g. 10%) in the overall resistance. Furthermore, the order in which EM voids occur is critical to the circuit lifetime. In power grids, the current density profile is much more complex than that of a single wire structure. This difference can result in considerable discrepancy between EM behaviors in single wire and power grids.

In this paper, we employed the voltage tapping idea [7] to study the EM effects in a power grid. The main contribution of this work is that for the first time, we successfully tracked the failure location and failure time of each individual EM event in a power grid with realistic structure. We also report EM healing phenomena in a power grid under constant voltage and constant current stress. We tested several chips under a variety of stress conditions and found that the first failure location is always close to the terminal with a lower voltage level. For accelerated testing, we utilized on-chip poly heaters to raise the local die temperature to 350 °C. This approach obviates the need for an extensive high temperature setup and allows us to utilize on-chip circuits for EM characterization. The temperature control was proven to be accurate and efficient. We observed both abrupt and progressive failures, however, due to the difficulty in tracking progressive failures (wire resistance value increases gradually like a slope), this work mainly focuses on abrupt failures (failure occurs almost instantly and ends with open-circuit or very high resistance) and EM healing effects.

This journal is an extended version of our previously published conference paper [8].

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II. Power Grid EM Test Structure Design

The overall EM test structure consists of the power grid, an analog MUX for voltage readout, and on-chip heaters for stress temperature control.

A. Power Grid and Analog Multiplexer

We implemented the power grid test structure in Fig. 2 and Fig. 3, with 9 horizontal M3 wires and 9 vertical M4 wires. The width of each metal wire is set to 0.1 µm in order to accelerate the EM testing with a higher current density. Each wire segment is 20 µm in length, therefore the entire power grid is $160\,\mu\text{m} \times 160\,\mu\text{m}$. There are 81 intersections between Metal 3 and Metal 4 across the entire grid. A single minimum sized M3-M4 via is placed at each intersection. Multiple vias are used in real power grids to lower the resistance, however in our study, a single via is employed to observe failure within an attainable stress time. Therefore, 162 ($= 9 \times 9 \times 2$) measurement points are created uniformly across the entire grid, with half of the nodes at the top of the M3-M4 vias and the other half at the bottom of vias. The interconnection nodes are labeled on the grid, as shown in Fig. 2. To apply stress current through the power grid, three pad connection locations *A*, *B*, and *C* are selected on the grid. *A* is placed at the top left corner, *B* is at bottom right corner, and *C* is at the center of the grid. *A* and *B* are connected to two wire segments, while *C* is connected to four segments. Multiple vias are used between the power grid and the IO pads for reduced resistance. During stress, the current density is highest at the three access points. The current density would be very high if without enough vias. If the access locations fail too quickly, we would not obtain any useful data. Admittedly, the structure may not represent the exact power grid found in a real product. However, it is a suitable test structure for us to study the EM effects in a power grid. The authors did consider implementing two power grids (VDD and VSS) with active load current. However, active circuits placed between VDD grid and VSS grid may be damaged during the experiments due to the high stress temperature, so we opted for a single grid in this version.

The voltage tapping technique was implemented through metal vias which allows us to directly measure the voltage values at each intersection of the power grid test structure. As shown in Fig. 2, at every intersection node, the M5-M4 via taps the node voltage on M4 grid, while a M3-M2 via taps the M3 grid. No current flows through the voltage tapping vias. Although previous work [9] indicates that dummy vias could extend wire EM lifetime, the focuses of this work are power grid EM failure locations, failure order and EM healing observations, in addition to the EM lifetime itself. Therefore, we believe the results presented in this paper provide valid insight into EM failure behavior in power grids.

Note that the barrier layer between the copper wire and dielectric isolates the voltage tapping via and the power grid structure, and hence impact on the EM mechanical stress is minimal. Therefore, we can conclude that the power grid EM effect is not affected appreciably by the voltage tapping vias. M5 and M2 connect the tapping vias to the IO pads. To keep

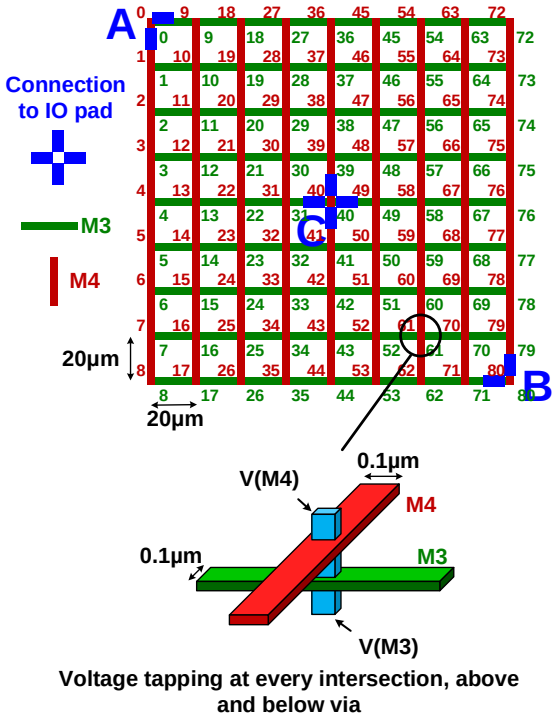

Fig. 2. 9×9 power grid EM test structure. Points *A*, *B*, and *C* are connected to individual IO pads.

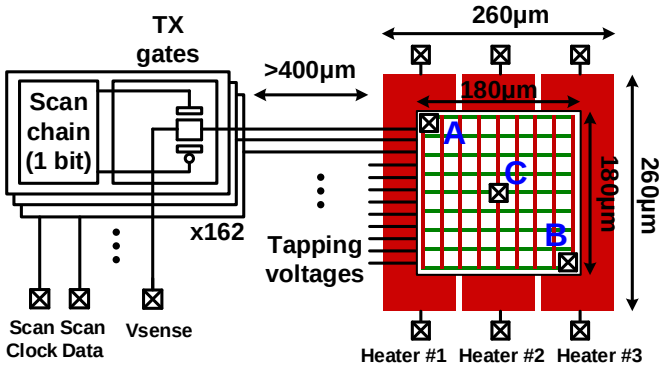

Fig. 3. EM test chip with on-chip heaters, power grid DUT, IO transmission gates and scan chain.

the number of IO pads of the chip tractable, a transmission gate multiplexer is used to select measurement voltage at a time. IO devices are used to suppress leakage current. A scan chain is used to enable one of the transmission gates. To keep the temperature of the multiplexer circuit in a safe range (e.g. $< 100\,^{\circ}\text{C}$), both the switch array block and the scan chain block are placed more than 400 µm away from the EM heating area. By accessing each top and bottom node, the voltage distribution of the entire grid can be directly measured. Based on this information, we can calculate the voltage drop value across each wire segment by taking the voltage difference between each two adjacent nodes, as shown in Fig. 4. For example, the voltage drop in M4 segment between node #9 and #10 is $V_{node\#9,M4} - V_{node\#10,M4}$. The voltage drop in M3 segment between node #1 and #10 is

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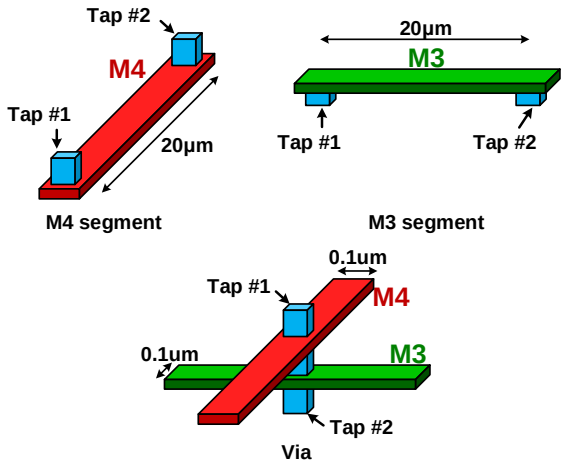

Fig. 4. Voltage drop calculation of each via, M4 segment and M3 segment, based on tapped voltage.

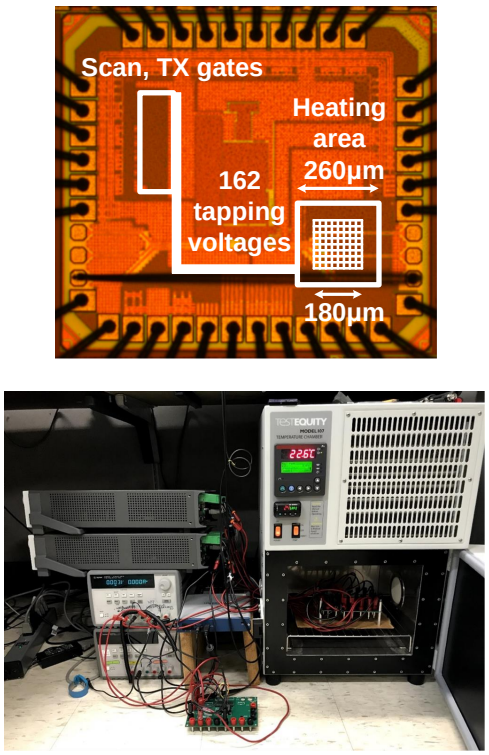

Fig. 5. Die photo of 65 nm test chip and the test setup.

$V_{node\#1,M3} - V_{node\#10,M3}$. Meanwhile, the voltage drop in M4-M3 via at node #10 is $V_{node\#10,M4} - V_{node\#10,M3}$.

B. On-chip heater design

The high temperature required for accelerated EM stress is provided by on-chip poly resistor heaters instead of placing the entire setup in an oven. On-chip heaters provide two unique capabilities; extremely fast temperature control and on-chip circuit based testing. In our design, three identical heaters are employed. The entire heating area is $260\,\mu\text{m} \times 260\,\mu\text{m}$. To ensure uniform stress temperature distribution across the entire power grid test structure, the grid is placed at the center of the

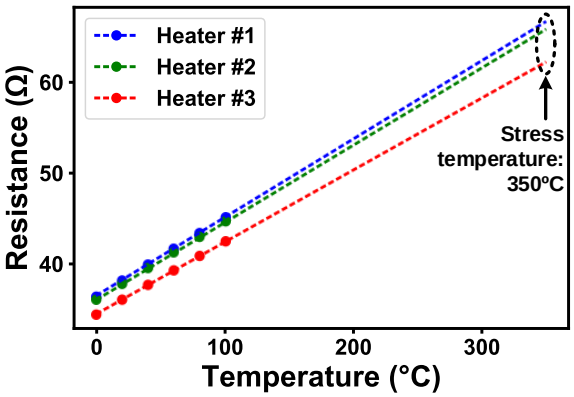

Fig. 6. Temperature coefficient of resistance (TCR) of heaters.

heating area. The die photo and the test setup is shown in Fig. 5. By applying high current through the heaters, we are able to maintain the test structure at the targeted stress temperature, which was 350 °C in this work.

During stress mode, the stress temperature was monitored by measuring the resistance change of the on-chip poly resistor itself. Considering that the power grid test structure is only several metal layers above the heaters, the temperature of the heater can be assumed to be very close to the temperature of the power grid. The effect of DUT joule heating is discussed in section II-C. The temperature of heater was calculated from the measured heater resistance value and pre-extracted temperature coefficient of resistance (TCR). Because the heater is made of metal layers, TCR results show excellent linearity versus temperature. This trend is characterized and validated under low temperature (100 °C) inside an accurate temperature chamber, an shown in Fig. 6. We can easily extend the trend line to the target temperature of 350 °C.

The entire test including repetitive stress/measurement cycles and heater temperature control was implemented by a software program shown in Fig. 7. The voltage sensing measurement takes 13 seconds each time, and is performed after every two minutes of stress. The stress current is maintained during the measurement without interruption. The power of each heater was adjusted individually every 0.83 seconds. The stress current direction was periodically reversed every hour to prevent EM in the heaters themselves as shown in Fig. 8. Compared to traditional oven based heating, our approach can raise the die temperature to the target value in seconds rather than minutes.

The main difference in terms of temperature control of this work compared with our previous work [2] [10] is the absence of a temperature ramp down before taking the voltage measurement. In other words, the measurement is taken at the same temperature as the stress mode, and therefore there is no need to change the temperature between stress and measurement mode. This was possible due to the long distance between the active circuits and the heating area. Since the on-chip circuits remain cool all the time, we were able to simplify the temperature control.

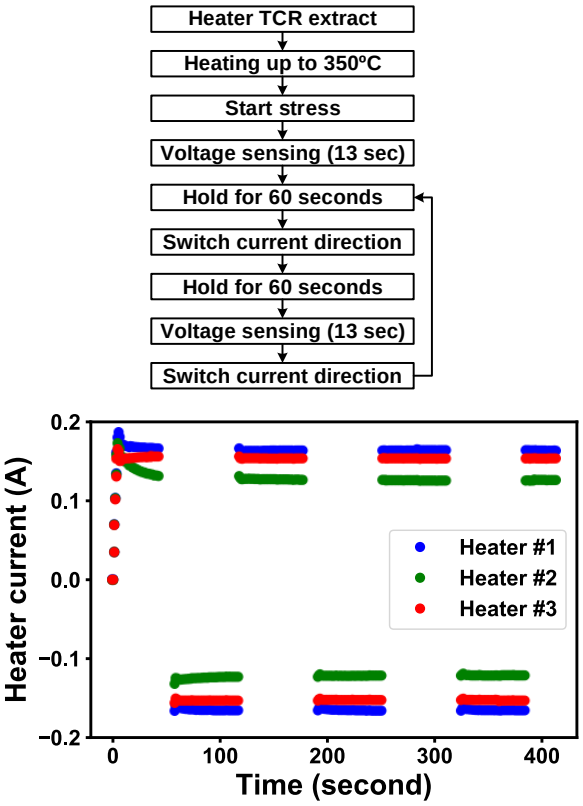

Fig. 7. (Top) temperature control loop. (Bottom) heater current direction was reversed periodically to prevent EM in heaters.

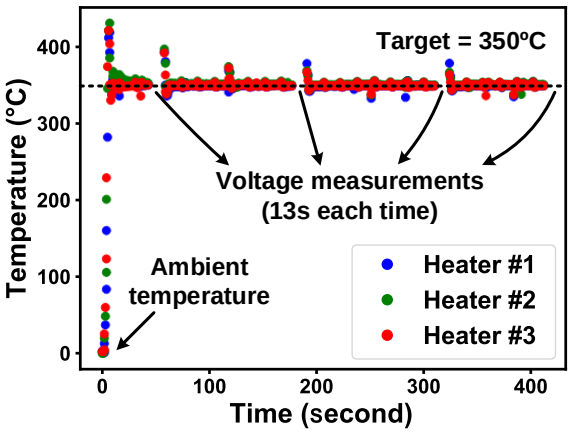

Fig. 8. Temperature logs measured from 3 heaters.

C. Discussion on DUT Joule heating

To accelerate EM testing, we chose a relatively large stress current for the size of the power grid. The stress current from points A and B to C was 10 mA resulting in a power dissipation of 2.8 mW. The average DUT temperature estimated based on the power grid TCR and power grid resistance is in the range of 399 °C to 407 °C. A detailed temperature map of the power grid can provide more insight but this requires specialized equipment or accurate thermal conductance values which are not available at this time. The authors believe that Joule heating cannot be ignored for EM studies as it can change the temperature distribution and thermal gradient

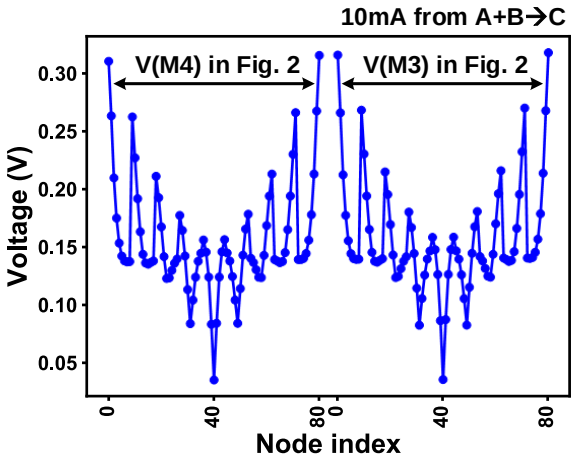

Fig. 9. Measured tapping voltages for all 162 M3 and M4 nodes.

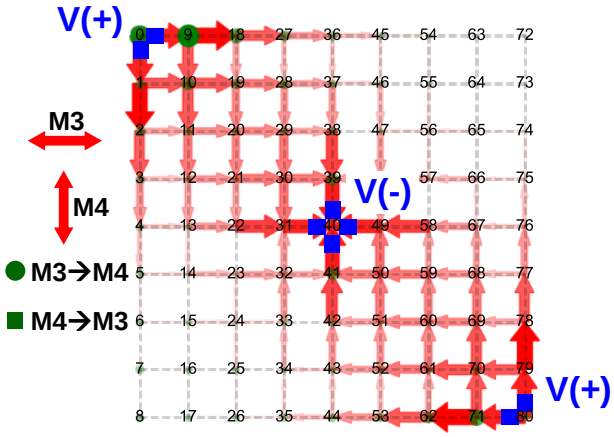

Fig. 10. Measured voltage drop for a fresh power grid. Arrow indicates the magnitude and polarity of voltage drop between adjacent nodes.

significantly. Estimating the EM lifetime in the absence of additional Joule heating effect involves detailed thermo-electro-mechanical modeling which is beyond the scope of this work. A reasonable alternative would be to measure the EM lifetime under lower stress currents which generates less Joule heating.

III. Voltage Drop Traces vs. Resistance Traces

This section compares our voltage drop traces based approach and traditional resistance traces based approach.

Fig. 9 shows the direct voltage measurement value of all 162 tapping nodes at fresh state t_0 for a 10 mA current flowing from node A and B to C. The voltage drop across each segment (M3 trace, M4 trace and M4-M3 via) was calculated and plotted as shown in Fig. 10. Here, the arrow direction indicates the voltage drop direction (i.e. current flow direction), while the width of arrow is proportional to the voltage drop value. For the M4-M3 via at each intersection, a circle denotes M3 to M4 current and a square denotes M4 to M3 current. Similarly, the size of the marker indicates the voltage drop across the via. Note that the voltage drop may not be directly linked to current density since the resistance of each segment may change if EM failures occur. However, for

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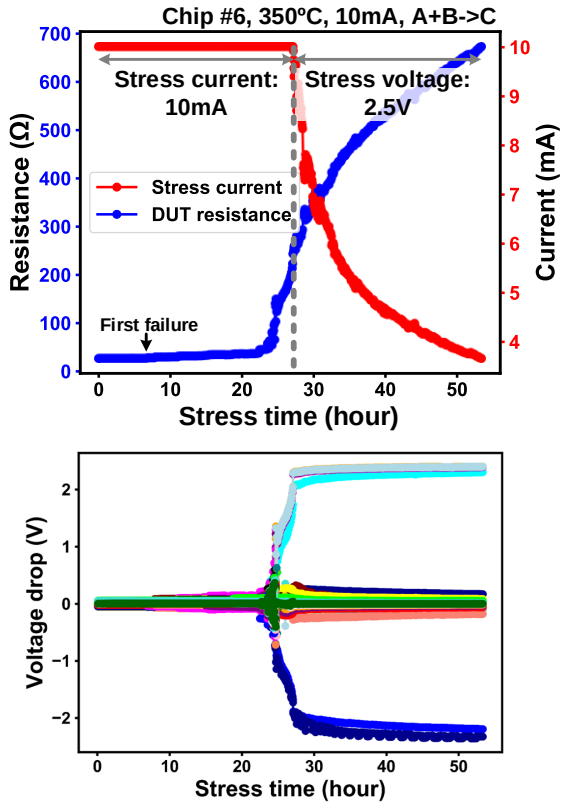

Fig. 11. (Top) Stress current and resistance trace of entire power grid. (Bottom) Voltage measurement traces of each power grid segment.

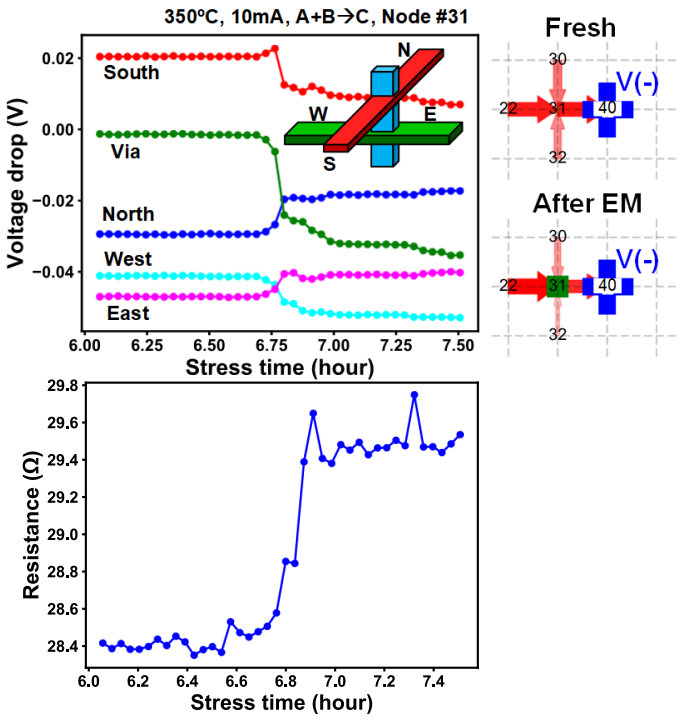

Fig. 12. Example of (top) nearby voltage drop traces and (bottom) resistance trace after an EM event. The increased voltage across the via suggests a change in the via resistance.

the fresh power grid results shown in Fig. 10, the arrow and marker dimensions represent the current density. As expected, current flows from the two corners *A* and *B* to the center point *C*, with almost no current in the upper right and lower left portions of the grid.

As shown in Fig. 11, the stress starts with a constant current of 10 mA flowing from node A and B to C. When the voltage drop of the entire power grid reached the source-meter compliance voltage of 2.5 V, it switched to constant voltage stress mode. Fig. 11 (bottom) plots the voltage drop value traces of all 72 M3 wire segments, 72 M4 wire segments and 81 M3-M4 vias during the entire experiment. Compared to the total resistance trace, the individual voltage traces provide more detailed information on EM effects.

Fig. 12 shows how the voltage drop in the north, east, south, and west branches change for the first EM failure location. The total resistance trace between $A+B$ and C is also plotted for comparison. In this test, a $10\,\mathrm{mA}$ stress current is sourced from node A and B to C. Only the traces around failure location are plotted. At 6.8 hours, the total resistance jumps from $28.4\,\Omega$ to $29.5\,\Omega$ in a very short time and then stabilizes around $29.5\,\Omega$, indicating that it is an abrupt EM failure rather than a progressive EM failure. From the resistance trace, we can only conclude that the first failure occurs at 6.8 hours and that it is an abrupt failure. There is no direct approach in traditional test structures to obtain the failure location during stress. Only scanning electron microscope (SEM) after stress can reveal the failure locations, but the failure order is still impossible to know. Note that the failure location and failure order are critical information in power grids. These information help us better understand the failure mechanism and impact. Fortunately, in our work, the tapping based direct voltage measurement allows us to easily find the failure locations in real time. As shown in Fig. 12 (top), when a failure occurs several voltage drop traces have sudden jumps that indicate a failure event. With only the traces that have significant changes displayed, we can easily find that the failure location is nearby nodes #22, #30, #31, #32 and #40. The change of the voltage can be attributed to two reasons: (1) resistance increase in the via or wire segment due to EM effect, or (2) current increase due to EM effect at a nearby location. In our analysis, we believe the failure location has the largest change among changes of all traces. For instance, Via #31 shows the largest voltage drop shift of $-31\,\mathrm{mV}$. Therefore, the change at via #31 can be attributed to the aforementioned reason (1), while changes in other traces can be explained by reason (2). In Fig. 12 (top), after the EM failure, the current flowing from #30 to #31 and from #32 to #30 decrease while the current from #22 increases. In other words, the current flow tends to bypass the high impedance path after EM failure.

Another interesting observation is that the abrupt failure actually takes several minutes to finish in our accelerated test. The resistance sample rate of this work is every two minutes. The long time for an abrupt failure to complete means that under normal operation, that failure may happen slowly over a long time period such as weeks or months.

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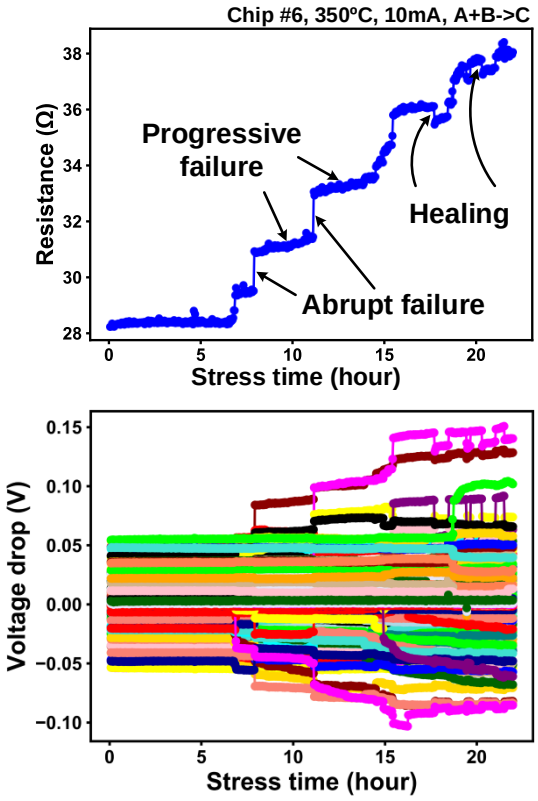

Fig. 13. (Top) Resistance traces and (bottom) voltage drop traces exhibiting EM abrupt failure, progressive failure and temporary healing behavior.

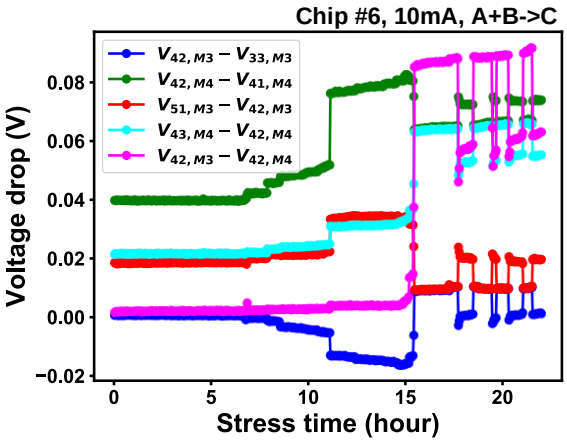

Fig. 14. Voltage drop traces near an early EM healing location #42 in chip #6.

IV. EM Failure and Healing Types

Fig. 13 shows the total power grid resistance between $A + B$ and C in the first 22 hours (10 mA, $A + B \rightarrow C$), along with voltage drops across each adjacent node. Several abrupt failures were observed which can be seen by the sudden resistance jumps. Between the abrupt jumps, resistance increased gradually indicating progressive EM failure. Besides the abrupt and progressive failures, healing effect was also observed, where there is a sudden resistance decrease. Abrupt and progressive failures have been widely observed; however this work is the first to report healing effect in a power grid.

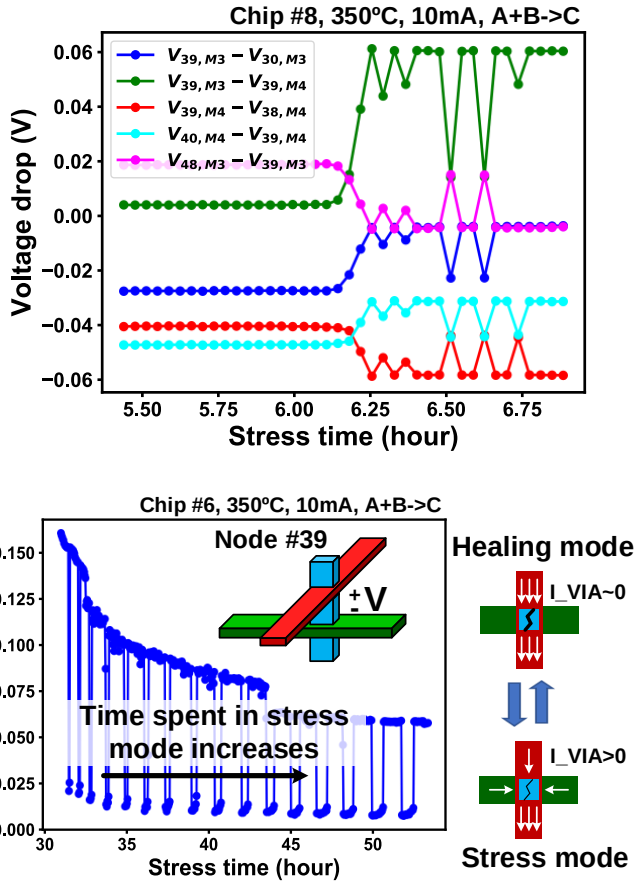

Fig. 15. Voltage across via toggles between stress mode and healing mode for an early failure (∼ 6 hours) and a late failure (∼ 30 hours). Time spent in stress mode gradually increases.

Earlier work [10] observed similar phenomenon, albeit in a single wire DUT, and concluded that the wire connections can be temporarily restored. As shown in Fig. 13 (bottom), several voltage traces show toggling behavior for stress times between 15 and 20 hours. Traces with large amount of toggling magnitude are replotted in Fig. 14. We conclude that via #42 is undergoing self-healing because via #42 has the largest fluctuation magnitude. We also observed healing effects in other test chips, for both early (before 8 hours) and late (after 30 hours) EM failures. Fig. 15 (top) elucidates the failure and healing cycles between 6 and 7 hours from chip #8. The first failure occurs around 6.2 hours on via #39, and after some gentle toggling, it completely failed at 6.8 hours. This observation clearly suggests that EM healing may happen soon after the failure. Therefore, the actual EM lifetime of power grids might be longer than previous predictions where EM healing was not considered. Fig. 15 (bottom) shows continuous failing and healing cycles in chip #6 at via #39. When the voltage drop across the via is larger than 50 mV, the connection is open and via is in healing mode. When the voltage drop is less than 25 mV, the connection is restored and the via is returned to stress mode. After 30 hours, the stress has switched to constant voltage mode (2.5V). As the power grids total resistance increases, the stress current keeps reducing, and it took longer and longer to break it again. This

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explains why in Fig. 15, the duty cycle between stress mode and healing mode increases with time.

EM healing was not addressed adequately in previous works. One reason could be due to the low sample rate used in those works which made it difficult to capture temporary healing behavior. [11] reported EM healing in a single Aluminum wire. In the authors previous work [10], EM healing was reported for the first time from a single dual-damascene copper wire. Both [10] and [11] suggest three possible causes for EM healing: 1) thermal contraction/expansion, 2) high temperature annealing, and 3) mechanical back stress. In this work, for the first time, we report EM healing in a power grid under constant current stress. Unlike previous works where the temperature was lowered during measurement [10], this work does not involve any temperature cycling, and thus thermal contraction and expansion can be ruled out as the reason behind the healing phenomenon. We believe EM healing is a natural process occurring in power grids due to the combination of electrical EM and mechanical stress. When electron wind pushes the metal atoms in one direction, compressive stress is formed at the higher voltage side while tensile stress is formed at the low voltage side. Mechanical stress then counteracts electrical EM. Since electrical EM is initially much stronger than the mechanical stress effect, wire breaks down. When the wire connection is broken, EM stress current immediately disappears, while mechanical stress persists. If the damage caused by EM is not serious enough, it could be reverted and restored by the mechanical stress. In our experiment, we saw failing and healing cycles because once mechanical stress restored the failure, the stress current came back on and broke the wires again. Healing and failing cycles do not necessarily involve a large number of Cu atoms moving in and out of the failure location. It only requires expanding and shrinking of a tiny void to induce open and short connection at the via. Or say, the via is always on the verge between conducting and open states. The two states may alternate due to EM and mechanical stress competing against each other. A thorough proof of this hypothesis requires extensive focused ion beam (FIB) analysis, which is beyond the scope of our work. Healing was rarely discussed in previous works because single wire test structures do not have any redundant current paths, so stress current is forced even after an EM failure, resulting in permanent damage that cannot be reversed. However, a power grid structure is different in that it has numerous redundant paths allowing the current to bypass the failure location immediately upon an EM event, providing the opportunity for stronger healing. Note that in our previous work on single wire test structure where limited healing was observed [10], constant voltage stress was applied instead of constant current. Since EM healing effect was overlooked in previous studies, the actual lifetime of a power grid might be significantly longer than previously thought. Since the stress temperature was fixed to 350 °C, it is unclear whether high temperature annealing is also a reason for EM healing, or whether high temperature is a requirement for healing to occur.

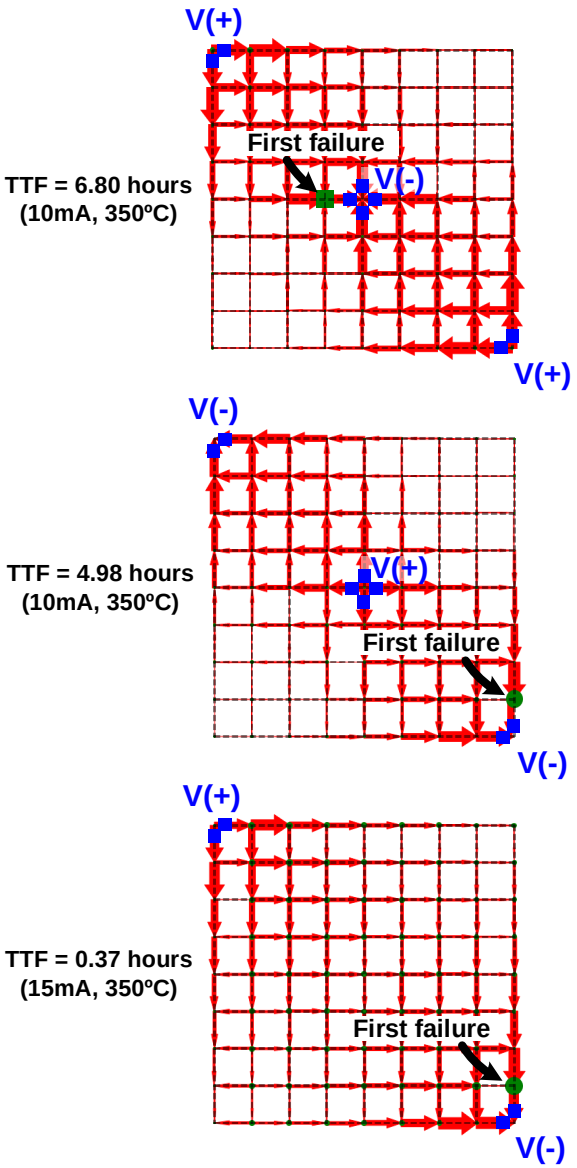

Fig. 16. First EM failure locations for different stress current configurations. Due to mechanical stress effects, the first failure occurs near the negative voltage terminal.

V. EM First Failure Locations

To study the factors that affect the EM failure locations, we have conducted experiments using different stress current configurations. Out of all locations failed during stress, in this section, we are interested in the first failure location under each stress condition. Fig. 16 shows the first EM failure point under three different stress current configurations: 10 mA, $A+B \rightarrow C$; 10 mA, $C \rightarrow A+B$; and 15 mA, $A \rightarrow B$. In all three cases, the first EM event happened close to the negative voltage terminal denoted V(-).

In our analysis, we conclude the first failure location is determined by three factors: 1) stress current density; 2) stress current direction (mechanical stress); 3) metal wire physical structure (via location). Our results match results from previous work [12].

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1) Current density: In a power grid, even though the grid structure is uniform, the current density across the entire gird map could be non-uniform depending on the load current distribution. In general, the connection point between power grid and the pad/bump has the highest current density since all nearby current is concentrated to that connection point.

2) Current direction: A higher current density usually shortens the EM lifetime, however, the current direction also plays an important role in the EM failure. Electron wind pushes metal atoms to move along the wire line. However, the local void can only be formed if the amount of atoms pushed out is larger than the amount of atoms pushed in. At the positive voltage terminal, metal atoms are mainly pushed in instead of pushed out, thus compressive mechanical stress builds up. Void will not form under compressive stress. This is the reason why even with a very high current density, EM failure still doesn't occur at the positive voltage terminal. On the other hand, at negative voltage terminal, metal atoms are mainly pushed out, therefore tensile stress is built up which facilitates EM void formation.

3) Metal wire physical structure: As shown in Fig. 16, the first failure locations are always at M4-M3 vias, rather than M4 or M3 wire segments. As we know, in a dual-damascene copper structure, copper materials are separated by barrier layer at the bottom of each via. Basically, the metal atom movement is blocked by barrier layer at each via [10]. The discontinuity of atom movement results in void formation since holes cannot be filled.

In our experiment, we limit the stress current to below 15 mA in order to suppress Joule heating. Since the metal resistance increases with temperature and Joule heating increases with metal resistance, this positive feedback between metal resistance and temperature can easily blow out the metal grid. For example, in our test structure, 30 mA current could cause failure immediately after power up.

VI. EM Failure Rate and Order

The previous section focused on the location of the first EM event. In this section, we will analyze the failure rate and failure order of all failures. Due to redundant current paths in a power grid, a single failure event may or may not decide the entire chip's lifetime. Therefore, it is worth studying the failure order.

Four chips were tested under the same stress condition; a constant 10 mA current stress and a current direction of $A + B \rightarrow C$. The failure rate during the entire 50 hour stress period is shown in Fig. 17. For chip #10, the entire curve can be divided into the three regions: (1) Initial period with a relatively low failure rate of 0.71 failures/hour; (2) A high failure rate period with 18.11 failures/hour, possibly due to the higher current density in the unbroken paths. (3) A low failure rate period with 0.79 failures /hour after the voltage compliance level (=2.5 V) of the sourcemeter equipment is reached. Stress current decreases gradually with more EM events under constant voltage stress, resulting in a low failure rate. Similar failure rate trends were observed in the four tested chips, as shown in Fig. 17 (bottom).

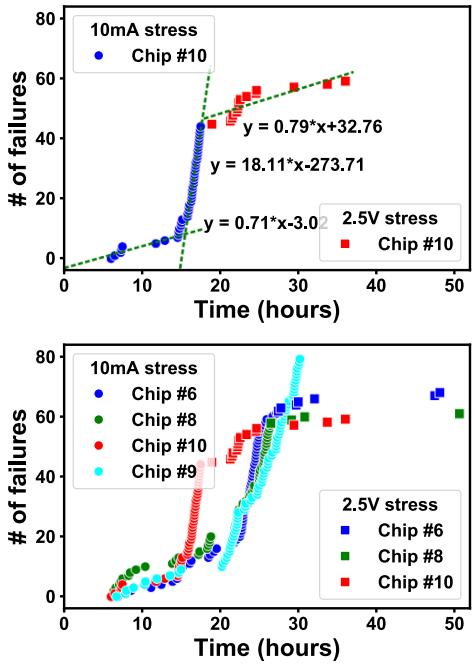

Fig. 17. (Top) Failure rate of chip #10 and (bottom) four tested chips. The failure rate changes from slow to fast (under constant 10mA stress) and then back to slow (under 2.5V constant voltage stress) for all tested chips.

Next, we analyze the correlation between subsequent failures in the same chip. One hypothesis is that failure at one location may trigger the failure in a nearby location due to the current flow reconfiguration. Fig. 18 displays the failure order of a power grid. It indicates that the failure can happen across the entire power grid, while there is almost no correlation between consecutive failures in time. In other words, the failure location is unpredictable. Fig. 18 (bottom) compares the results from different chips, limited to the first five failure locations for clarity. We observe no consistent behavior between different chips. One interesting observation is that the first five failure always happened close to the negative voltage terminal or on edges. Those locations usually have a larger local current density due to current concentration and tensile mechanical stress from barrier layer blocking effect. In modern dual-damascene copper technology, barrier layer is adopted to separate metal traces in different layers. When a void is formed at one side of the barrier layer due to mechanical tensile stress, metal atoms at the other side of the barrier layer are unable to fill the vacancies. Therefore, EM void usually appears at the via where traces are separated by barrier layer.

VII. CONCLUSION

In this paper, we present EM results measured from a 9×9 power grid test structure fabricated in a 65 nm technology. Unlike single wire EM structures, power grid EM events are hard to track due to the numerous internal voltages. In this work, we were able to detect EM events in every individual power grid segment using the voltage tapping technique. An on-chip heater was used to keep the DUT temperature at 350 °C during both stress and measurement modes. $9 \times 9 \times 2 = 162$

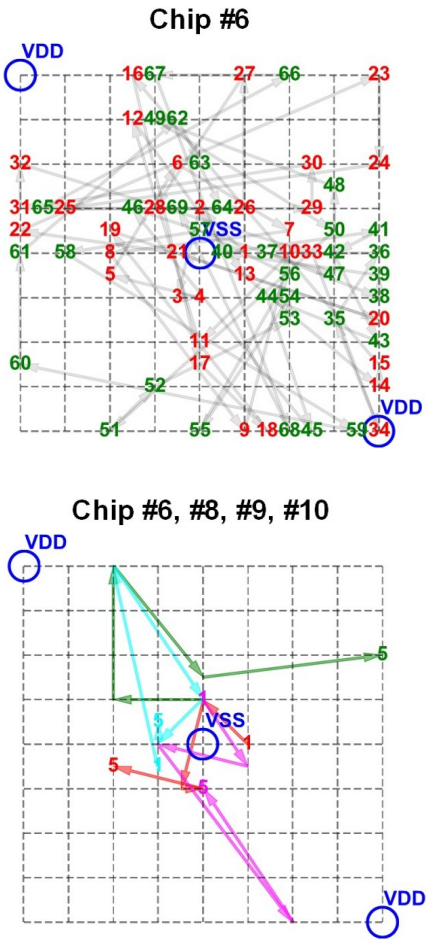

Fig. 18. (Top) The full failure order of chip #6 and (bottom) the first five failures of chips #6, #8, #9 and #10 showing relatively random behavior.

voltages from the power grid were sampled every 133 seconds, allowing us to capture detailed changes in the individual voltages. Abrupt failure, progressive failure, and healing were observed in our experimental data. Note that EM healing was easily observed in our power grid structure possibly due to the redundant current paths. We believe the lifetime of an actual power grid is longer than what conventional predictions due to healing effect. For the four chips we measured, the location of the first EM event was always near the negative voltage terminal, which suggests the presence of mechanical backstress. Failure rate was found to be a strong function of the stress current density. Although early failures always occurred near the negative voltage terminal, the location of the subsequent failures were unpredictable and relatively random.

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