Investigating the Aging Dynamics of Diode-connected MOS Devices using an Array-based Characterization Vehicle in a 65nm Process

Nakul Pande, Gyusung Park, Srikanth Krishnan†, Vijay Reddy† and Chris H. Kim

University of Minnesota, Minneapolis, MN, USA
†Texas Instruments, Dallas, TX, USA

nakul@umn.edu

Purpose

- **Comprehensive reliability characterization of the diode-connected MOS**
- **Decouple, and hence comparatively quantify the impact of feedback**
- **Evaluate the efficacy of iterative simulation frameworks for aging prediction in such scenarios**

Outline

- Introduction
- 65nm Array-based Characterization Vehicle
- Measurement Methodology
- Measurement Results
- Lifetime Prediction Efficacy
- Conclusion

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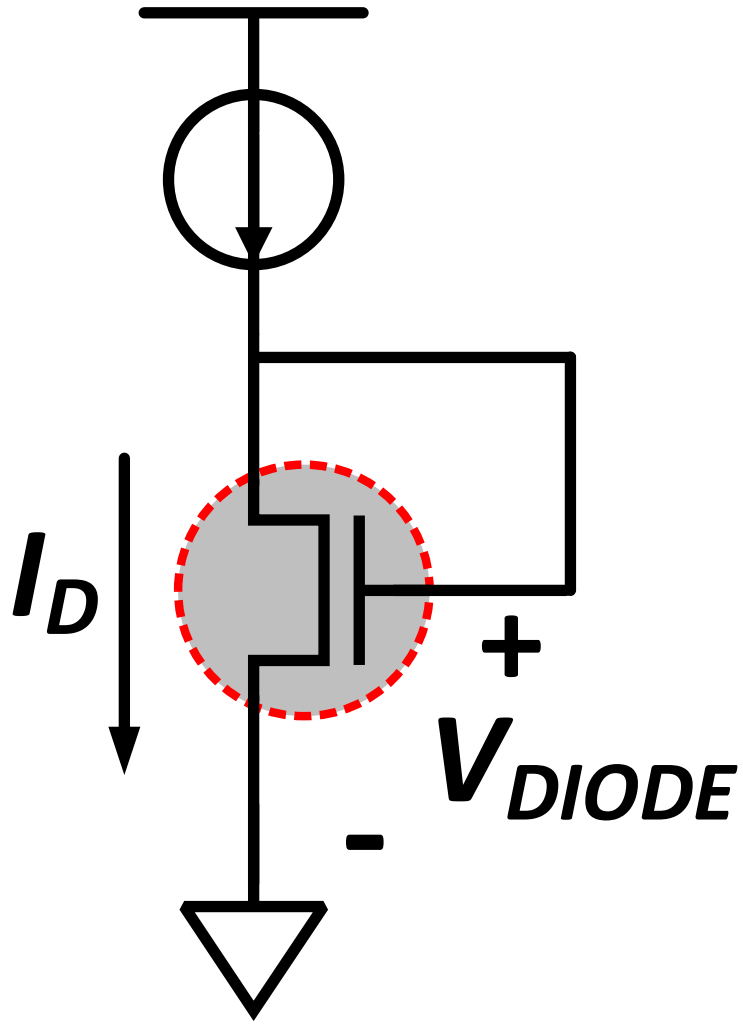
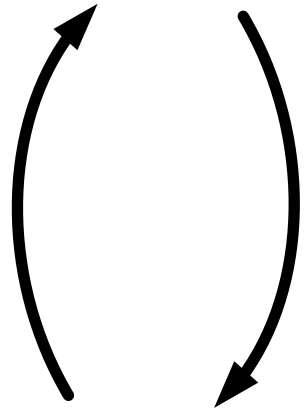
Accelerated Aging With Feedback

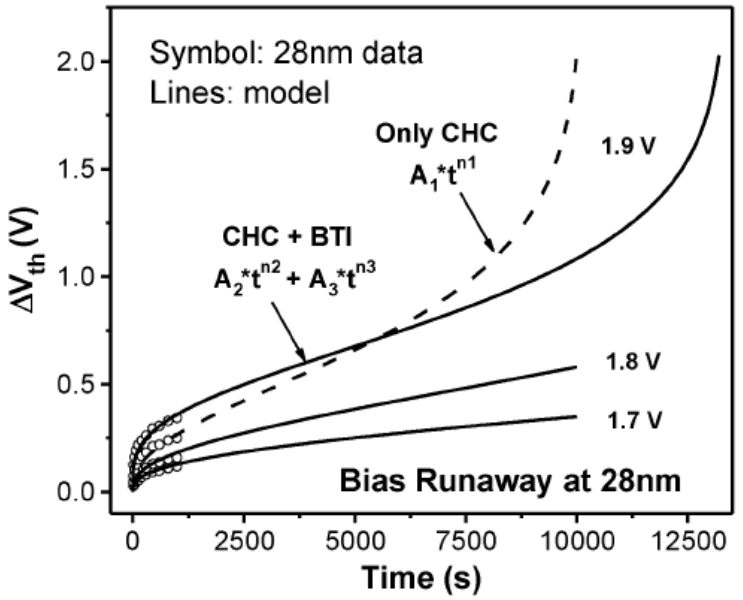


ΔV_{th} (*HCI Aging*)

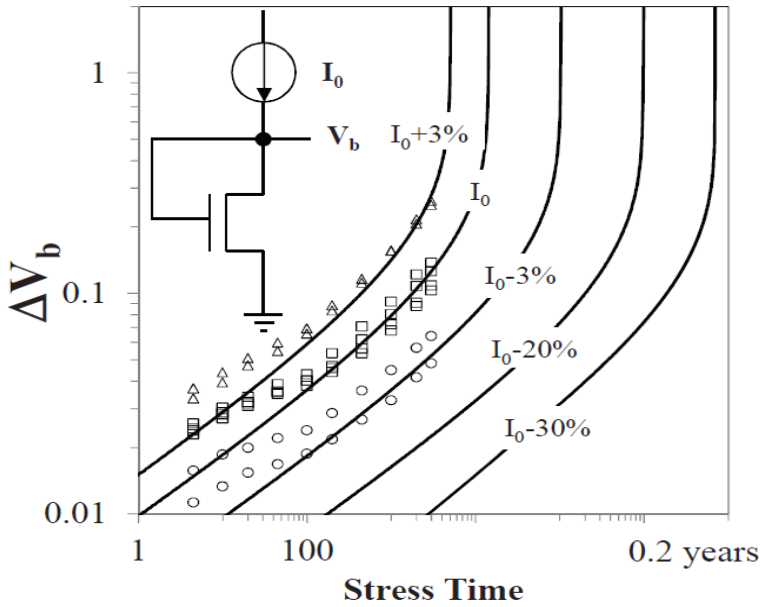


ΔV_{DIODE}

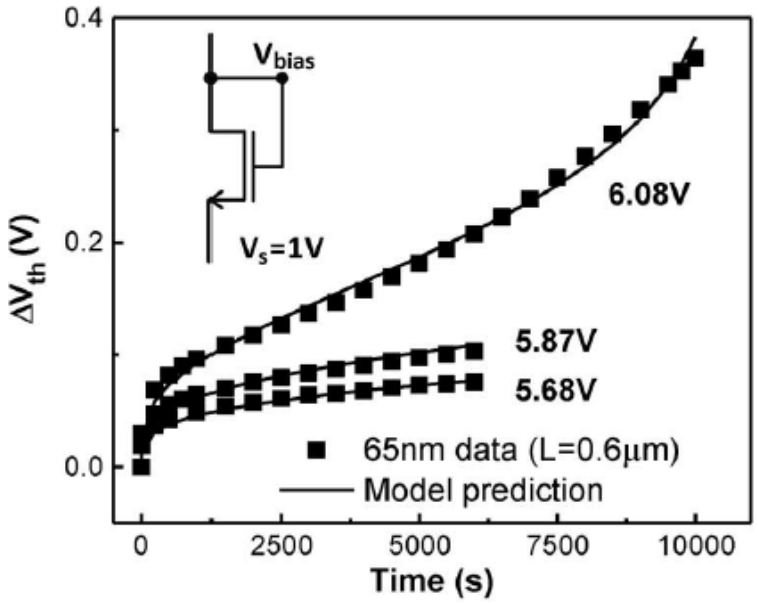
Prior Art: Diode-connected MOS



K. B. Sutaria et. al., TDMR, '15



V. Huard et. al., IEDM, '15



K. B. Sutaria et. al., IRPS, '14

- **Lack of comprehensive test-data does not clearly specify the extent of model fit**
- **Does a '$V_{Critical}$' actually exist beyond which accelerated and below which only gradual aging occurs?**

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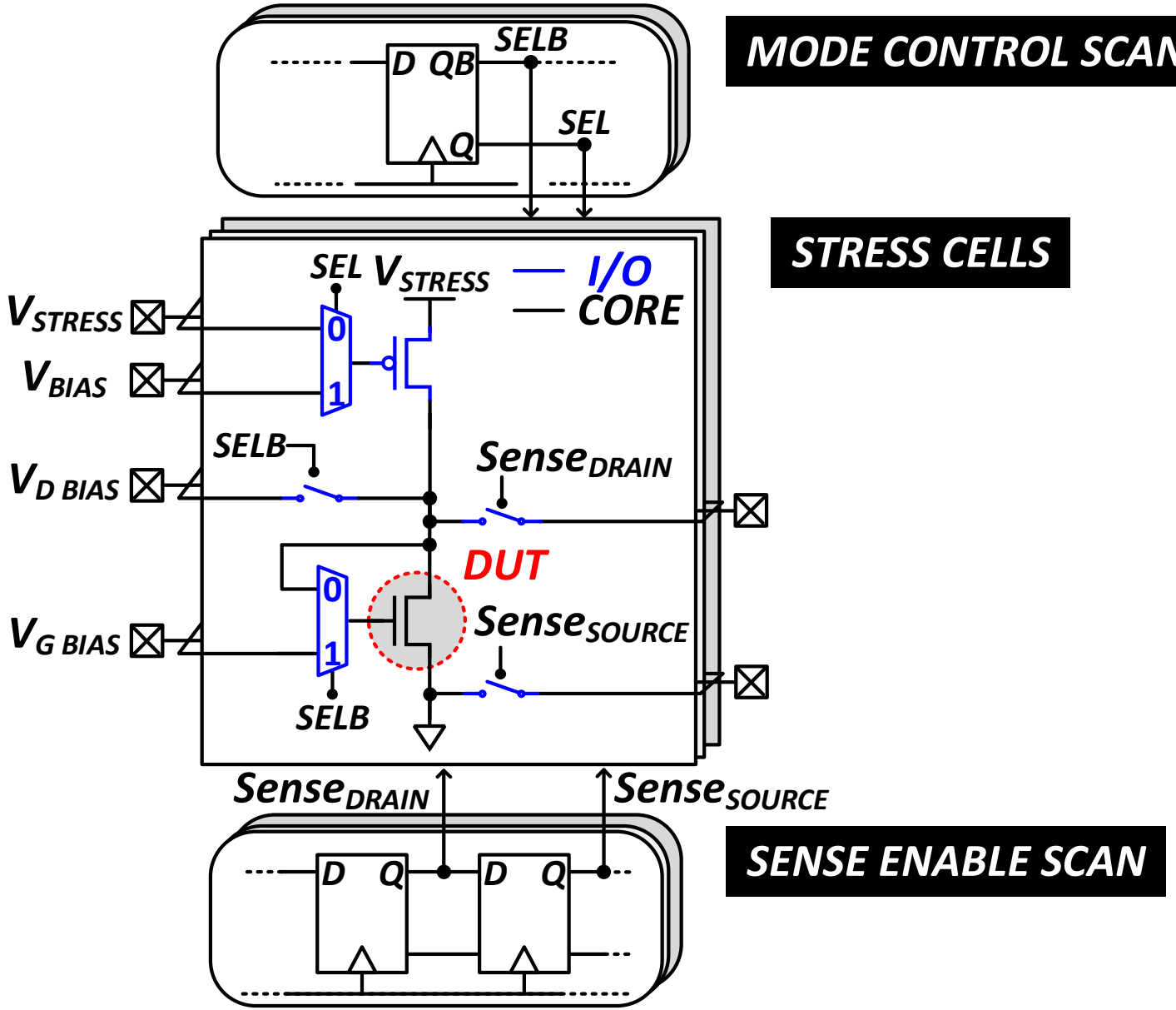
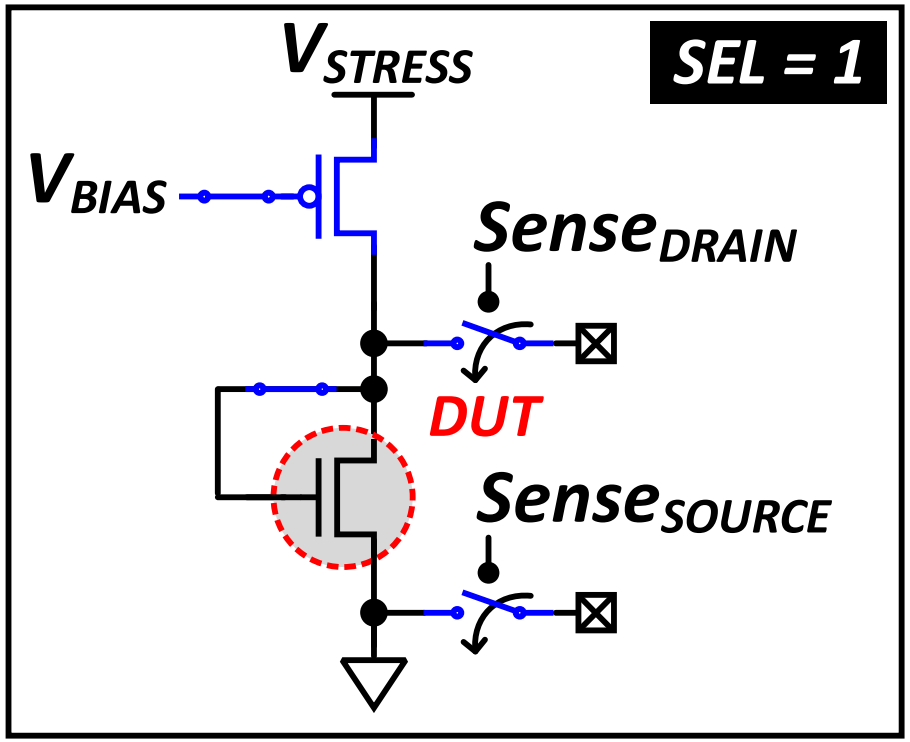
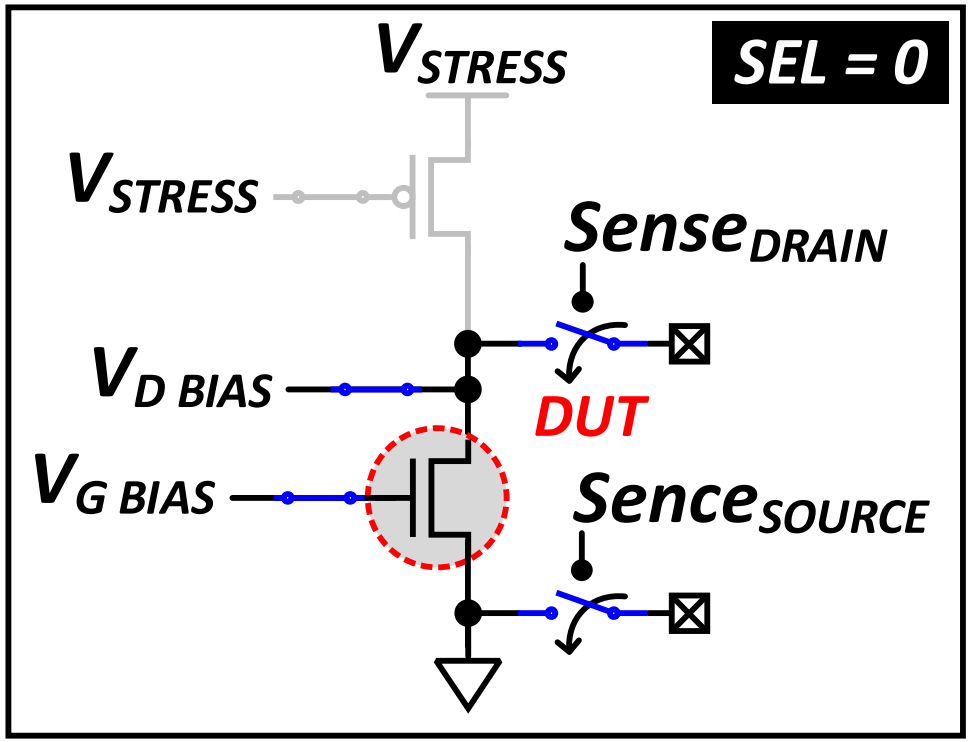
Stress Cell Specifics



Operation Modes

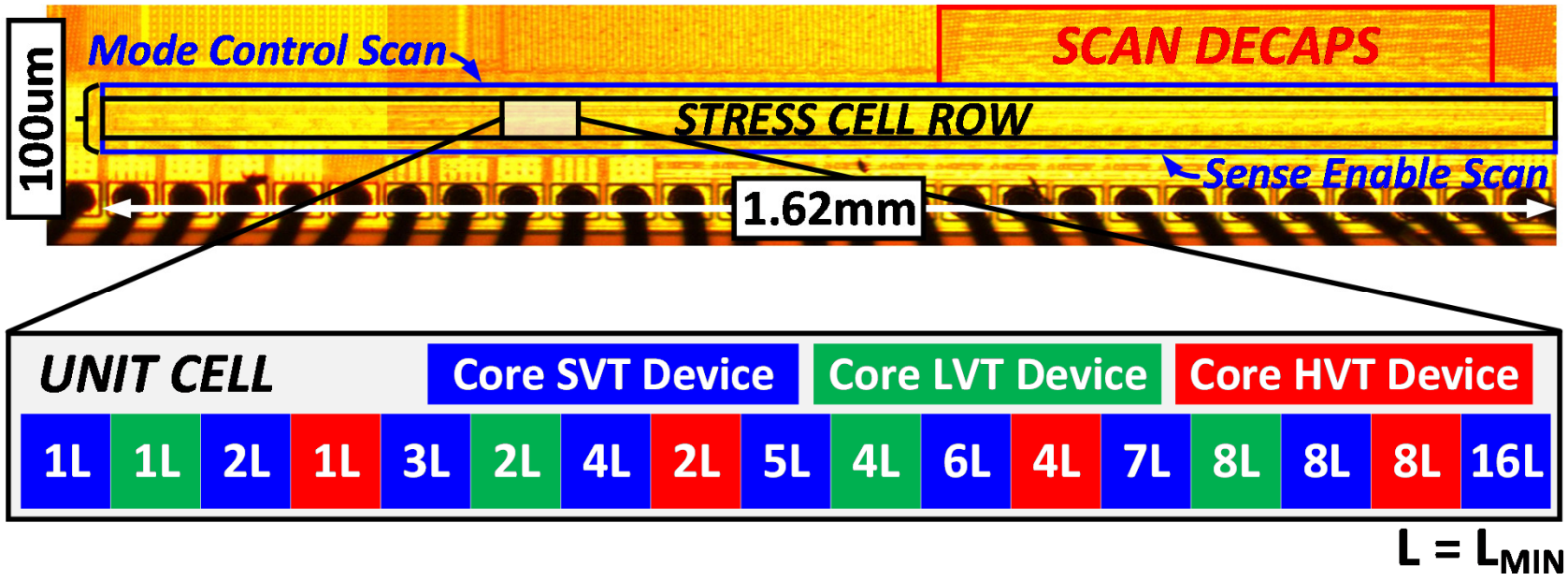


'STRESS' MODE



'IDLE' MODE

65nm Die-Photo & Implementation Detail



Technology	65nm LP Bulk
Core VDD	1.2V
I/O VDD	3.3V
Core + Test Area	0.1mm x 1.62mm
Cell Area	9.2um x 24.5um
DUT Count	192
DUT Widths	350nm
L_{MIN}	60nm

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- **Measurement Methodology**
- Measurement Results
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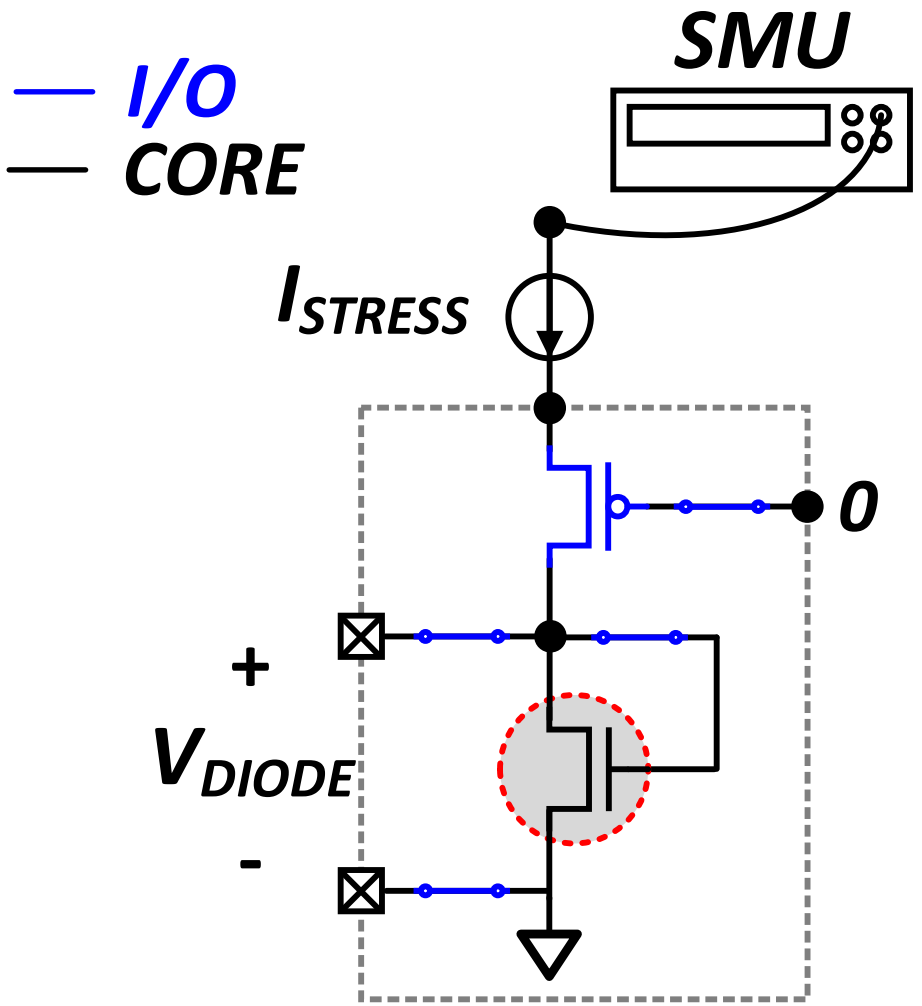
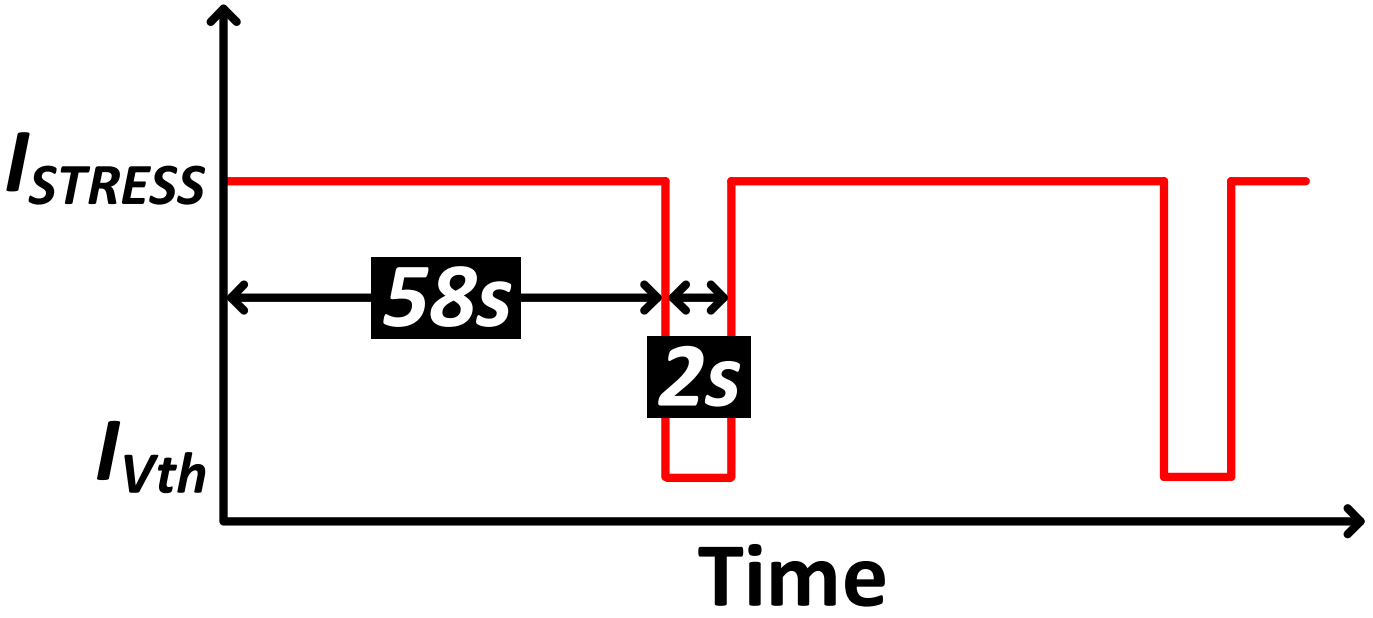
Constant Current Stress

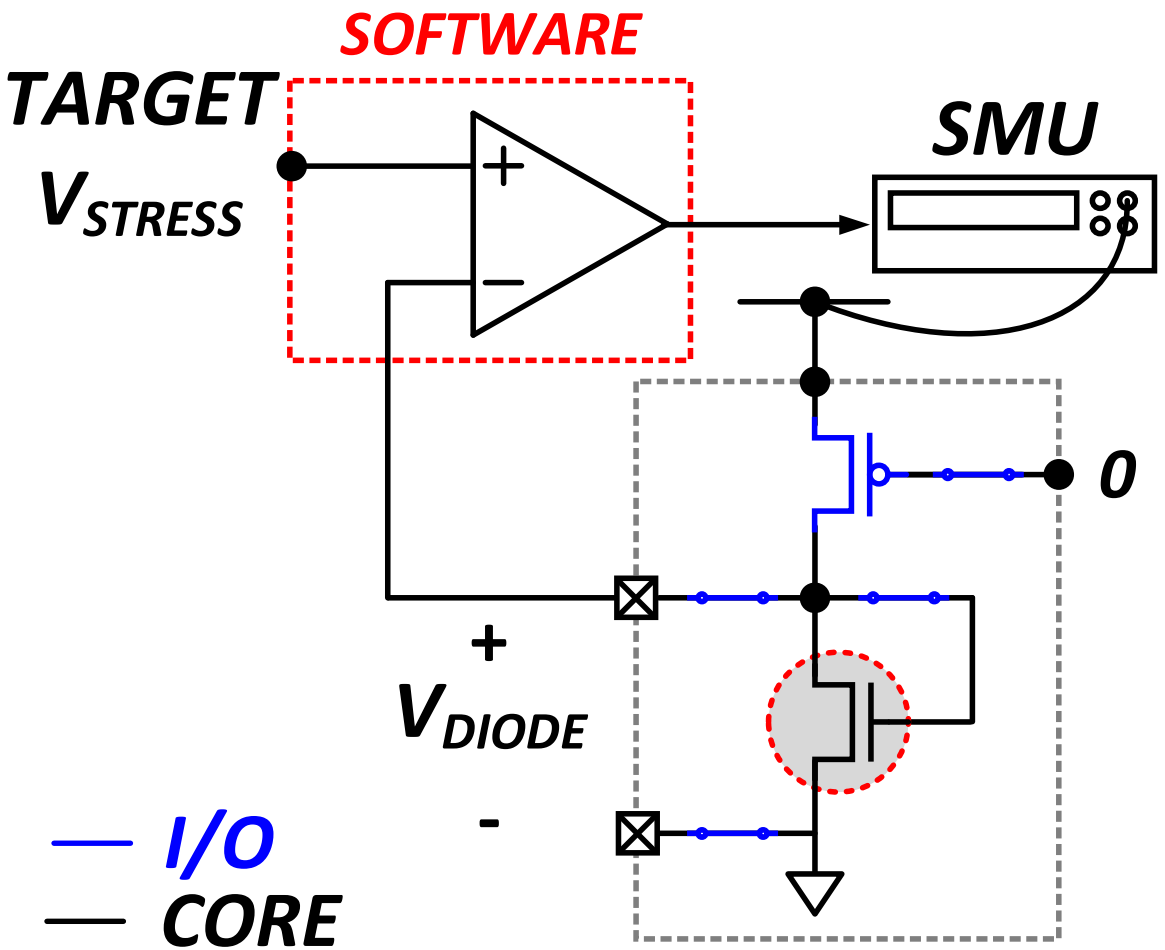


Ⓐ Stress with DUT in Feedback

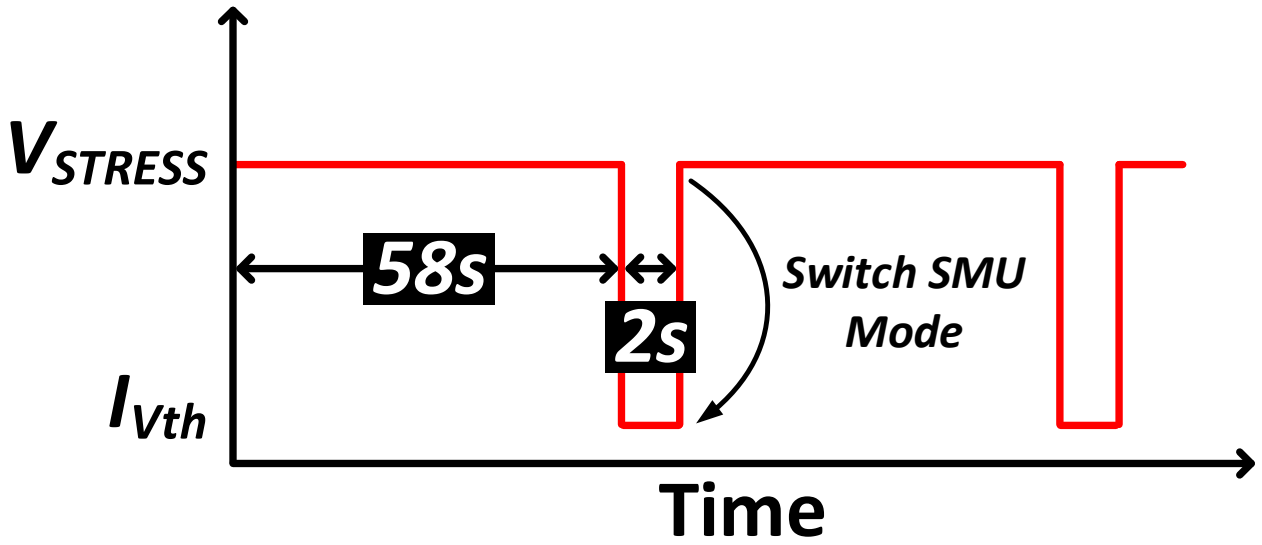


Ⓑ Stress-Measurement Cycle

Constant Voltage Stress

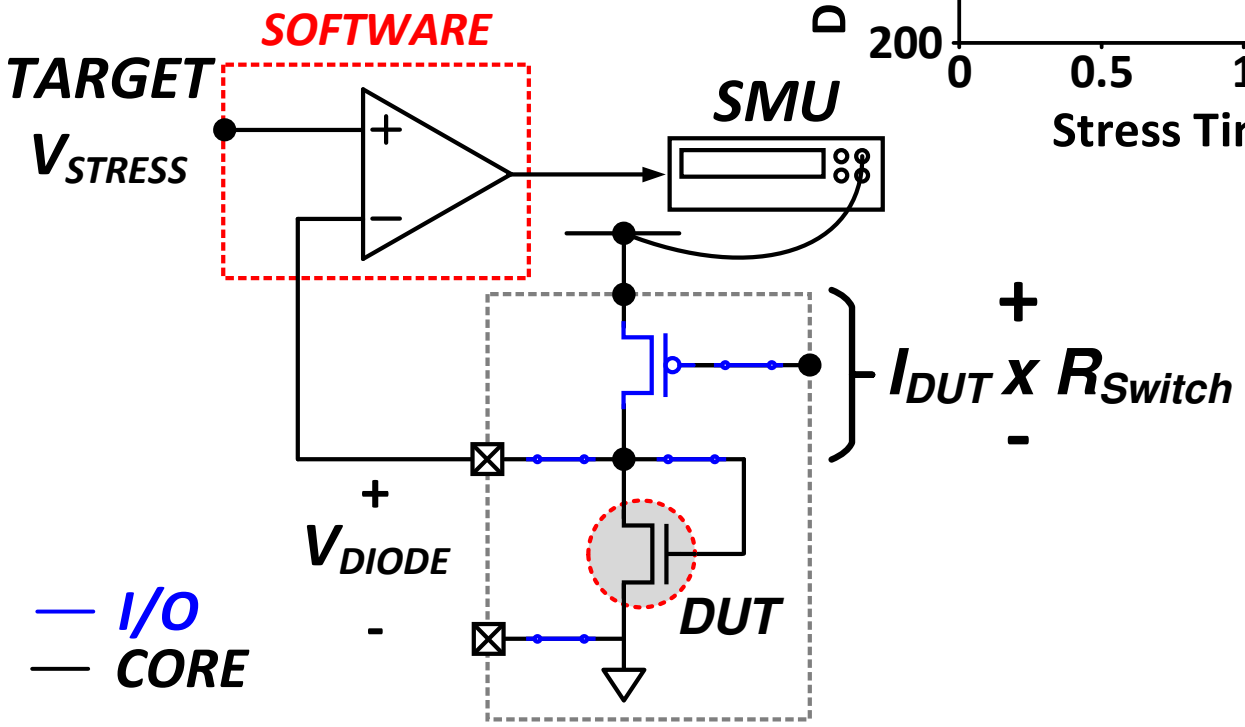


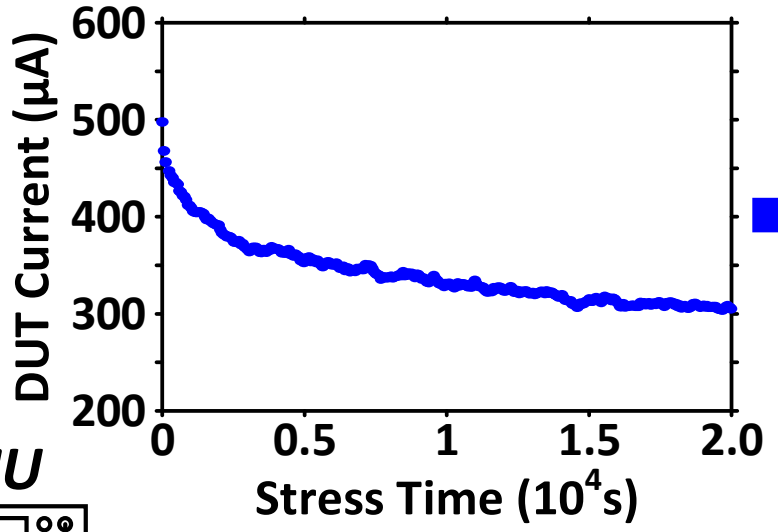
A No-Feedback Stress

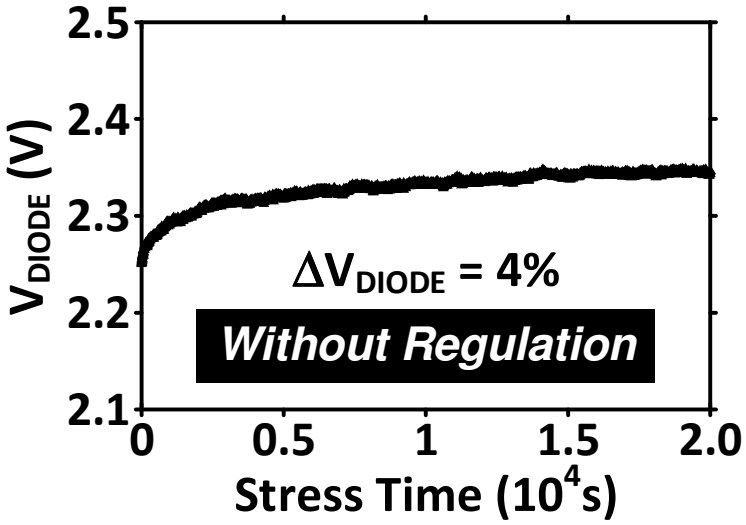


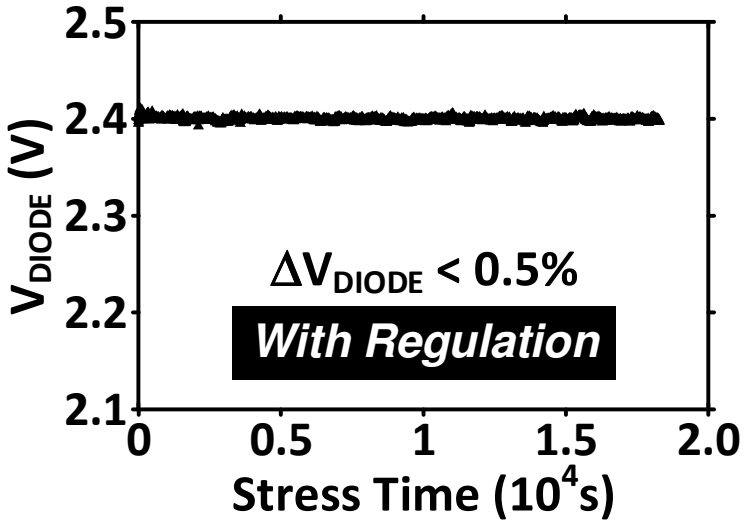
B Stress-Measurement Cycle

Need for Regulation for Constant Voltage Stress Case

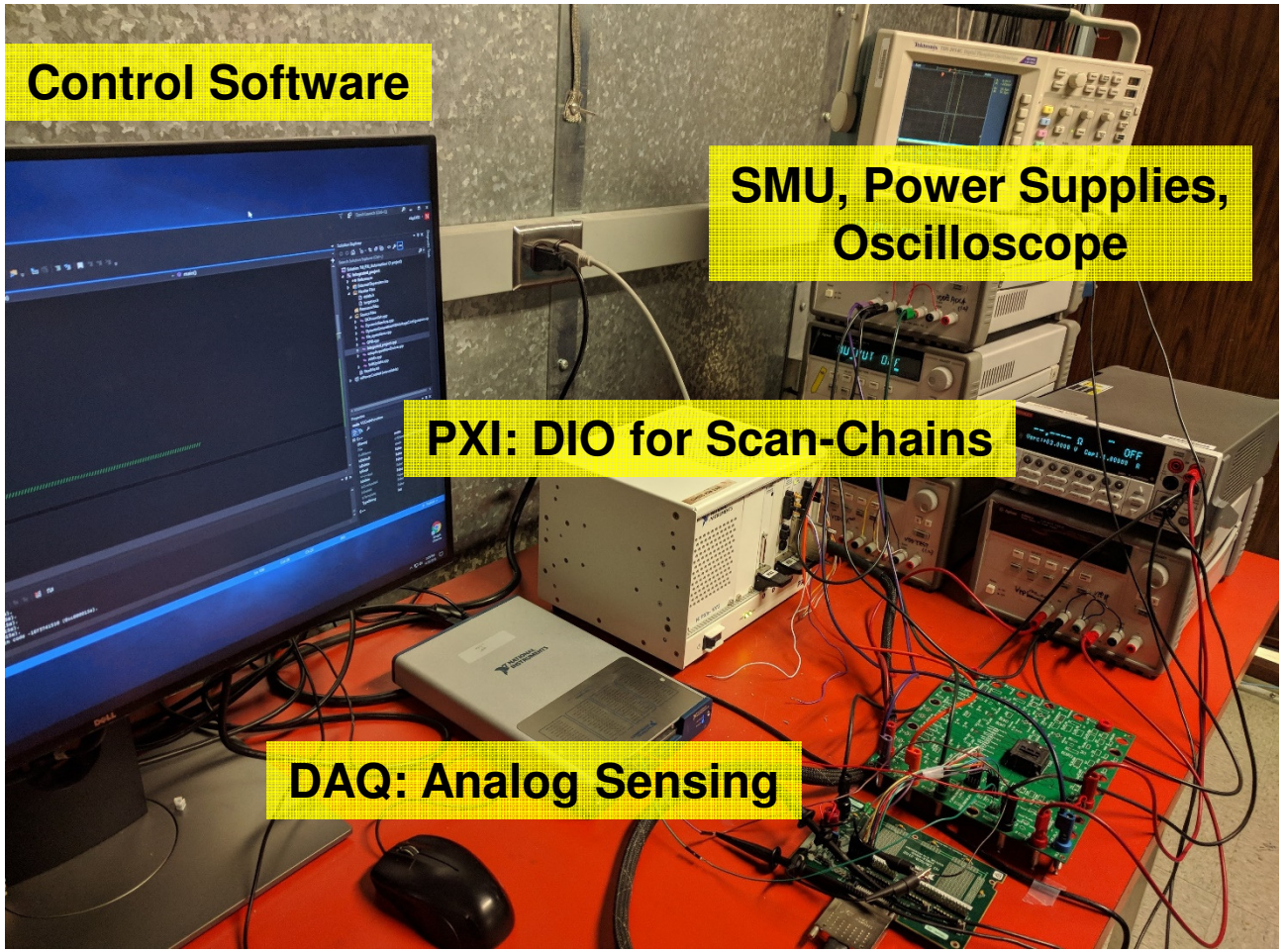




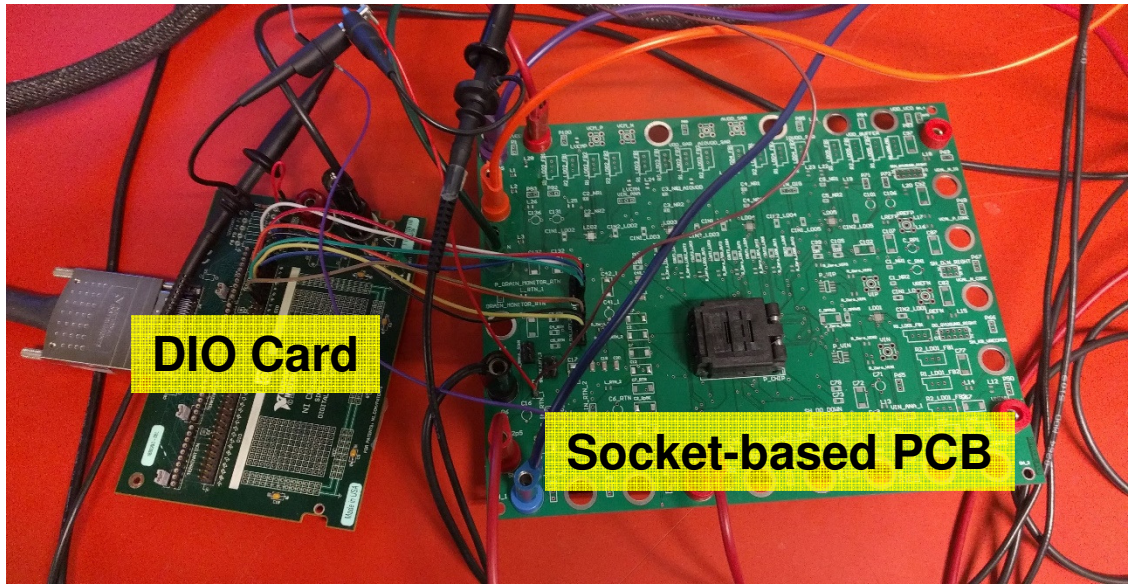




Measurement Setup



A Measurement Environment



B 65nm Test-Chip Interface

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- **Measurement Results**
- Lifetime Prediction Efficacy
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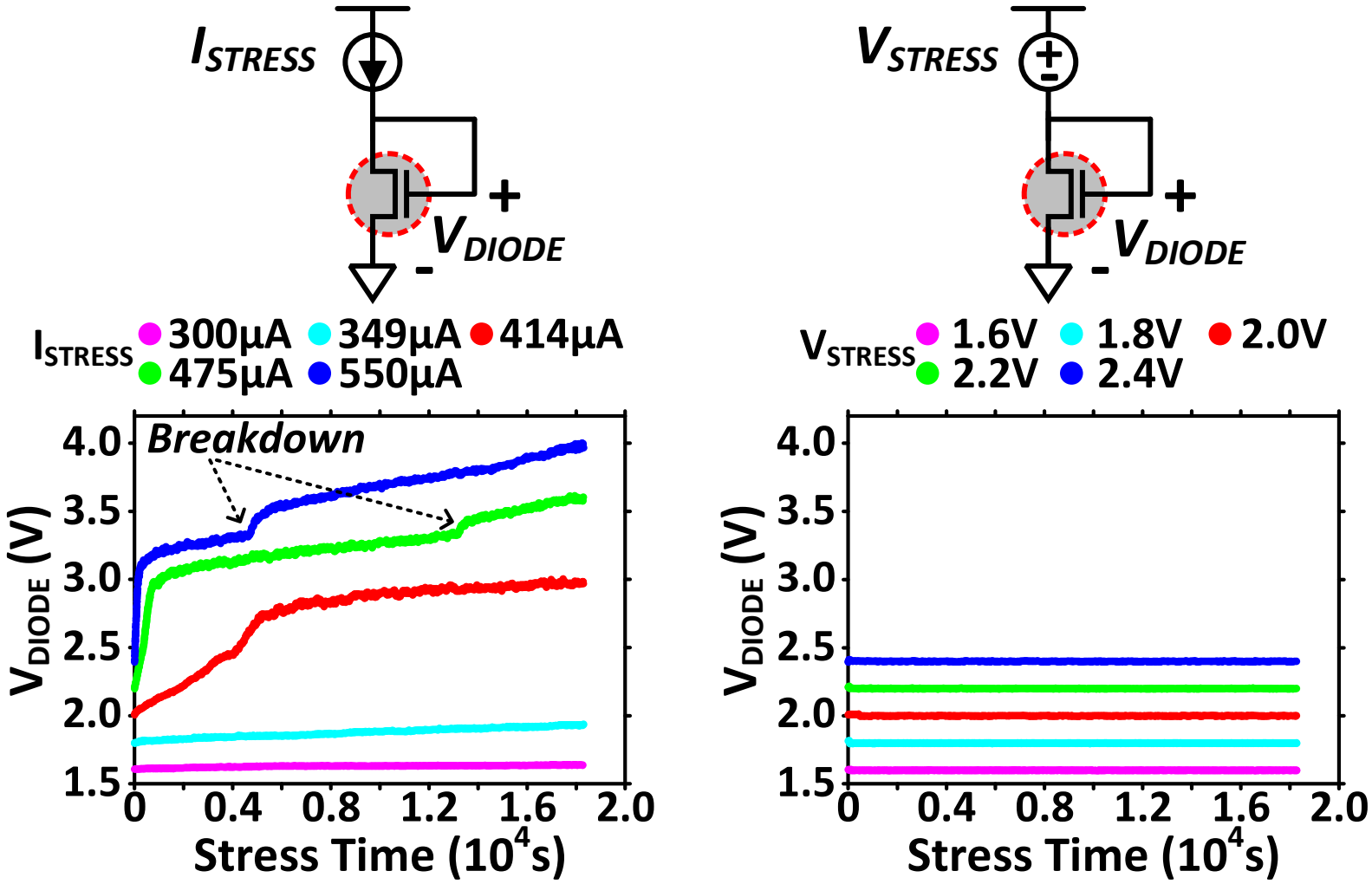
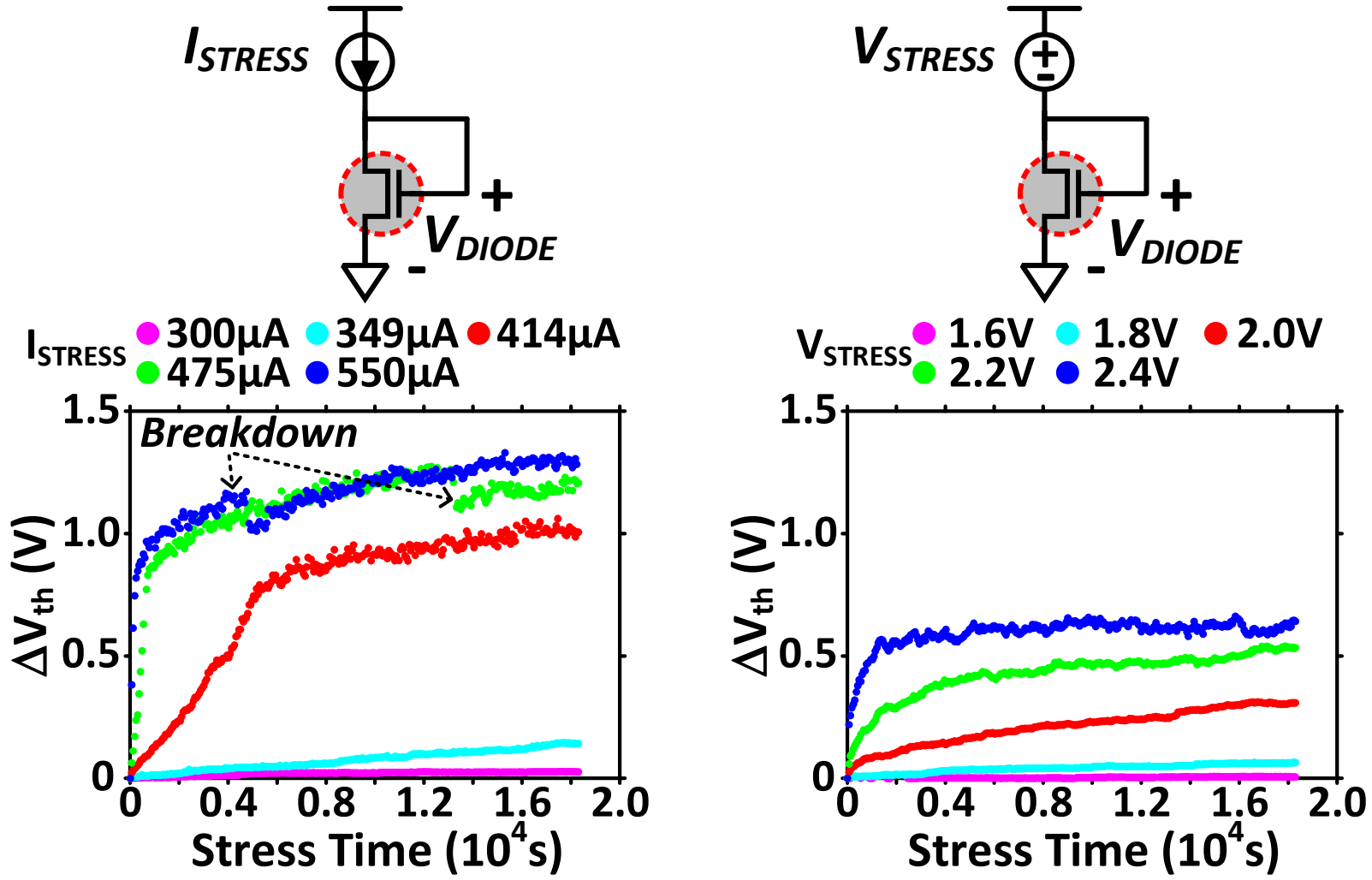
Measured V_{DIODE}



L_{MIN} HVT DUT, 25°C

- **Stress condition (V_{DIODE}) varies with time for feedback**

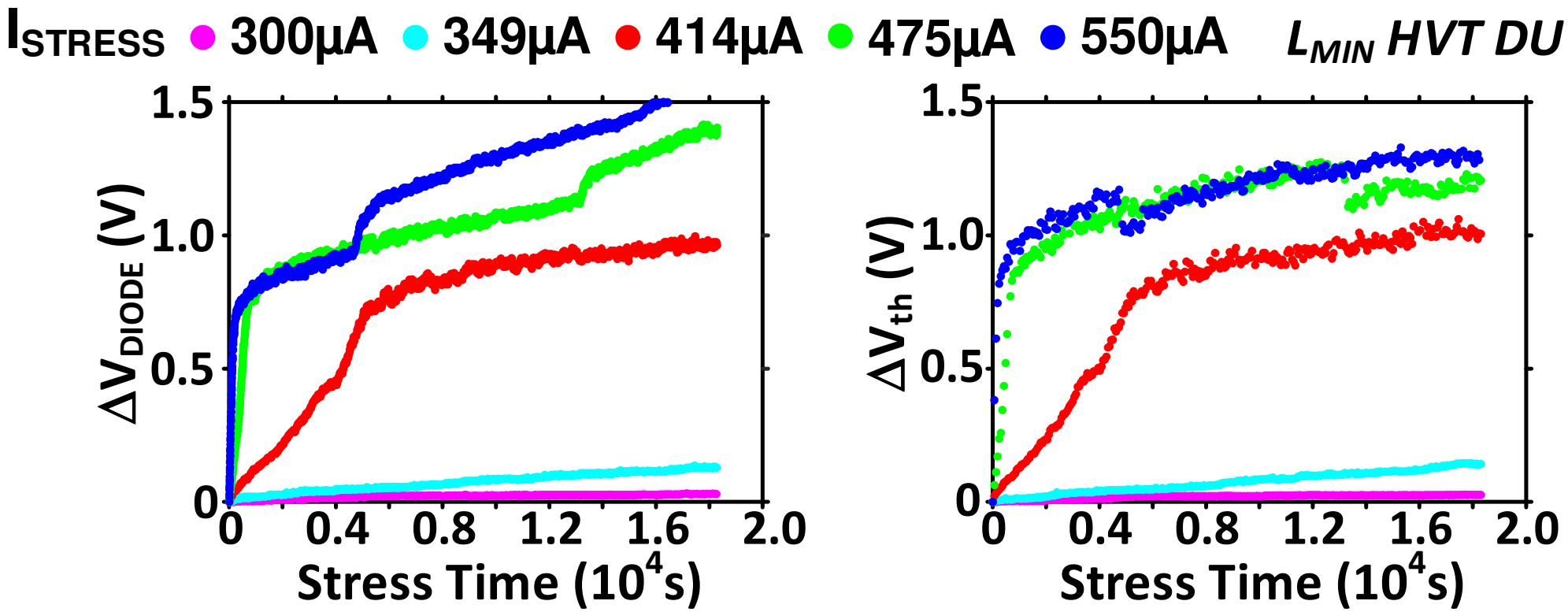
Measured V_{th}



L_{MIN} HVT DUT, 25°C

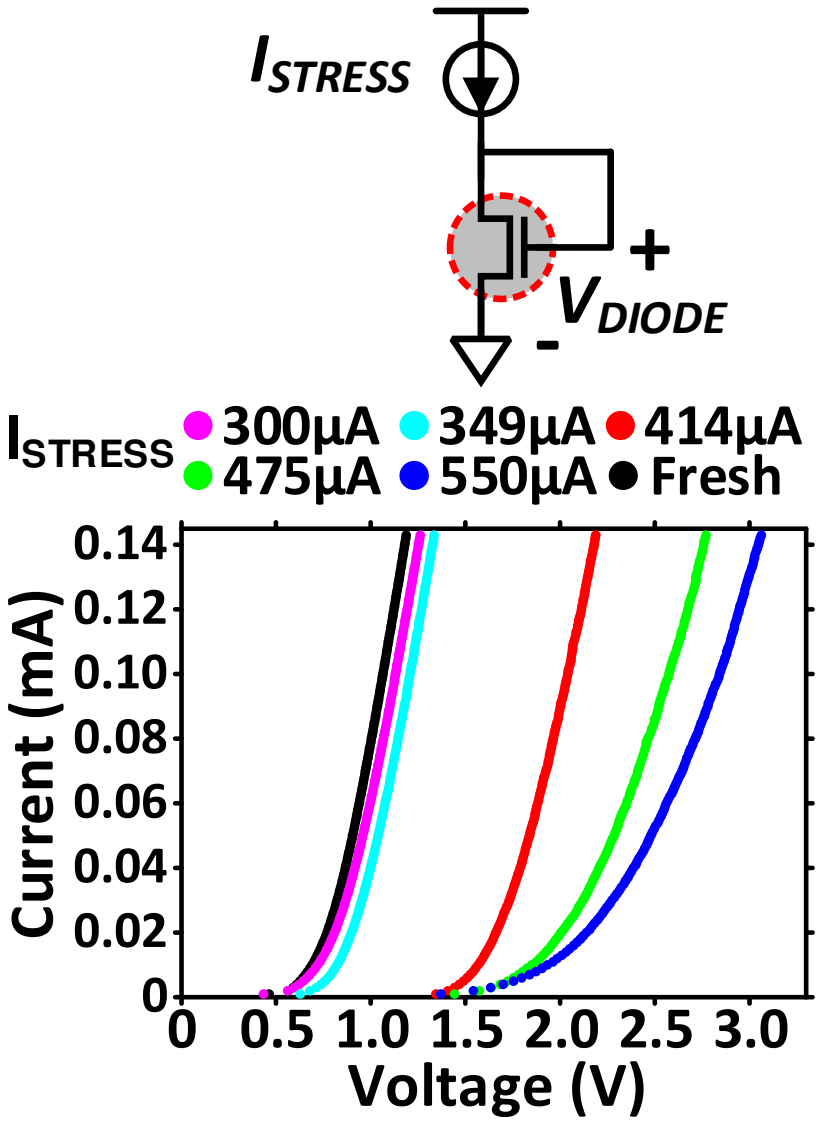
- **Time varying V_{DIODE} → Pronounced aging in feedback**

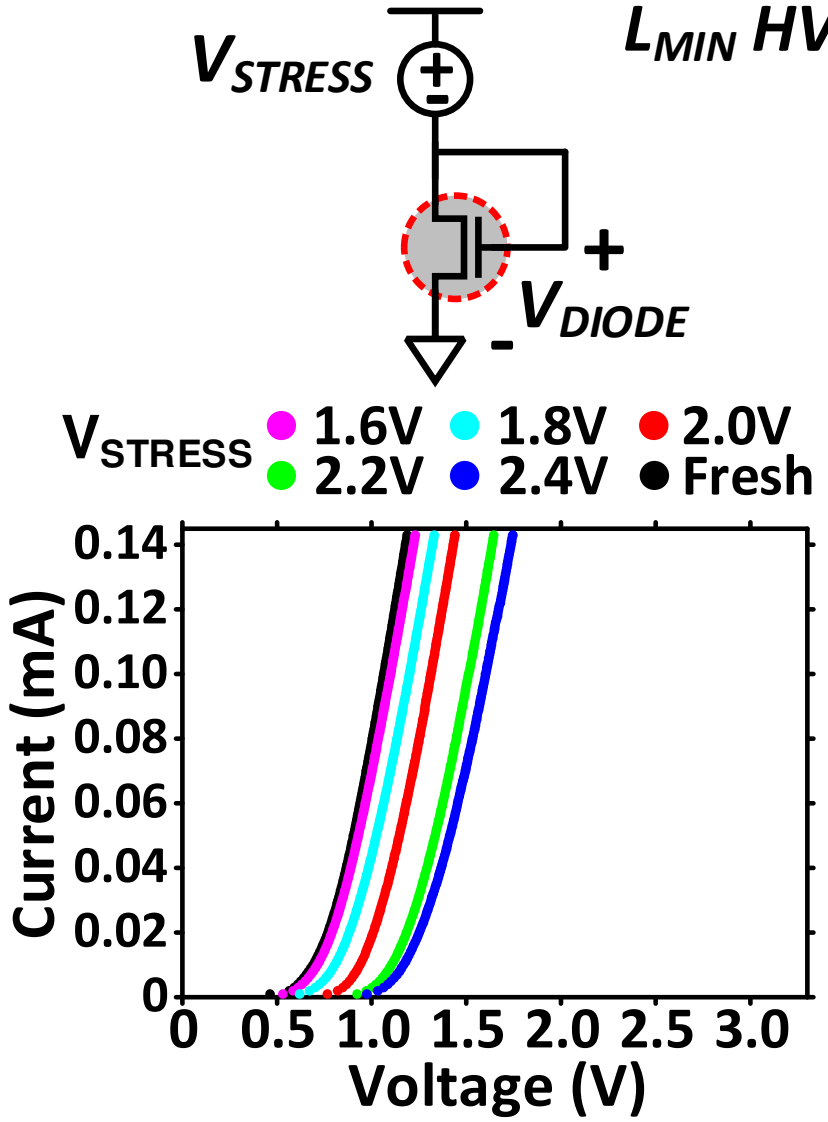
ΔV_{DIODE} vs. ΔV_{th}



- Shift in V_{DIODE} closely tracks the shift in V_{th}

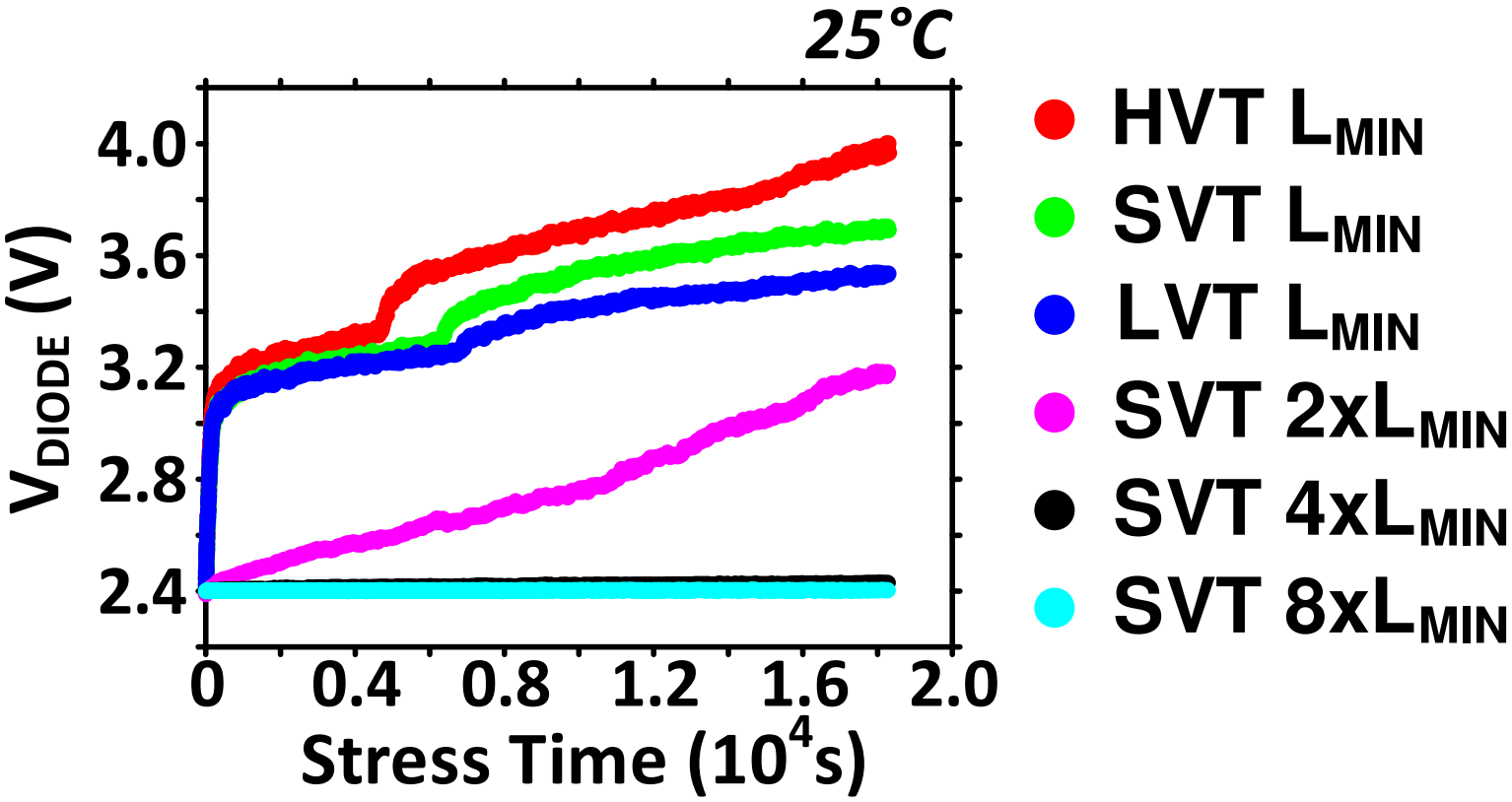
Measured Post-Stress I-V





L_{MIN} HVT DUT, 25°C

V_{DIODE} : Other DUT types



- Similar aging trends observed for L_{MIN} V_{th} variations
- Improved resilience for longer L DUTs

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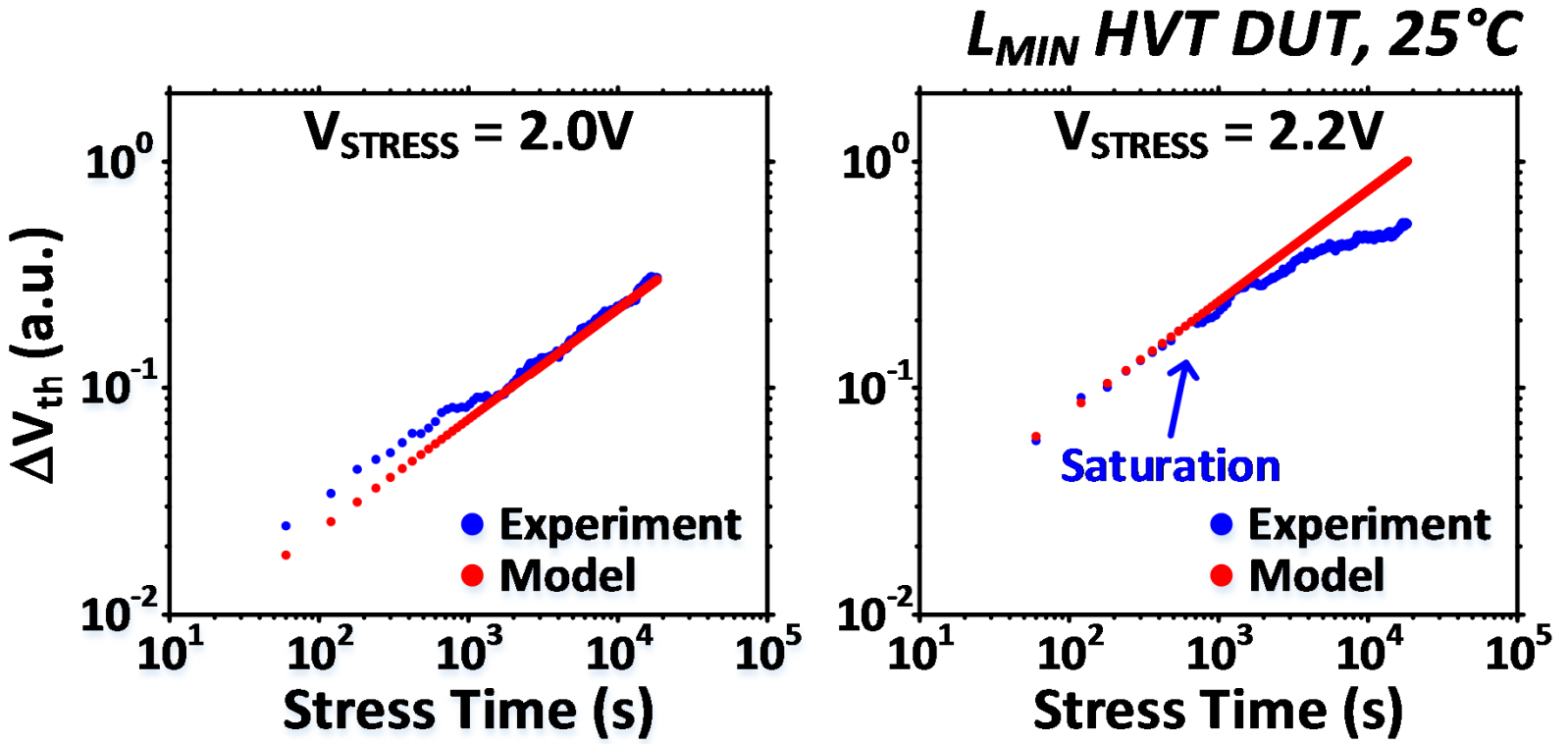
Modeling Constant Voltage Stress



$\Delta V_{th} = At^n$,

$A = k \times \exp(-B/V_{DIODE})$

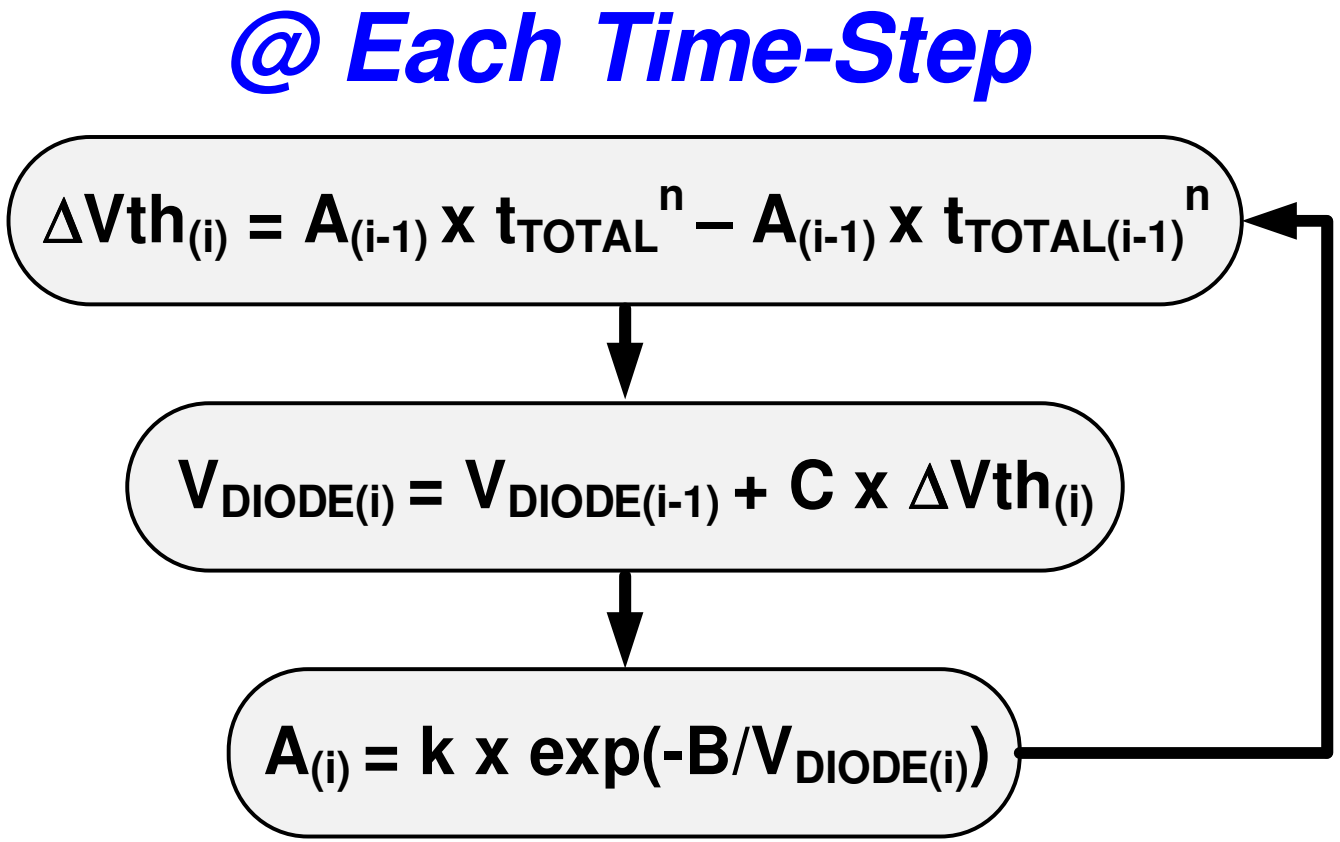
n = 0.49, B = 26.5, k = 1400

E. Takada et. al., EDL, '83

☺ Constant power law models provide reasonably good fits

☹ However, fail to account for saturation at higher V_{STRESS} or longer t_{STRESS}

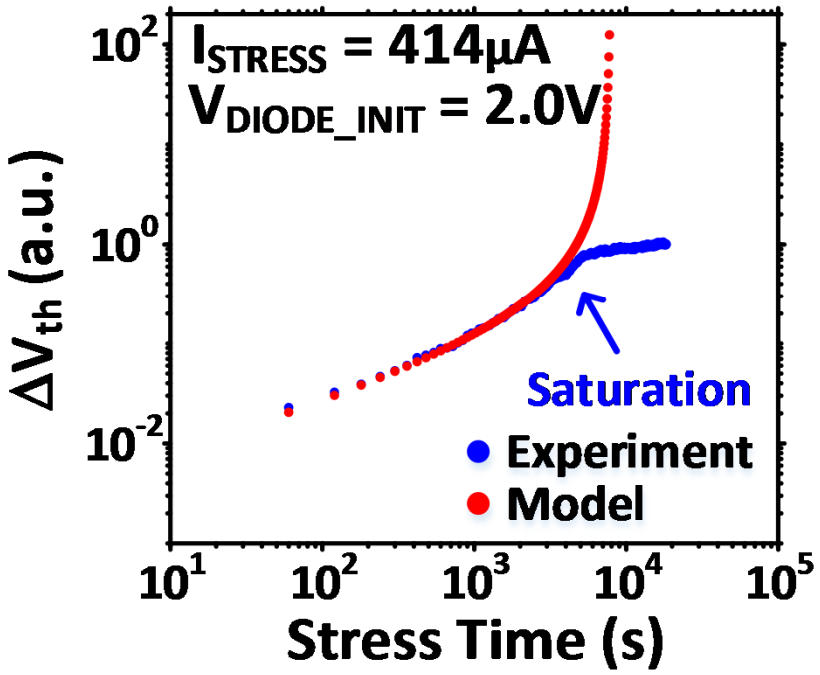
Iterative Flow for Constant Current Stress

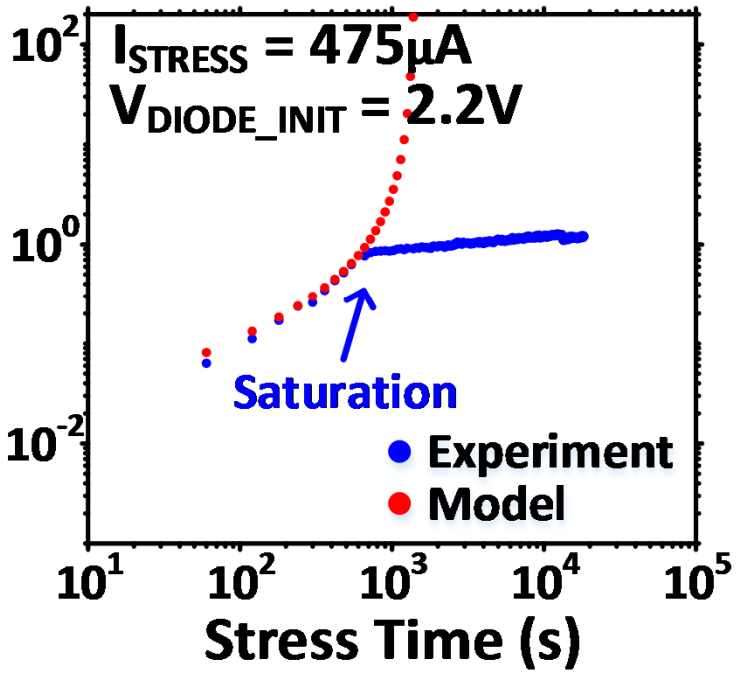


- Identical constants (k, B, n & A_0 = A) as constant voltage stress
- Stress condition (V_{DIODE}) updated iteratively at each simulation time step (= *60s,* as in measurement)

Aging Prediction

L_{MIN} HVT DUT, 25°C





$\Delta Vth = At^n$,

$A = k \times \exp(-B/V_{DIODE})$

$V_{DIODE} = V_{DIODE} + C \times \Delta Vth$

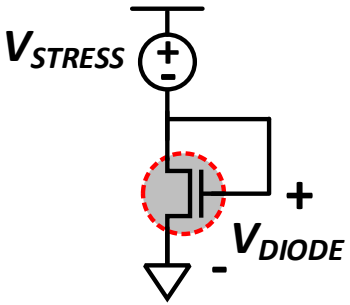
n = 0.49, B = 26.5, k = 1400, C = 0.93

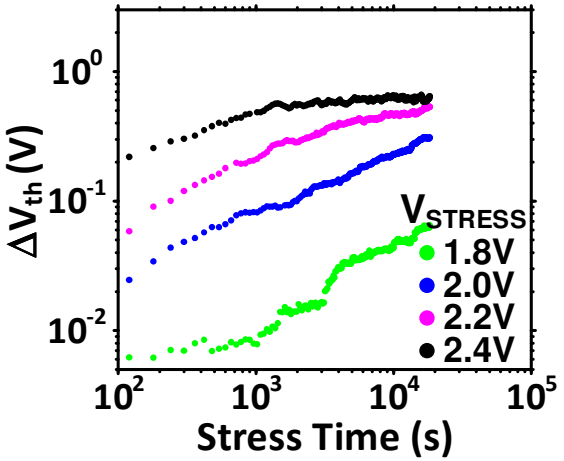
☺ Accurate fit to initial super-exponential aging trend

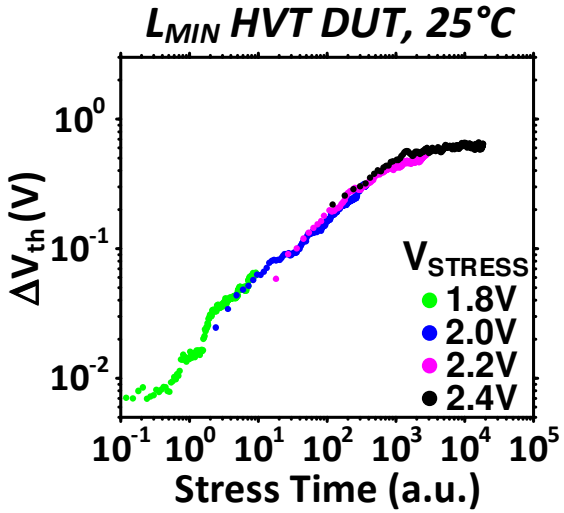
☹ Failing to account for onset of saturation in feedback →

<u>Severely limited fit owing to faster aging</u>

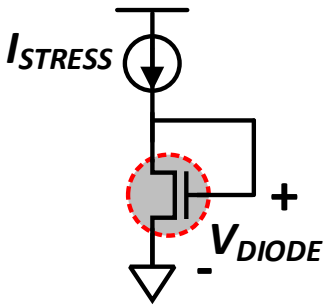
Using the Method of Universality of Degradation for Accurate Aging Prediction

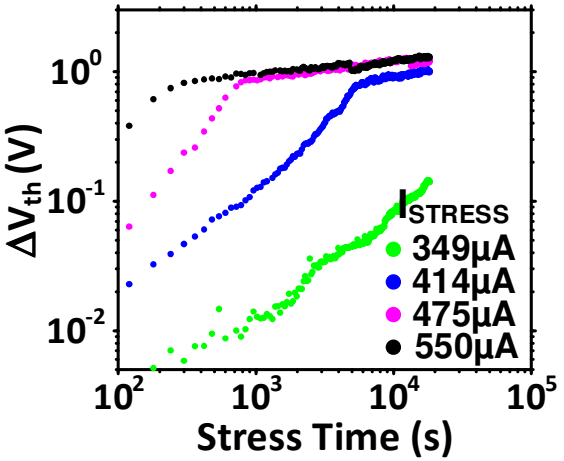


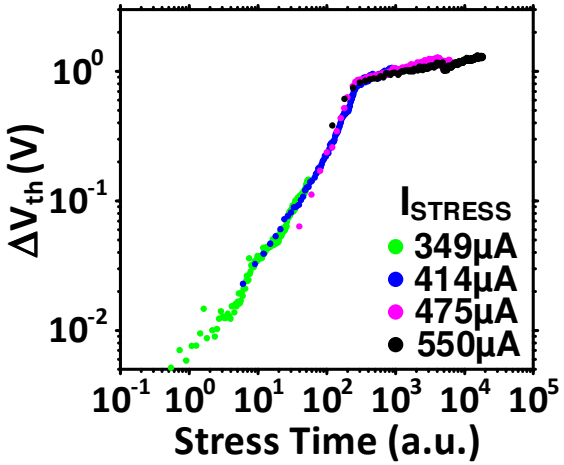




D. Varghese et. al., IRPS, '10

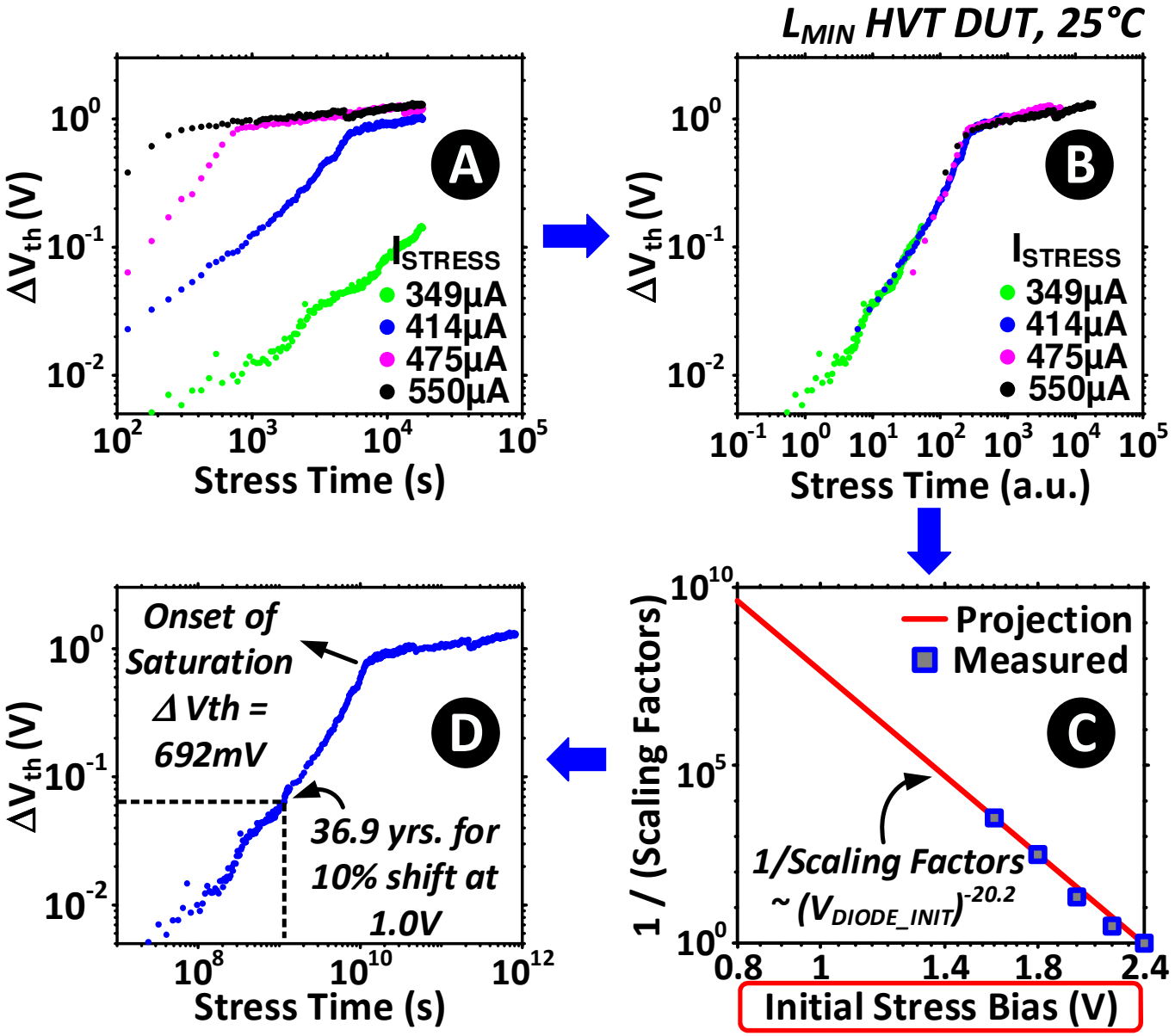






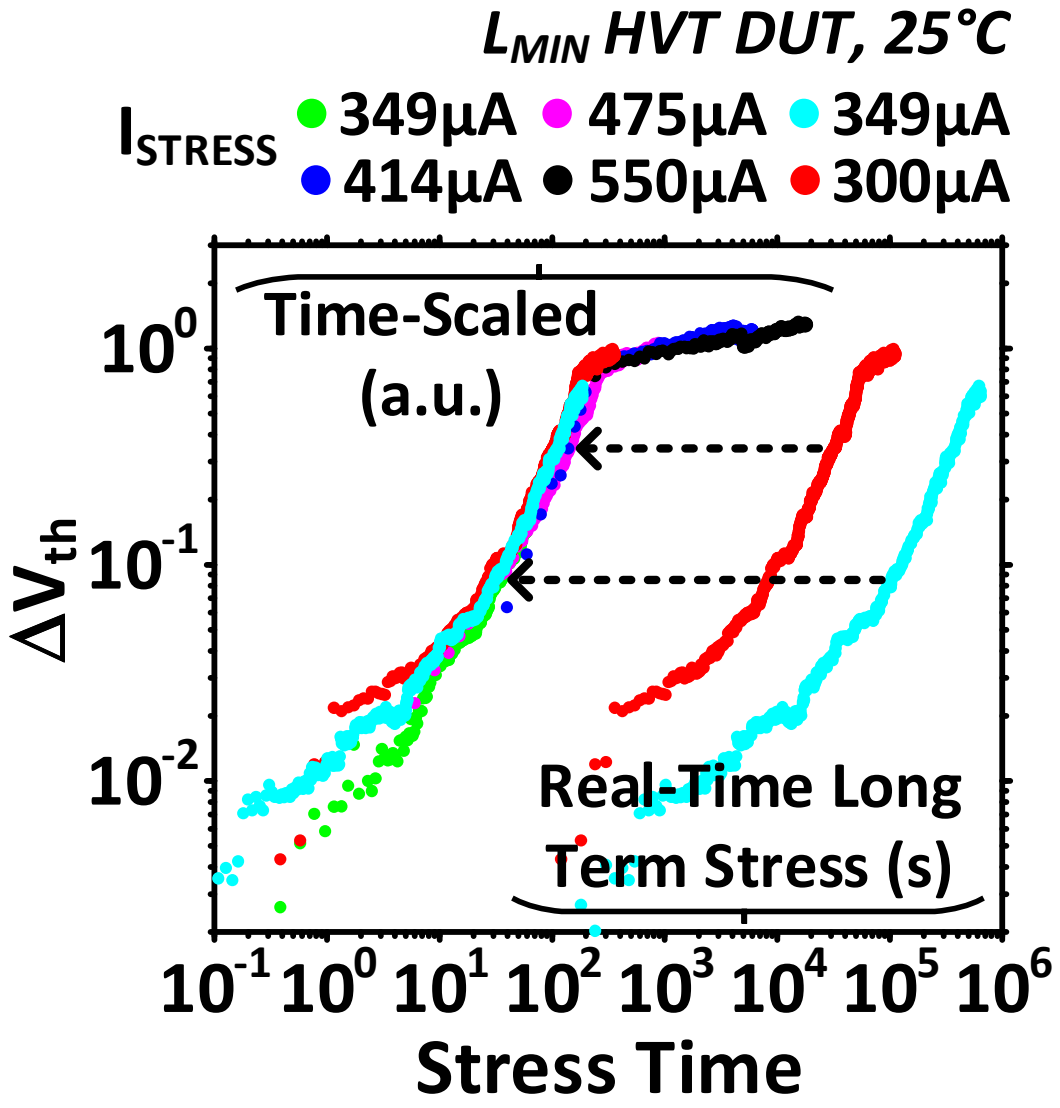
Universality holds for time-varying stress case as well ☺

Application to Constant Current Stress



- Initially developed stress bias serves as a reference for aging prediction
- Accurate aging prediction including onset of saturation
- Even fewer short term stress measurements on account of accelerated aging in feedback

Long-Term Stress Results



- Long-term measurements fit well to short-term stress derived scaling factors
- Temporal universality points to absence of '$V_{Critical}$'
- Risk of significant deviation in bias maintained, even for lower initial stress biases

Conclusion

- Diode-connected MOS reliability characterized from 65nm test chip
- Iterative simulation frameworks that don’t account for saturation provide limited fits in scenarios where aging is accelerated
- Temporal universality of degradation can be used for estimating full aging behavior