Investigating the Aging Dynamics of Diode-connected MOS Devices using an Array-based Characterization Vehicle in a 65nm Process

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***Abstract*— This work presents measured test-data corresponding to a comprehensive reliability characterization of diode-connected MOS transistors. An array-based test structure, with the specific aim of quantifying the impact of feedback on the aging dynamics for the circuit configuration of interest was designed and implemented in a 65nm Low-Power (LP) process. Through detailed measurement data obtained using the test-vehicle we, (1) characterize the impact of feedback on the aging rate and compare it to the no-feedback case & (2) evaluate the efficacy of iterative simulations for lifetime projection in such scenarios with the method based on the universality of hot carrier degradation extended to the case featuring feedback.**

Keywords – Analog / Mixed-Signal Aging; bond-dispersion model; circuit aging; circuit reliability; hot carrier injection (HCI); lateral scaling; universality of degradation; voltage acceleration model

I. INTRODUCTION

Most Analog / Mixed-Signal systems typically leverage feedback of some sort to ensure output precision in the face of changing circuit or load conditions. Of late, there has been growing interest towards understanding the impact of feedback on the aging mechanics in these circuits [1]. A popular method for modeling aging induced parameter shifts thus far has been the constant power law model t^n, where t is the stress time and n a constant. However, recent studies have shown that aging models such as the constant power law model may need to be augmented with a time-varying stress condition for circuits employing feedback [1, 2, 3, 4]. One such example of a circuit exhibiting accelerated aging due to time-varying stress is the diode-connected MOSFET (Fig. 1) As the NMOS device ages due to hot carrier injection (HCI), the diode voltage must increase to maintain the same stress current which in turn aggravates the HCI aging. Iterative simulation frameworks that account for the change in the stress condition over time have been proposed [1, 2, 3]. However, previous efforts have several drawbacks such as (i) lack of comprehensive experimental data from a real test-chip and (ii) prediction results suggesting runaway behavior which could not be experimentally verified due to HCI saturation (Fig. 2). These limitations can lead to gross overestimations of aging for high reliability applications and hence, improper design margins when extrapolating down to usage conditions. In this work, we present a 1-dimensional array-based test structure implemented in a 1.2V 65nm LP process featuring diode-connected MOS transistors as Device-Under-Test (DUTs) and offering the flexibility to investigate the aging behavior for a particular DUT type in either absence or presence of feedback.

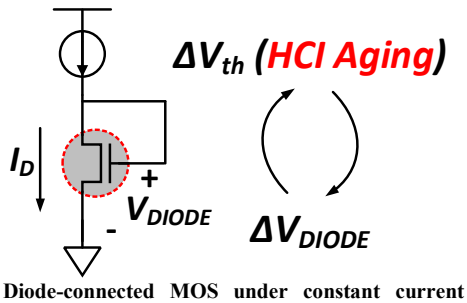

Fig. 1. Diode-connected MOS under constant current stress resulting in accelerated V_{th} shift due to increasing diode voltage with time.

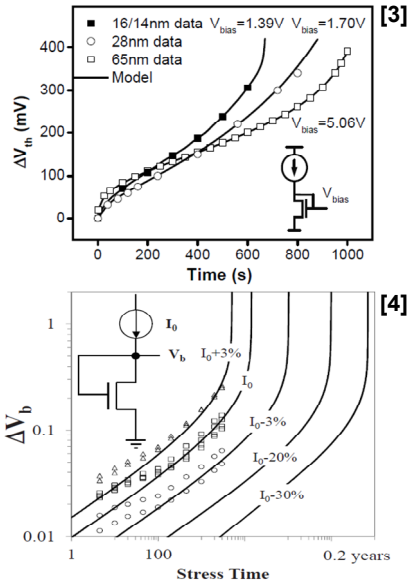

Fig. 2. Prior Art [3, 4]: Lack of comprehensive test-data does not clearly specify the extent of model fit and owing to the temporal universality of HCI degradation [6] requires long-term stress results at lower bias voltages to actually verify if only gradual aging without the possibility of runaway [2] occurs at voltages lower than the critical voltage detailed in [2].

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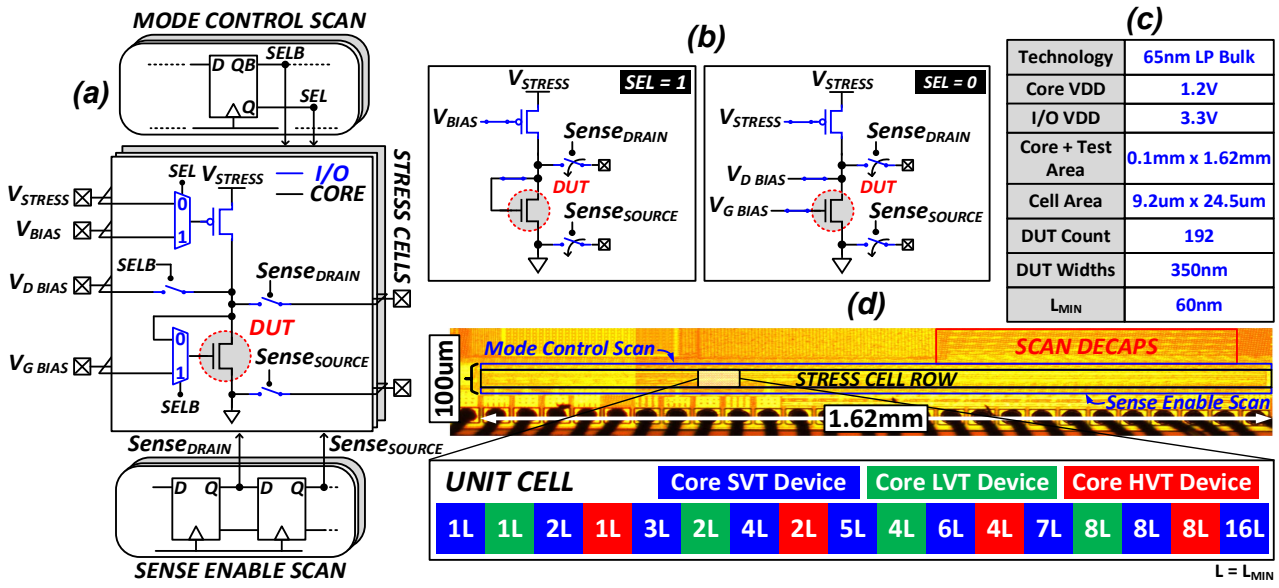

Fig. 3. (a) Stress-Cell of the proposed array-based test structure (b) Operation Modes (c) Implementation summary (d) Die Photo & Unit-Cell.

II. Test Structure & Measurement Methodology

A. Array-Based Test Structure

Fig. 3(a) illustrates the schematic of the unit stress cell with the DUT housed within. The array consists of a single row of such stress cells with dedicated scan bits per cell to either independently enable stress for one or multiple cells or enable sensing of the drain and/or the source voltages for a particular DUT of interest. Each stress cell contains a wide (W/L=30µm/1.2µm) thick oxide (3.3V) PMOS header which can either (i) be turned on fully to enable DUT selection when using the source measure unit (SMU) for applying a given stress current or voltage, or (ii) used as a near ideal on-chip current source with an elevated headroom and fixed bias to mimic a real test case scenario. Control signals to the stress cells come from the scan chains followed by level shifters for up-converting to the stress voltage. Three shared analog inputs V_{BIAS}, $V_{D\ BIAS}$ and $V_{G\ BIAS}$ are used for biasing the stress cells whereas V_{STRESS} works as the power supply of the entire array. A total of 17 different DUT types were implemented in a single unit block which was then instantiated over to form the 1-dimensional array (Fig. 3(d)). Fig. 3(d) also shows the die microphotograph of the 65nm test chip along with a description of the different DUT types. The stress cells can be programmed using the mode control scan chain to keep multiple devices under one of 'STRESS' (SEL = 1) or 'IDLE' (SEL = 0) modes as illustrated in Fig. 3(b).

B. Measurement Methodology

Fig. 4 shows the measurement methodology for the stress experiments. The DUT can be stressed using a constant current by operating the thick oxide PMOS header in the linear region and having the SMU generate a known stress current. For constant voltage stress experiments, a similar methodology

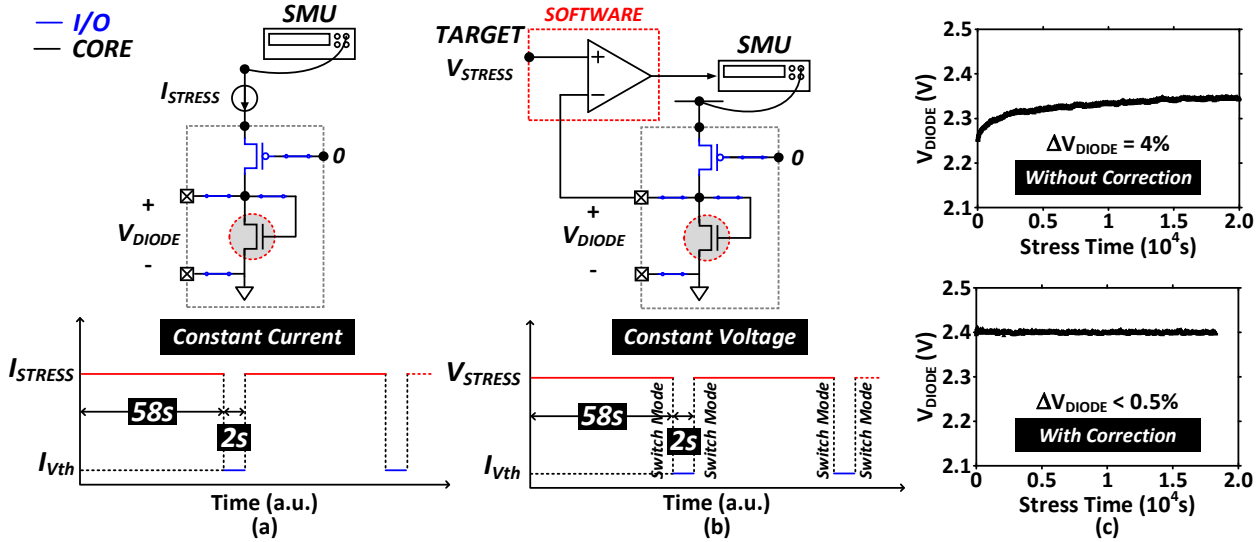

Fig. 4. Measurement methodology: (a) Constant Current Stress (b) Constant Voltage Stress & (c) Measured V_{DIODE} with and without correction.

can be adopted wherein the PMOS header is kept fully on and the desired stress voltage is sourced using the SMU. However, this leads to a complication: as the DUT ages overtime, the decrease in DUT current leads to a reduced drop across the PMOS device creating instead an accelerating stress condition like the constant current case. To ensure constant voltage at all times, a feedback loop is implemented in software (Fig. 4 (b)) which monitors the sensed V_{DIODE} every few seconds and compares its value with the target stress voltage to adjust the SMU output voltage accordingly. Fig. 4(c) shows the measured V_{DIODE} results with and without the correction mechanism implemented. Less than 0.5% (10mV) of variation in the sensed value of V_{DIODE} for 2.4V of stress was observed post-correction. In a measurement cycle of 1 minute, the DUTs were stressed for 58 seconds (with samples being recorded every 2s) and the last 2s were used for sampling the V_{th} using the method of constant current (Bottom Figures 4(a) & 4(b)).

III. Measurement Results & Aging Prediction

A. Measured V_{DIODE} and V_{th}

Fig. 5 compares the evolution of V_{DIODE} and V_{th} for the constant current and constant voltage stress experiments.

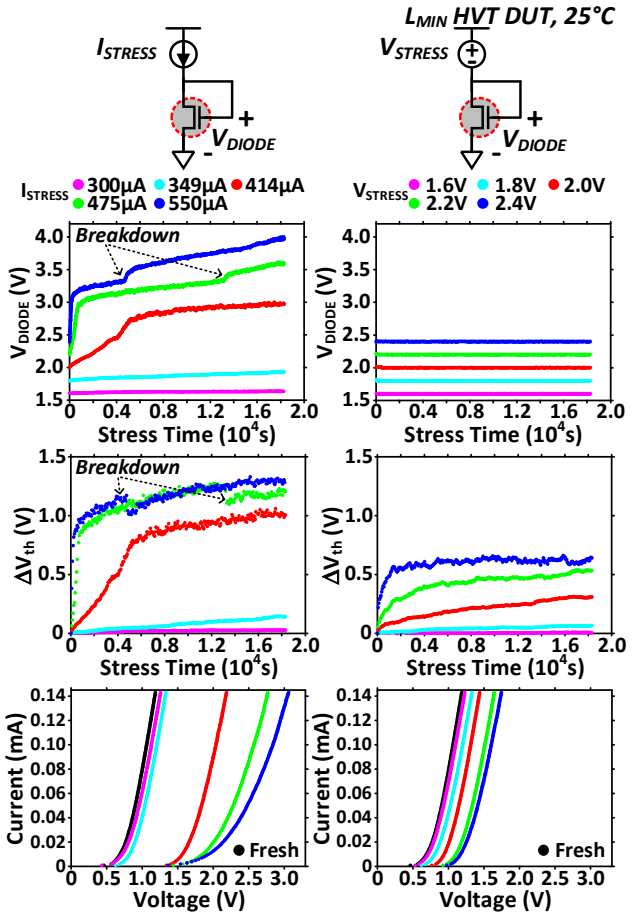

Fig. 5. Shift in V_{DIODE} and V_{th} for constant current stress (left column) and constant voltage stress (right column) for identical values of starting stress biases. V_{th} was monitored by applying a small fixed bias current and measuring the diode voltage. Bottommost figure shows the fresh & post-stress diode I-V curves.

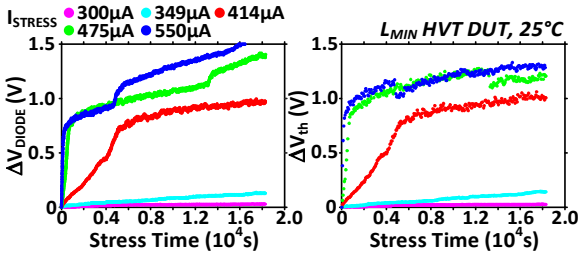

Fig. 6. Shift in V_{DIODE} compared side by side with the shift in V_{th}. The shift in V_{DIODE} closely follows the shift in V_{th}.

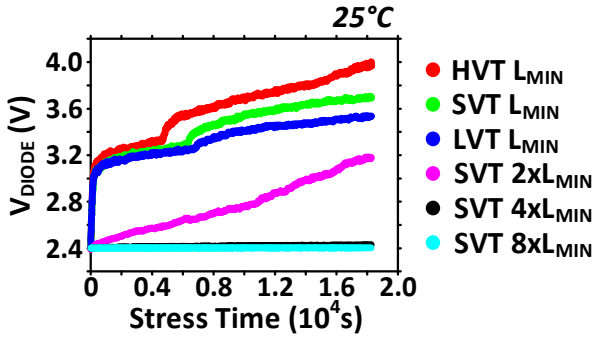

Fig. 7. Measured V_{DIODE} for core DUTs with different V_{th} (LVT, SVT, HVT) and channel lengths (L, 2L, 4L, 8L) under constant current stress for identical values of starting stress bias (= 2.4V).

Although the results shown are for the case of minimum channel length High V_{th} (HVT) DUTs, similar trends were observed for the Standard V_{th} (SVT) and Low V_{th} (LVT) DUTs as shown in Fig. 7. As can be seen in Fig. 5, aging is more pronounced for the constant current case due to the increasing stress voltage overtime. Looking at the degradation traces for both the stress conditions, it can be concluded that (1) the degradation which is primarily due to HCI, saturates over time and, (2) the onset of saturation depends on the initial value of the stress bias. These observations are in alignment with the bond-dispersion model [5] and point to the universality of the degradation [6], presented comprehensively in [7]. Bottommost figures in either column in Fig. 5 show the measured fresh and post-stress diode I-V curves and are reflective of the high V_{th} degradation in presence of feedback. Once the aging rate saturates, the device (for constant current stress) continues to age at a slower rate until oxide breakdown after which the current drawn by the gate causes a drop across the transmission gate connected between the drain and gate. This is evinced by both the jump in V_{DIODE} (needed to force the same current on account of reduction in the gate bias due to IR drop in the transmission gate) and drop in the measured V_{th} (owing to the parallel current path drawing a portion of the small current needed for measuring V_{th}). For constant voltage case, the range of stress values applied in our experiments (<= 2 x Nominal VDD) were not sufficient to cause an oxide breakdown (nearly 3.3V, as can be seen from the constant current case). Longer channel length devices showed substantially higher resilience to HCI degradation even in presence of feedback (Fig. 7).

Fig. 6 shows the measured shift in diode voltage for the constant current case plotted along side the shift in V_{th}. As can

be observed from Fig. 6, the shift in V_{DIODE} closely follows the shift in V_{th}. The insight from this result was used to update V_{DIODE} at each simulation time step for the iterative version of the model used for the constant current stress (discussed in the next section).

B. Modeling the Constant Voltage and Constant Current induced degradation

Fig. 8 shows the results of using the simple constant power law model [8] for modeling the constant voltage induced V_{th} degradation (left) at two different stress biases. The model provides a good fit to the experimental data at lower stress voltages and/or for shorter stress durations but does not predict the onset of saturation occurring for longer stress times or at higher stress biases [6]. When an iterative methodology (similar to [3]) is employed to update the stress condition for the constant current case, the model correctly predicts the initial super-exponential trend but fails to account

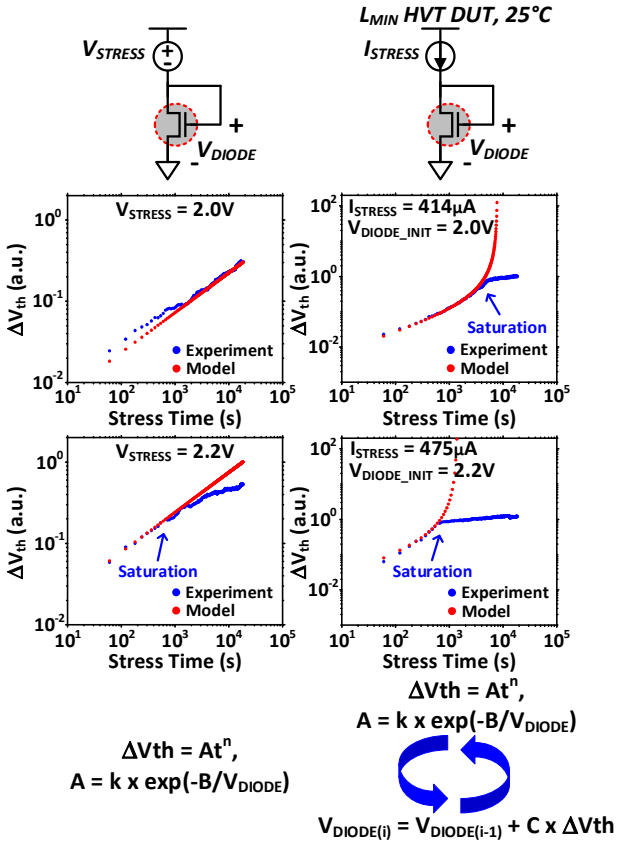

Fig. 8. Using the constant power law model [8] in conjunction with an iterative approach leads to an accurate fit with the constant current stress data as shown in the figure. One limitation of this method is that it cannot incorporate the onset of saturation. This figure shows measurement data from Fig. 5 plotted on log scale along with the modeled data. Where n = 0.49, B = 26.5, k = 1400 & C = 0.93 (close to 1, as expected from Fig. 6). Constants derived from curve fitting the constant voltage stress results were used as it is for the constant current case with the stress condition updated iteratively (similar to [3]) at each simulation time-step (60s, similar to our measurement).

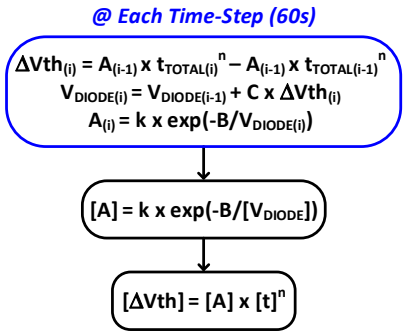

Fig. 9. Iterative flow detail for the constant current model in Fig. 8 (Right) implemented in MATLAB, A_0 = A (Constant voltage case).

for the onset of saturation, thus resulting in a limited fit depending upon the applied stress bias (more at lower voltages or shorter stress durations and less at higher stress biases or longer durations) This is particularly concerning for the constant current (feedback) case where starting from a higher stress bias can cause a high initial aging rate followed quickly by the onset of saturation after which the device continues to age at a much slower rate (Fig. 8, Right). Hence, an alternative method is needed for modeling the entire degradation characteristics including saturation. This would be especially useful for high reliability applications with longer operational lifetimes.

C. Application of the method based on the universality of hot carrier degradation [6] to the diode-connected FET

In this section we explore the usefulness of the temporal universality of HCI degradation, also referred to as lateral

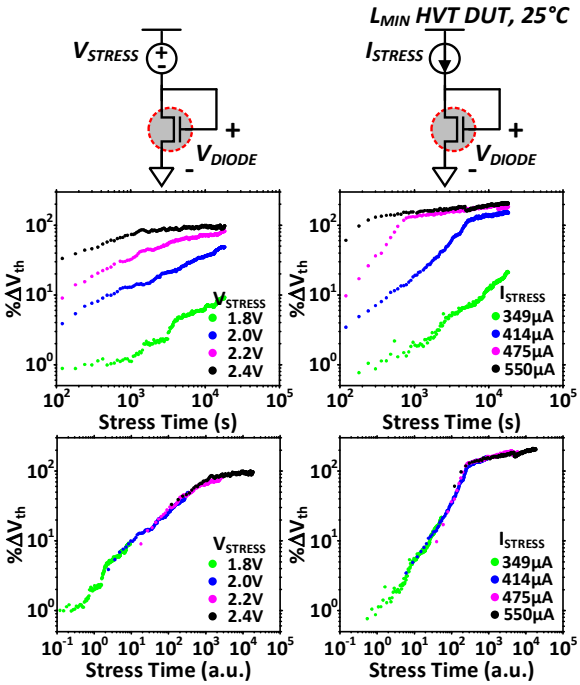

Fig. 10. Time Scaling the test-data results in universal curves [6] for both constant voltage and constant current (feedback) stress cases. This figure shows the original (top) and time-scaled (bottom) versions of measurement results from Fig. 5 plotted on a log scale.

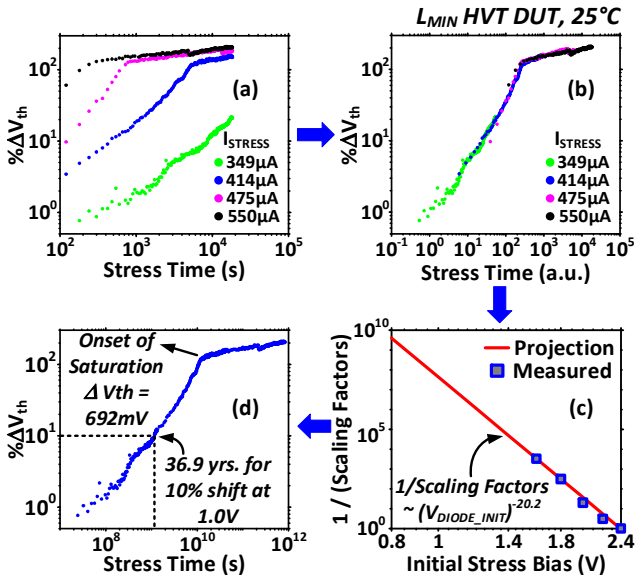

Fig. 11. Application of the method based on universality of degradation [6, 9] to the diode-connected DUT: (a) Short-term stress measurements under constant current stress; (b) Universal curve obtained by time scaling the measurement results in (a) ; (c) Voltage acceleration for scaling factors [9] obtained using the 'initial' values of diode stress biases (V_{DIODE_INIT}) developed corresponding to stress currents in (b) / Fig. 5 (Left Column). (d) Aging prediction at a usage voltage (=1.0V) including the onset of saturation.

scaling, in the context of circuits with varying stress conditions. Fig. 10 shows the original as well as the time-scaled versions of the V_{th} degradation curves corresponding to different values of stress biases for the constant voltage and the constant current stress experiments. Upon time scaling the measured results on the log scale, we can clearly observe the universality of degradation (i.e. the time-scaled versions all lie on different parts of a common curve) holding for both the constant voltage (a known result, [6]) and the constant current (feedback) stress cases. Fig. 11 then illustrates the application of this method to the feedback case. Following a few short-term measurements at different stress currents, the results are laterally scaled along the time axis. The projection for scaling factors [9] is then derived from the measured values of 'initial' stress biases (V_{DIODE_INIT}), corresponding to the different values of stress currents and the scale factors obtained in the previous step. Using this projection, accurate lifetime prediction including the onset of saturation becomes possible for a diode usage voltage (for instance 1.0V, as illustrated in Fig. 11 (d)). Finally, Fig. 12 presents real-time long-term stress data for lower initial stress biases such as 1.6V (300uA) and 1.8V (349uA) showing the onset of saturation for longer stress times and time scaled versions of the same, (using the scaling factors derived from the short-term measurement data / projection) fitting well to the universal curve. On account of the DUTs experiencing a common range of stress voltages (V_{DIODE}) for the constant current case, there is a greater overlap between the individual degradation traces in presence of feedback. Hence, even fewer short-term measurements (which are also quick, on account of accelerated aging) are now needed to construct the full universal curve. It should also be noted from Fig. 12 that the V_{th} undergoes the same total shift overtime starting at a lower bias (owing to the universality of degradation) and thus the bias itself would undergo the same shift as for a higher initial value albeit in a longer time. Hence, the risk of a significant deviation overtime in the initially applied value of bias still remains even for lower initial biases.

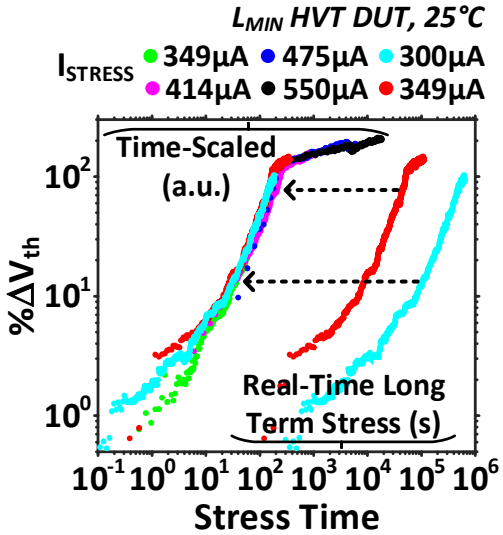

Fig. 12. Real-time long-term stress data at diode biases of 1.6V (cyan) and 1.8V (red) fits well using the projected scaling factors derived in Fig. 11 (c). Then, using the inverse of scale factors and unrolling the Universal Curve in time provides an accurate estimate of the aging dynamics and hence, shift in the bias for an initial value of stress bias applied to the diode.

IV. Conclusion

This work presents comprehensive test-data showcasing the detailed impact of feedback on aging. We present an array-based characterization vehicle intended specifically to quantify the impact of feedback on aging. The efficacy of iteratively updating the stress condition for lifetime prediction in such scenarios is also evaluated and it is observed that simple models that don't account for saturation provide a limited fit (depending on the stress level or the stress duration) and predict non-realistic super exponential rates thereafter. Finally, we discuss the application of the method based on the universality of hot carrier degradation to the feedback stress case. Owing to greater overlap between the individual degradation curves coupled with accelerated aging in presence of feedback, only a few short-term measurements at different stress currents are sufficient to construct a universal curve that can accurately predict the aging dynamics including saturation given the initial stress bias of the diode-connected device.

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